Heterogene III-V/silicium fotonica:
bondingtechnologie en geïntegreerde componenten

Heterogeneous III-V/Silicon Photonics:
Bonding Technology and Integrated Devices

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Doctoreren. Vier jaar lang. Het is de moeite geweest. Alhoewel volgens sommige outsiders gelijk gesteld aan bezigheidstherapie of een uit de hand gelopen hobby, heb ik in die vier jaar geleerd wat doctoreren echt is. Het is je, met veel vallen en opstaan maar met een quasi grenzeloze vrijheid, verdiepen in wetenschappelijk onderzoek. Best niet te onderschatten. Natuurlijk heeft het zo zijn extra-legale voordelen, zoals je 's morgens nog eens kunnen draaien als je vriendin de deur uitgaat op weg naar haar werk, of het bijwonen van talrijke conferenties, verspreid over de hele wereld ... Eigenlijk heb ik er nooit aan getwijfeld of doctoreren wel iets voor mij zou zijn.

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Het amusement ermee!

Günther Roelkens
Gent, 1 februari 2007

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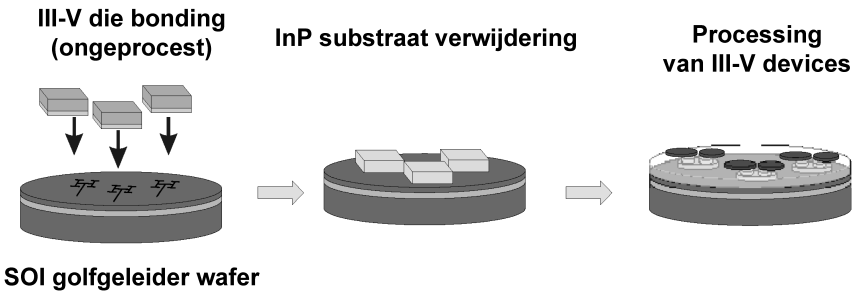
Nederlandstalige Samenvatting

1. Heterogene integratie

Geïntegreerde fotonische circuits bieden het potentieel om goedkope en compacte optische functies te realizeren. Silicium-op-isolator (SOI) treedt naar voren als een veel belovend materiaal om deze componenten in te integreren, omwille van zijn groot omni-directioneel brekingsindexcontrast. Bovendien kan gebruik gemaakt worden van de micro-elektronica processing infrastructuur voor de fabricage van deze componenten. De integratie van licht emitterende, licht versterkende en licht detecterende componenten in het nabije infrarood, rond de telecommunicatiegolflengtes van 1.55μm en 1.3μm (waarvoor de attenuatie en dispersie in een optische vezel respectievelijk het laagst zijn), wordt echter bemoeilijkt door de indirecte bandkloof van silicium. Alhoewel vooruitgang wordt geboekt op het vlak van lichtemissie uit silicium, ofwel door het silicium te wijzigen op een nanometer schaal of door zijn niet-lineaire optische eigenschappen uit te buiten, zullen deze componenten binnen afzienbare tijd geen betere performantie halen dan hun III-V halfgeleider tegenhangers, die vandaag de dag de state-of-the-art optische componenten leveren voor de telecommunicatiemarkt. Om geïntegreerde fotonische circuits te fabriceren die zowel passieve als actieve optische functies bevatten, wordt in dit werk de heterogene integratie van passieve SOI golfgeleidercircuits en actieve InP/InGaAsP componenten voorgesteld. Om de kost van het integratieproces te verminderen, zowel in tijd als in consumptie van duur III-V epitaxiaal materiaal, wordt in dit werk een die-to-wafer bonding proces voorgesteld, waarin verschillende ongeproceste InP/InGaAsP dies met de epitaxiaallagen naar beneden toe gekleefd worden op de geproceste SOI wafer. Dit reduceert de materiaalconsumptie omdat



Figuur 1: Heterogene integratie van III-V componenten en SOI golfgeleidercircuits - procesvolgorde

enkel III-V materiaal wordt geplaatst daar waar het nodig is en reduceert ook de tijd nodig voor het integratieproces daar slechts een beperkte alignatienauwkeurigheid nodig is, omwille van het ontbreken van enige structuur in de epitaxiaallagen. Na het verwijderen van het InP substraat, kunnen actieve opto-elektronische componenten worden gefabriceerd in de epitaxiaallagen, gebruik makend van waferschaaltechnieken en lithografisch gealigneerd ten opzichte van de onderliggende structuren in het SOI. De procesvolgorde is schematisch weergegeven in figuur 1.

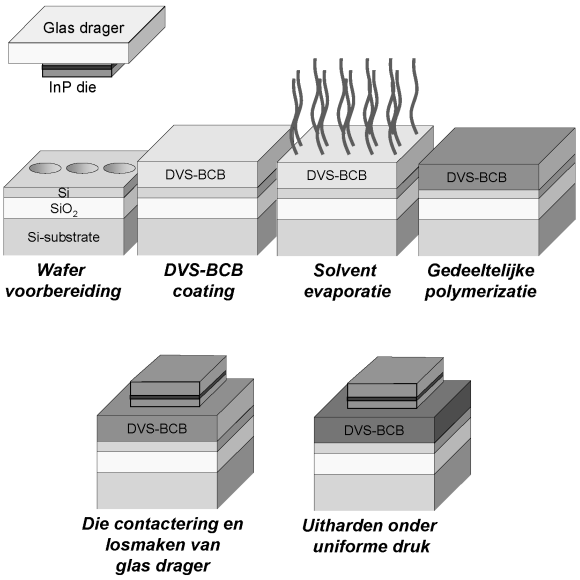
Alhoewel er verschillende methodes zijn om een InP/InGaAsP epitaxiale lagenstructuur te integreren op een SOI substraat (epitaxiale groei, moleculaire bonding, adhesive bonding, anodisch bonden, metallische bonding), werd in dit werk een adhesive bonding proces voorgesteld, daar deze enkele belangrijke voordelen heeft. De minder strikte vereisten qua oppervlaktekwaliteit in termen van contaminatie en partikels, gecombineerd met de planarizerende eigenschappen van het spin coating proces voor het aanbrengen van het polymeer, bieden een versoepelde substraatvoorbereiding. Bovendien grijpt het bonding proces plaats bij lage temperatuur, hetgeen de spanningen in de gebonde lagenstructuur vermindert. Het thermisch hardende polymeer DVS-BCB (divinylsiloxane-bis-benzocyclobutene) werd geselecteerd voor de procesontwikkeling omwille van zijn excellente planarizatie eigenschappen, zijn hoge glastransitietemperatuur (hetgeen belangrijk is om voldoende thermisch budget te hebben voor de post-processing van de epitaxiaallagen), de lage krimp van het materiaal en het feit dat geen bijprodukten gecreëerd worden tijdens het uitbakken.

2. Bonding proces ontwikkeling

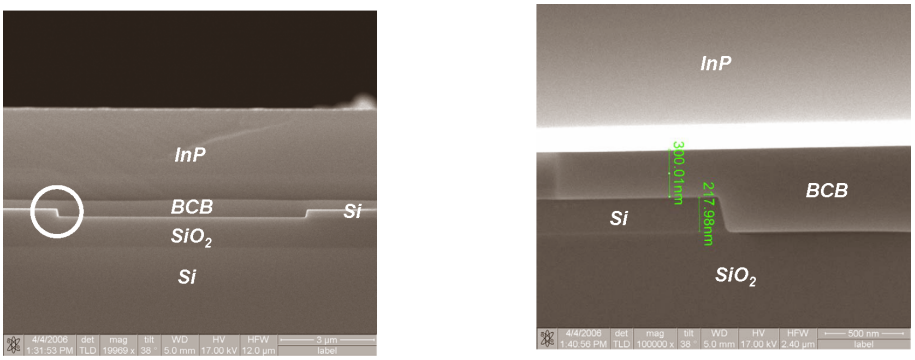
Twee types bonding procedures werden ontwikkeld in dit werk, één gebaseerd op standaard DVS-BCB laagdikten die behaald kunnen worden met commercieel verkrijgbare oplossingen (>1μm) en één gebaseerd op dunne DVS-BCB bonding lagen (>300nm), waarvoor een zelf gemaakte DVS-BCB oplossing werd gebruikt. Terwijl in het eerste geval de planarizatie van de SOI topografie en de insluiting van partikels aan de bonding interface geen belemmering vormen, is dit veel meer het geval voor de dunne DVS-BCB lagen. De planarizerende eigenschappen van het DVS-BCB werden onderzocht, hetgeen resulteerde in een aantal design rules voor de SOI topografie om voldoende planarizatie te bekomen. De voorbereidingsprocedure voor beide substraten werd geoptimaliseerd om contaminatie van de te bonden oppervlakken te vermijden en om de sterkte van de bond te maximaliseren. Na het reinigen van de substraten en spin coaten van het DVS-BCB worden de substraten samengebracht in een vacuumomgeving om het insluiten van lucht aan de bonding interface te vermijden. Het DVS-BCB wordt uiteindelijk uitgehard onder een uniforme druk om een intiem contact van beide substraten te bereiken. Het ontwikkelde bonding proces is schematisch weergegeven in figuur 2. Bonding was succesvol tot DVS-BCB laagdiktes van 300nm op een 220nm hoge SOI topografie, zoals getoond in figuur 3. Na het bonden wordt het InP substraat verwijderd door middel van een combinatie van mechanisch verdunnen en chemisch etsen tot een etsstoplaag wordt bereikt. De spanningen in de gebonde lagenstructuur werden zowel theoretisch als experimenteel bestudeerd in dit werk, hetgeen aantoonde dat de spanningen bij kamertemperatuur voldoende laag zijn voor optische toepassingen. Het post-bonding thermisch budget is beperkt om geen dislocaties in de gebonde epitaxiale lagenstructuur te genereren.

3. Optische koppelingsschema's

Naast het ontwikkelen van een DVS-BCB bonding proces werden in dit werk verschillende schema's geanalyseerd om op efficiënte manier licht te koppelen tussen de SOI passieve golfgeleiderlaag en de gebonde epitaxiale lagenstructuur. Een koppelingsschema gebaseerd op adiabatische modetransformatie toont de hoogste koppelingsefficiëntie, de grootste fabricage tolerantie en grootste optische bandbreedte, ten nadele van zijn afmetingen. Koppelingsschema's gebaseerd op diffrac-



Figuur 2: Ontwikkeld DVS-BCB bonding proces



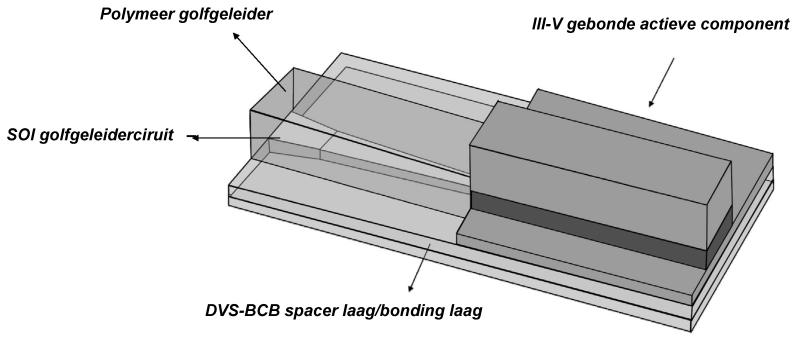
Figuur 3: Cross-sectie van een gebonde lagenstructuur

tieve roosters tonen een iets lagere efficiëntie en optische bandbreedte maar zijn veel compacter. Het voorgestelde koppelingsschema is getoond in figuur 4, hetgeen een geïnverteerde adiabatische taper koppelaar in SOI weergeeft, waarboven zich een polymeergolfgeleider bevindt. Deze polymeergolfgeleider is gekoppeld aan de actieve InP/InGaAsP lagenstructuur. Hoge koppelingsefficiëntie over een grote optische bandbreedte kan op deze manier worden bereikt, zowel voor de koppeling van licht dat zich in de SOI golfgeleider bevindt naar een III-V fotodetector in de InP/InGaAsP laag of om licht vanuit een gebonde laserdiode te koppelen naar de SOI golfgeleider.

Daar het probleem van de koppeling van licht tussen beide golfgeleiderlagen sterk verwant is met het probleem van optische koppeling met een glasvezel, werden in dit werk de geanalyzeerde koppelingsschema's ook toegepast op dit probleem. Zowel een koppelaar gebaseerd op een adiabatische taper als een koppelaar gebaseerd op een diffractief rooster werden geanalyseerd en gefabriceerd. Alhoewel beide structuren reeds voorgesteld werden in de literatuur, werden enkele markante verbeteringen aangebracht. In het geval van de adiabatische koppelaar werd de fabricage van de taper tip door middel van standaard 248nm diep UV lithografie mogelijk gemaakt door een DVS-BCB spacerlaag aan de koppelstructuur toe te voegen. Voor het diffractief rooster werd de haalbare koppelingsefficiëntie sterk verhoogd door een extra silicium laag te deponeren alvorens het rooster te etsen. Dit concept werd verder uitgebreid naar het gebruik van het rooster als een duplexer, waarbij twee golflengtebanden ruimtelijk gescheiden kunnen worden in twee verschillende golfgeleiders, waarvoor een patentaanvraag werd ingediend.

4. Componenten gebaseerd op DVS-BCB bonding

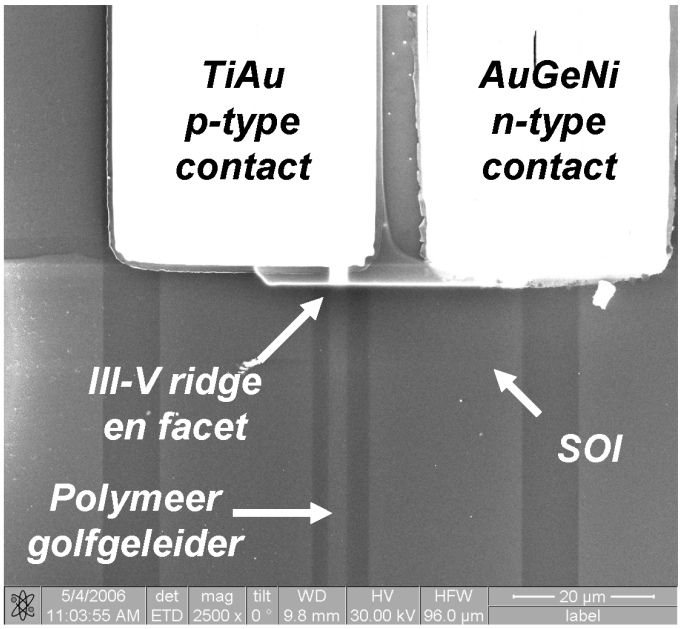
In dit werk werden gebonde licht emitterende componenten gefabriceerd en gekarakteriseerd, zowel stand-alone componenten als componenten gekoppeld naar een onderliggend golfgeleidercircuit. Gebonde LEDs, gebonde Fabry-Perot laserdiodes en DFB laserdiodes werden gedemonstreerd, terwijl een geïntegreerde Fabry-Perot laserdiode gekoppeld werd naar een SOI golfgeleidercircuit. Het thermisch gedrag van deze componenten werd grondig bestudeerd, daar de lage thermische geleidbaarheid van de DVS-BCB bondinglaag een efficiënte warmteafvoer in de weg staat. Dit kan worden omzeild door een extra warmteafvoer te integreren bij de laserdiode. Een foto van een laserdiode geïntegreerd



Figuur 4: Koppelingsschema gebaseerd op een geïnverteerde adiabatische taperstructuur

op en gekoppeld naar een SOI golfgeleidercircuit wordt getoond in figuur 5. Het InP/InGaAsP epitaxiaal materiaal gebond op het golfgeleidercircuit is duidelijk zichtbaar, evenals de laserdiode die erin gefabriceerd is en de eraan gekoppelde polymeergolfgeleider. De SOI adiabatische taperstructuur ligt begraven onder de polymeergolfgeleider en is niet zichtbaar. Laserwerking werd waargenomen in deze structuren en koppeling naar het onderliggende golfgeleidercircuit werd gedemonstreerd. Naast deze licht-emitterende componenten werden in dit werk ook III-V fotodetectoren geïntegreerd op een SOI golfgeleidercircuit.

Behalve voor de integratie van passieve en actieve optische functies, kan het DVS-BCB transfer proces ook gebruikt worden om nieuwe types optische componenten te fabriceren, omwille van de mogelijkheid tot dubbelzijdige processing (of optische toegang). Dit leidde tot de demonstratie van thermisch bistabiele ringresonatoren bij laag optisch vermogen, hoog efficiënte roosterkoppelaars gebaseerd op een goud spiegel en de integratie van een SOI interconnectielaag bovenop een CMOS substraat.



Figuur 5: Bovenaanzicht van de gefabriceerde laserdiodes gekoppeld naar een SOI golfgeleidercircuit

English summary

1. Heterogeneous integration

Photonic integrated circuits (PICs) offer the potential of realizing low-cost, compact and high yield optical functions. Silicon-on-insulator (SOI) is an emerging material platform for this integration, due to the large omni-directional refractive index contrast that can be achieved. Moreover, the massive CMOS processing infrastructure can be used to process these optical components. The integration of light emitters, amplifiers and detectors in the near-infrared, around the telecommunication wavelengths of 1.55μm and 1.3μm (for which the optical fiber respectively has the lowest attenuation and dispersion), is hampered by the indirect band gap of silicon. Although several advances are being made to achieve light emission from silicon, either by changing the silicon material on a nano-scale or by exploiting its non-linear optical properties, in the foreseeable future these devices will not outperform their III-V semiconductor counterparts, supplying state-of-the-art opto-electronic components for the telecommunication market nowadays. In order to create photonic integrated circuits comprising both active and passive optical components, the heterogeneous integration of passive silicon-on-insulator waveguide circuits and active InP/InGaAsP components is proposed. To decrease the cost of the integration process, both in time and consumption of expensive III-V material, a die-to-wafer bonding process is proposed in this work, in which unprocessed InP/InGaAsP dies are bonded, epitaxial layers down, to the processed silicon-on-insulator wafer. This reduces the material consumption, as III-V semiconductors are only bonded where they are needed, and reduces the time to perform the integration process, as limited alignment accuracy is needed due to the absence of structure on the epitaxial layers. After removal of the InP substrate, active opto-electronic components can be fabricated in the InP/InGaAsP epitaxial layers, using

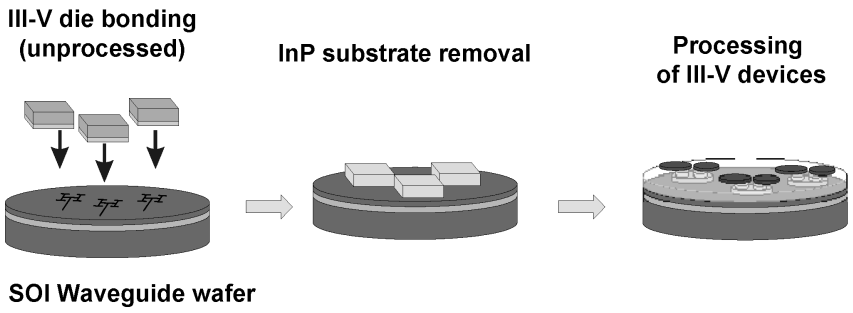


Figure 6: Heterogeneous integration of III-V devices and SOI waveguide circuits - process flow

wafer-scale processing, while being lithographically aligned to the underlying SOI features. The processing sequence is schematically shown in figure 6.

While there are various methods to create an InP/InGaAsP epitaxial layer structure onto the SOI waveguide wafer (hetero-epitaxial growth, molecular bonding, adhesive bonding, anodic bonding, metallic bonding), it is argued in this work that adhesive bonding offers some significant advantages over other bonding methods. The relaxed requirements on surface cleanliness, contamination and surface roughness combined with the planarizing action of the adhesive spin coating process, offer a significant reduction in surface preparation. Moreover, the integration process is a low temperature process, reducing the stress in the bonded stack due to the difference in thermal expansion coefficients between silicon and III-V semiconductor. The thermosetting polymer DVS-BCB (divinylsiloxane-bis-benzocyclobutene) was selected for process development due to its excellent planarizing properties, its high glass transition temperature (supplying sufficient post-processing thermal budget), its low shrinkage and the fact that no by-products are created upon cure.

2. Bonding process development

Two types of bonding procedures were developed in this work, one based on standard DVS-BCB layer thicknesses achievable using commercially available solutions ($>1\mu$m), and one based on ultra-thin DVS-BCB layers (on the order of 300nm), for which a custom made solution

was applied. While in the former case, planarization of the SOI waveguide topography and the inclusion of particles at the bonding interface is less an issue, these are major causes of concern in the latter case. The planarization properties of the DVS-BCB spin coating process were assessed in this work, resulting in design rules for the SOI topography in order to achieve sufficient planarization. The cleaning and handling procedures for both SOI wafer and III-V dies were optimized, to avoid surface contamination and particles at the bonding interface and to maximize the bonding strength. After substrate cleaning and DVS-BCB spin coating, the substrates are attached in a vacuum environment in order to prevent the inclusion of air voids at the bonding interface. The bonded stack is finally cured using a uniform pressure on the stack to intimately contact both surfaces. The developed processing sequence is shown in figure 7. Bonding was successful down to 300nm thick bonding layers on a 220nm high SOI topography, as can be seen in figure 8. After bonding, the InP substrate is removed using a combination of mechanical grinding and wet chemical etching until an etch stop layer is reached. The stress in the bonded wafer stack was both theoretically and experimentally studied in this work, showing that, owing to the low bonding temperature, the stress at room temperature is sufficiently low for optical applications. The post-bonding thermal budget is limited however, in order to avoid dislocation generation in the bonded epitaxial layer stack.

3. Optical coupling schemes

Besides the development of a DVS-BCB bonding process, various schemes were analyzed in this work to efficiently couple light between the SOI passive waveguide layer and the bonded InP/InGaAsP epitaxial layer stack. Coupling schemes based on adiabatic mode transformation show the highest coupling efficiency, fabrication tolerance and optical bandwidth, at the expense of device footprint. Diffractive grating structures show slightly lower coupling efficiency and optical bandwidth, but the coupling structure footprint is much smaller. The proposed coupling scheme is depicted in figure 9, showing an inverted adiabatic taper coupler in SOI with a polymer waveguide overlay. This polymer waveguide is butt-coupled to the InP/InGaAsP active waveguide structure. High coupling efficiency over a large optical bandwidth can be achieved in this way, either by coupling light travelling in the SOI

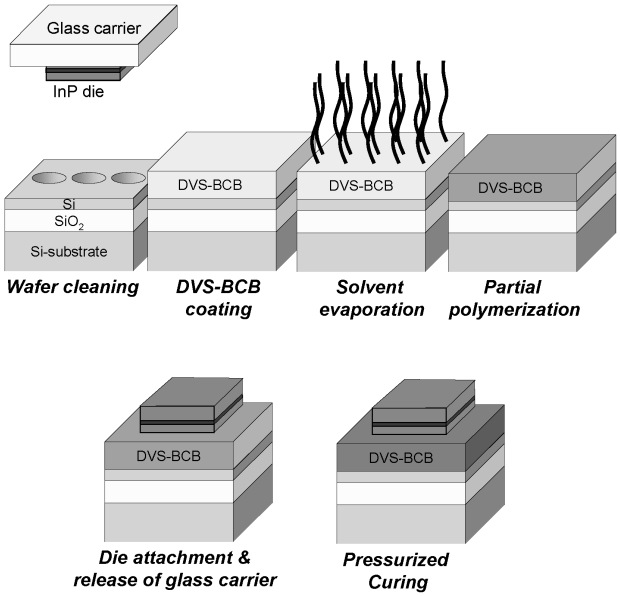


Figure 7: Developed DVS-BCB bonding process

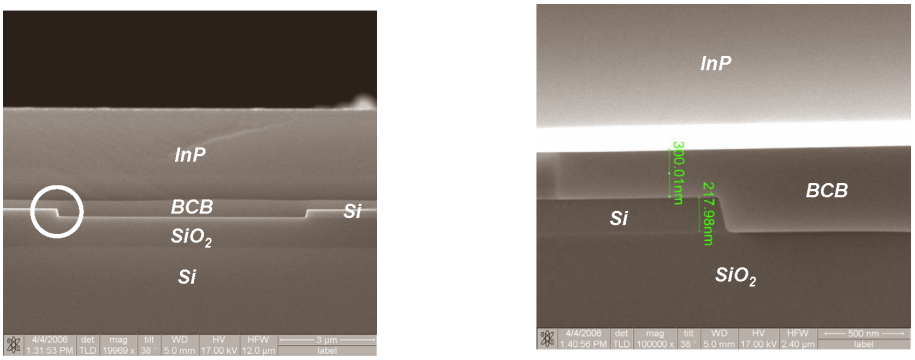


Figure 8: Cross-section of a bonded layer structure

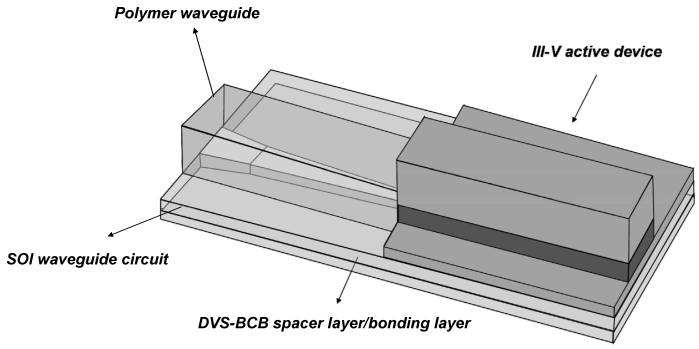


Figure 9: Inverted-taper-based coupling scheme using a polymer waveguide

waveguide to a III-V photodiode or by coupling light from a bonded laser diode to the SOI waveguide.

As the problem of the coupling of light between both waveguide layers is similar to the fiber-chip coupling problem, the analyzed coupling schemes were applied to interfacing a silicon-on-insulator waveguide circuit with an optical fiber. Both inverted-taper-based couplers and diffractive-grating-based couplers were analyzed. Although both type of coupling schemes were already presented in literature, in this work significant advances were made in the developed structures. For the case of an inverted taper coupler, the definition of the taper tip using 248nm deep UV lithography was made possible by adding a low refractive index DVS-BCB spacer layer. For the diffractive grating coupler approach, the obtainable fiber coupling efficiency was significantly enhanced by optimizing the grating coupler structure, i.e. by depositing an additional silicon layer prior to grating fabrication. This concept was further extended to use the grating coupler structure as a duplexer, spatially separating two wavelength bands into different waveguides, for which is patent application was filed.

4. Components based on DVS-BCB bonding

In this work, bonded light emitting devices were fabricated and characterized, both stand-alone devices and devices coupled to an underlying SOI waveguide circuit. Bonded LEDs, bonded Fabry-Perot and DFB laser diodes were demonstrated, while an integrated Fabry-Perot laser

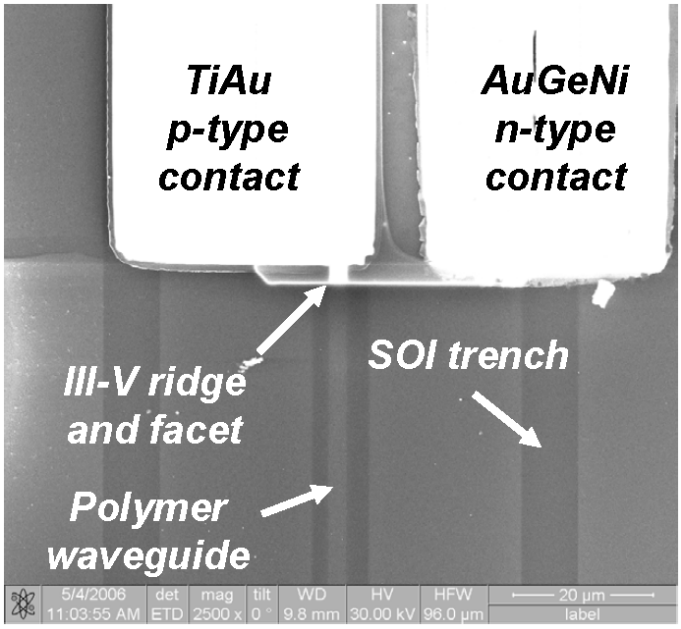


Figure 10: Top view of the fabricated laser diodes coupled to the SOI waveguide circuit

diode was coupled to an SOI waveguide circuit. The thermal behavior of these devices was thoroughly studied, as the low thermal conductivity of the DVS-BCB bonding layer hampers efficient heat sinking. This can be circumvented by integrating an additional heat sink circuit. An SEM picture of a laser diode integrated on top of and coupled to an SOI waveguide circuit is shown in figure 10. The InP/InGaAsP epitaxial layer structure bonded to the SOI waveguide circuit can clearly be identified, together with the laser diode fabricated in it and the butt-coupled polymer waveguide. The SOI inverted taper structure is buried underneath the polymer waveguide and cannot be seen. Laser emission was observed from these laser diodes and coupling to the underlying SOI waveguide circuit was demonstrated. In addition to these light emitting components, also III-V photodetectors were integrated on an SOI waveguide circuit in this work.

Besides for the integration of passive and active optical functions, the DVS-BCB layer transfer process can be used to fabricate new types of devices due to the possibility of double-sided processing (or optical access). This led to the demonstration of low-power bistable bon-

Chapter 1

Heterogeneous integration for photonics

Best of both worlds
Van Halen

In this chapter, the need for heterogeneous integration will be motivated by means of several applications in photonics, in which this technology gives added value. The heterogeneous integration of III-V semiconductors and silicon photonic circuits will be discussed in detail. The various ways in which heterogeneous integration technology can be interesting for photonics will be outlined.

1.1 Telecommunication and photonics

1.1.1 History of telecommunication

Telecommunication refers to long-distance communication. The old Greece and the Roman empire already possessed good organized telecommunication systems. Fire signals were given from mountain to mountain or from tower to tower. The Greek poet Aischylos (525BC), a soldier in the fight of Marathon, describes in one of his poems a "fire post", probably the first line of sight transmission in the world.

Since then, things have changed. The advent of modern telecommunication came in 1837, when Samuel Morse patented the first electrical telegraph. The first telegraph message was sent from Washington to Baltimore in 1844, while in 1865 the first functional telegraph line between Europe and America was finished. A next major step in telecom-

munication came in 1876, when Alexander Graham Bell patented his telephone system. Bell founded the "Bell Telephone Company". This company delivered and installed 50000 telephones within the first three years and was soon the world's largest telephone company known as "American Telephone and Telegraph Company".

The discovery of electromagnetic waves (predicted by James Maxwell in 1873 and experimentally observed by Heinrich Hertz in 1888) opened new ways of transmitting information. In 1895, the Italian Marconi experimented with wireless telegraphy. He was very successful: already in 1899 he was able to send his messages across the Channel between France and England. Only two years later the first transatlantic signals were sent across the ocean from Europe to North America.

The advent of television further diversified the type of information that could be transmitted. The first commercial television programmes were broadcast by the BBC in Great Britain in 1936. Communications satellites were first introduced in the mid-1960s (TELSTAR 1) and have been used for telecommunication and for television relay since.

A stepping stone in telecommunication history came in 1966, when for the first time light-guiding glass fiber was used to transmit phone calls, resulting in a massive increase in the amount of phone calls that could be transmitted at once. Infrared light was used to transmit the signal and the light was guided in the optical fiber by total internal reflection. In 1977, an optical telecommunication system was installed in downtown Chicago. Each optical fiber pair carried the equivalent of 672 voice channels. Today more than 80 percent of the world's long-distance voice and data traffic is carried over optical fiber cables.

In 1969, the Advanced Research Projects Agency (ARPA) of the US Department of Defence commissioned the development of a computer net, which helped on the one hand to communicate in case of a nuclear attack and on the other hand to improve the co-operation between the different research departments. The ARPANET for the first time connected universities and military instances. Soon, methods were built into the system for electronic file transfer and for electronic mail. The basic property of the network was that it kept functioning when one or more lines were destroyed: the system automatically switched to an other line, which was intact. When there came more networks worldwide, scientists searched for a method to connect the several systems together so that they could communicate without limits. Under the name "internetting project", a new project started to achieve this.

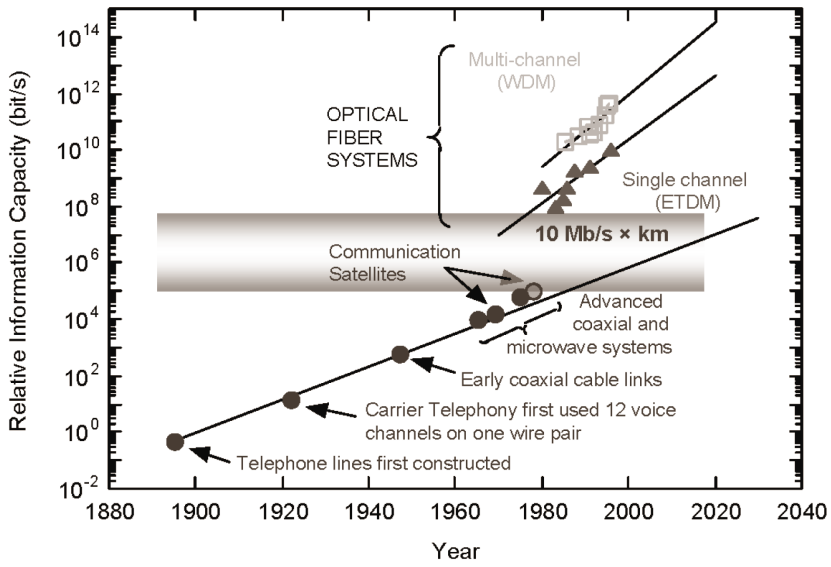


Figure 1.1: Overview of the information capacity across a range of communication technologies and time (from [1])

In 1980 at CERN, Tim Berners-Lee proposed a project based on the concept of hypertext, to facilitate sharing and updating information among researchers. In 1989, when CERN was the largest Internet node in Europe, this concept led to the development of the World Wide Web (WWW) as we know it today.

After the public discovered the Internet in the late nineties, the number of hosts has increased dramatically. Since then, the Internet has gone commercial. Massive amounts of data have to be sent between the various computers in the network and the electrical wires, which were used in the original small networks, can no longer handle this huge data stream. The use of and demand for optical fiber in telecommunication industry have grown tremendously ever since.

An overview of the achievable information capacity across a range of communication technologies and time is shown in figure 1.1. The cross-over point to optical technology occurred in the early eighties as soon as the bandwidth distance product of 10Mbit/s x km was required.

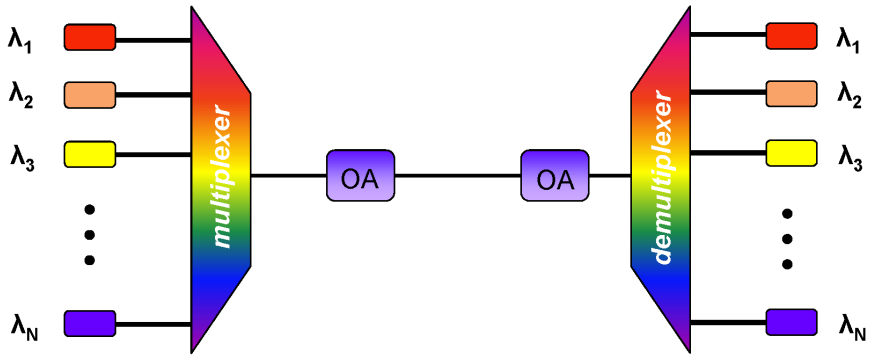


Figure 1.2: The structure of a WDM link (OA=optical amplifier)

1.1.2 Fiber-optic communication

The high bandwidth (meaning the amount of data that can be transmitted per second) of the optical fiber implies that a single optical carrier can be modulated at about 25.000 Gbps around a wavelength of 1.55 μm before transmission losses of the optical fiber would limit transmission. To efficiently use this large bandwidth of the optical fiber, wavelength division multiplexing (WDM) techniques are used in which multiple optical carrier signals can be multiplexed on a single optical fiber by using different laser light wavelengths to carry different data signals. Both coarse WDM (CWDM) and dense WDM (DWDM) techniques are used, which differ in the amount of wavelength channels used per fiber. Dense WDM tends to be used at a higher level in the communications hierarchy, for example on the internet backbone networks connecting places all over the world. Coarse WDM is typically used on shorter-distance links with lower aggregate bandwidth requirements, for example in short-distance data communication or in fiber-to-the-home (FTTH) applications. The concept of wavelength division multiplexing is schematically depicted in figure 1.2.

A fiber-optic telecommunication link requires at the transmitter side an array of laser diodes, each emitting light at a different wavelength and modulated by a different data signal, and a multiplexing circuit to bundle the different beams into one optical fiber. At the receiver side, a demultiplexer circuit is needed to unravel the optical signals and send them to the corresponding photodetector. Intermediate optical amplifiers in the link are required to restore the signal levels, due to attenuation in the optical fiber.

Besides for telecommunication, fiber-optic links can be used for short-distance bidirectional data communication. This requires a transceiver circuit (containing both a transmitter and receiver) at both sides of the link. As the required volumes are much higher in this case, the cost per component is more crucial than in the case of telecommunication applications. This is definitely the case for the ongoing deployment of fiber-to-the-home (FTTH), where each subscriber requires a transceiver at home to receive the downstream optical signal for data, voice and television and to transmit an upstream optical signal.

1.1.3 Photonic integrated circuits

Just like in electronics, the photonic components required for an optical link can be integrated on a single chip resulting in a photonic integrated circuit (PIC). Like in electronics, this integration will improve performance, yield and compactness, and lower the cost of the fabricated devices due to the economy of scale. In photonics there is an extra reason to integrate as many functions as possible on a chip: coupling light from one component to another typically requires accurate and therefore time consuming and expensive mechanical alignment. When integrating optical functions this alignment is largely taken care of by means of a collective lithography process for all photonic integrated circuits on a wafer.

In such a PIC, the routing of light is performed by integrated optical waveguides. Waveguides are structures that can confine light within a certain area and transport it over a given distance. In almost all situations, this confinement is achieved by index guiding, where light is trapped in a core of material with a higher refractive index than the surrounding material. Light is bundled in a spot around the center, or a mode. Most optical fibers used in telecommunication, the basic example of non-integrated optical waveguides, support only one guided mode.

Photonic integrated circuits can be fabricated in a variety of material systems. The most popular and mature one is silica-on-silicon, where light transport takes place in a glass layer on top of a silicon substrate. Alternative materials are III-V semiconductors like InP/InGaAsP or GaAs/AlGaAs, which make it easier to integrate active optical functions (light emission, detection, modulation) onto the chip. As will be discussed later, silicon can also be used as a waveguide material. As silicon has an indirect band gap, active opto-electronic components at

telecommunication wavelengths (especially light emitting devices and optical amplifiers) are hard to achieve. Besides semiconductors, many other types of materials can be used as well. Polymers or SiON (silicon oxynitride) for example are low-cost materials for the fabrication of photonic integrated circuits.

An important issue however is the integration density that can be achieved in a particular material system. This is predominantly related to the minimum achievable waveguide bend radius to avoid substantial bending losses and the minimal pitch of the waveguides to avoid substantial coupling between waveguides. This is related to the achievable refractive index contrast between waveguide core and cladding. A high refractive index contrast will lead to a higher degree of integration. As semiconductors typically have a refractive index around 3, the III-V semiconductors and silicon allow a higher integration density than silica-on-silicon, SiON and polymer waveguide circuits (with a refractive index in the range of 1.5-2).

1.2 Optical interconnects and photonics

1.2.1 Introduction

While fiber-optic communication has deeply penetrated the long-haul and metro communication networks connecting points more than 100m apart, optical interconnections are starting to be introduced on shorter interconnection distances, for example to connect different racks in a system (1m to 100m), to connect different boards on a back plane (50cm to 100cm) or to interconnect different chips on a board (1cm to 50cm). With decreasing distances, also the volumes of required interconnects increases, making cost a very important issue. An even further extending application of optical interconnects is the connection of different points on a chip (intra-chip interconnect), with distances ranging from 100μm to 1cm. This drive to further decrease the distances at which to implement optical interconnects instead of copper interconnections, will be discussed in the following sections.

1.2.2 CMOS: Complementary Metal Oxide Semiconductor

CMOS has become the predominant technology in digital electronic integrated circuits. This is essentially because area occupation, operating speed, energy efficiency and manufacturing costs have benefited and

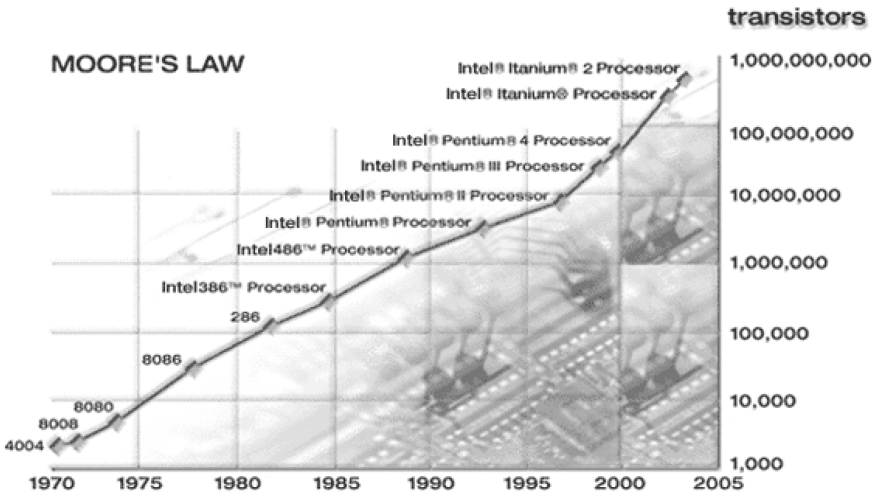


Figure 1.3: Moore's law in electronics (from [3])

continue to benefit from the geometric downsizing that comes with every new generation of semiconductor manufacturing processes. The speed of a transistor fabricated in a silicon circuit keeps increasing by shrinking its device dimensions. Besides the increase in speed, the amount of transistors steadily increases in modern electronic integrated circuits. This is dictated by Moore's law [2], which predicts a doubling of the number of transistors on integrated circuits (a rough measure of computer processing power) every 18 months. While first stated in 1965, the law has largely held the test of time, as is shown in figure 1.3. Nowadays, processors have reached a transistor count of over 1 billion per electronic circuit. As this trend of increasing circuit complexity and speed continues, the data density (in Gbps/cm^2) that has to be transported between either two points on a chip, two different chips, two different boards or two different racks is steadily increasing.

1.2.3 Limits to electrical interconnects

In [4] it was found that there is a limit to the total number of bits per second, B, of information that can flow in a digital electrical interconnection, that is set only by the ratio of the length l of the interconnection to the total cross-sectional dimension $\sqrt{A}$ of the interconnect wiring, the "aspect ratio" of the interconnection. This limit is largely independent

of the details of the design of the electrical lines. The limit is approximately $B \approx B_0 \frac{A}{l^2}$ bits/s, with $B_0 \approx 10^{15}$ bits/s for high-performance strip lines and cables, 10^{16} for small on-chip lines, and 10^{17} to 10^{18} for equalized lines (a relatively simple passive network can compensate for the frequency dependence of the loss in the cable over some frequency range, at the expense of attenuation of the overall signal).

As with increasing technology node (and thereby decreasing device dimensions), the pitch between the wires interconnecting two points on a chip or interconnecting two different chips decreases, the available bandwidth density of the interconnect decreases as the size of the systems (or the interconnection length l) stays approximately the same. The required data density to be transmitted increases however, as the transistors become faster. Therefore, at a certain point, the electrical interconnections can no longer deliver the amount of bandwidth required by the transistors and this happens first at the long interconnection distances.

Intra-chip interconnects are expected to run into this bandwidth density limit soon, especially on the global interconnection level, where the interconnection distances are the longest (in the order of 1cm). This inferior performance scaling of intra-chip global interconnects with respect to overall technology progression threatens to saturate Moore's law (see figure 1.3). Global interconnects suffer disproportionately from higher RC delay, power dissipation, and clock skew, and are a primary source of noise due to high cross-capacitance. Reverse scaling has successfully contained these issues thus far, but will not suffice in the future. This problem can be alleviated by the use of repeatered interconnections as shown in figure 1.4, where $(N-1)$ repeaters (buffers) are inserted to increase the bandwidth of the interconnection by a factor N^2. However, these repeaters impose a significant consumption of silicon real estate, are power hungry and complicate the routing of the other interconnections, as always a via connection has to be made through the whole metal stack. Moreover, the signal delay becomes more important and the effective signal propagation velocity is limited to a relatively small fraction of the velocity of light.

Besides the bandwidth issues discussed above, electrical interconnects have additional drawbacks. Electromagnetic wave phenomena such as the need for impedance matching and the occurrence of crosstalk between adjacent lines make the design of these electrical interconnections difficult and dependent on operation frequency.

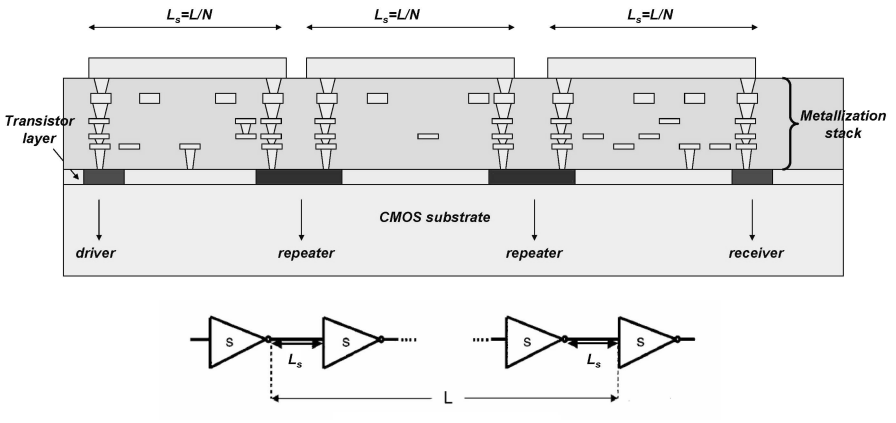


Figure 1.4: On-chip electrical interconnects with repeaters - a cross-section of the CMOS metallization stack and transistor layer

1.2.4 Optical interconnects

Optical interconnects do not have such an aspect ratio limit as discussed in the previous section, because loss in optical media is essentially independent of the modulation bit rate. Most of the difficulties of impedance matching and wave reflections can be avoided in optics (anti-reflection coatings). Crosstalk between adjacent fibers is negligible and in integrated waveguides it can be kept low by taking a sufficiently large waveguide pitch (which still provides a much higher bandwidth density than electrical wires).

Therefore, the use of integrated optical waveguides can aid in alleviating the bandwidth issues in on-chip interconnects, especially on the global interconnection level, while fiber interconnections between chips and at larger interconnection length can moderate the bandwidth issues there. For intra-chip interconnects, the optical approach has many variants, the simplest perhaps having emitters off-chip, based on free space propagation and detectors in top layers on-chip. Progressively more complex options culminate in monolithic emitters, waveguides and detectors.

1.2.5 Comparison between optical and electrical on-chip interconnects

In order to evaluate the feasibility of an on-chip optical interconnect, the performance and requirements of this optical interconnect should

be compared to the electrical interconnect case. In [5] this analysis was made. In particular, the performance and cost of optical interconnects and copper interconnects for clock distribution and intra-chip global signaling were compared. The analysis did not reveal significant advantages for on-chip clock distribution using optical interconnects as compared to conventional electrical clock distribution. For signaling, it was found that optical interconnects, in conjunction with wavelength division multiplexing, can potentially provide a low latency-high bandwidth option. In this analysis, an off-chip continuous wave laser diode is used as the optical power supply. On-chip optical modulators and on-chip photodetectors modulate and receive the data signals respectively. For clocking, an off-chip mode-locked laser is used as the clocking source, which is distributed through an H-tree optical network with a photodetector at the end of every branch.

For clocking, it was observed that, although optical interconnects show a better performance than scaled copper interconnects in terms of skew (being the difference in time arrival of the clock signal at the various points in the circuit) and jitter (being the variation of the interval between two successive clock pulses), they do not offer improvements with respect to non-scaled copper interconnects, which are an option with lower cost and less technological risk. For signaling, different metrics have to be used. Especially the delay and bandwidth density are important issues. Concerning delay, high speeds of signal propagation are obtained in the optical waveguides, but there is significant time overhead in the electrical-optical-electrical conversion. For long interconnects, where most of the latency is associated with the waveguide propagation, optical interconnects can be advantageous. This is compared to the scaled copper interconnects however, as non-scaled copper interconnects show a comparable delay-to-clock-cycle ratio as optical interconnects, for a typical global interconnect length of $1cm$. However, besides delay, also bandwidth density is an important metric. This is determined by the pitch of the optical waveguides and electrical lines. Comparing non-scaled copper interconnects, optical interconnects based on a single wavelength and based on a wavelength division multiplexing optical technology, the WDM technique shows a superior bandwidth density compared to non-scaled copper interconnects. Moreover, to meet the wire demand for non-scaled copper interconnects, additional metal layers would be required, which will add cost to the final product.

1.3 Sensing and photonics

Besides for use in optical interconnects and telecommunication, photonic integrated circuits can be used for sensing applications [6]. By changing an environmental parameter (for example strain of the chip or the attachment of bio-molecules to the waveguide walls [7]), the properties of light propagation in the waveguide change and can therefore be detected. High sensitivity can be obtained. In order to interrogate the optical sensor, light has to be coupled into the sensor element and detected. Light generating and detecting components could be located off-chip and interconnected to the photonic integrated circuit using optical fiber, or, in a more advanced integration, they could be located on chip together with the passive sensor element.

For analyzing the spectral properties of an optical beam (for example carrying the characteristic signature of the absorption spectrum of a gas through which the beam propagates), an integrated spectrometer can be used. In these devices, wavelengths are spatially separated to be detected by an array of photodetectors, which are integrated on the circuit.

1.4 Vision, lighting, displays and printing

While in the previous sections the applications of photonic integrated circuits were discussed, the photonics research area is much broader. For example, the fabrication of infrared cameras using III-V semiconductors or LADAR imaging systems (laser radar systems, which use time of flight measurements to construct three-dimensional images of an object [8]), the fabrication of printer heads based on LED arrays [9] or the use of LED matrices for micro display [10] or lighting applications [11], are only a grasp of typical research areas in photonics. These applications all have in common that the optical functionality needs to be integrated with electronics.

1.5 Heterogeneous integration

1.5.1 Introduction

In the previous sections, various areas of research in the field of photonics were discussed. The aspect of integration is predominant in this

field. This implies the need for the integration of both active and passive optical components on a photonic integrated circuit or the integration of optical components on an electronic integrated circuit. The development of a heterogeneous integration process in this work, can tackle these integration issues. Moreover, the developed process allows an increased flexibility in the processing of optical components and allows the fabrication of new types of optical components, which were previously hard to achieve.

1.5.2 Heterogeneous integration for optical systems-on-a-chip

Photonic Materials - heterogeneous integration

As was discussed in section 1.1.3, various material systems can be used to fabricate photonic integrated circuits. They differ in the density of integration that can be achieved, the fabrication process, the ability to combine active and passive functionality and the cost of the components. We will argue in the subsequent section that silicon-on-insulator is a promising platform for integrated optical circuits. While this material system has significant advantages in terms of fabrication, integration density and cost, the fabrication of active opto-electronic devices (light emission, amplification and detection) at telecom wavelengths using electrically contacted devices is difficult. On the other hand, the InP/InGaAsP material system is better suited to integrate active and passive optical functionality at telecom wavelengths, but has some disadvantages in terms of fabrication, cost and achievable integration density. Therefore, the heterogeneous integration of silicon-on-insulator (SOI) passive waveguide circuits and InP/InGaAsP active opto-electronic components is proposed, to combine the advantages of both material systems.

Silicon-on-insulator

Large core SOI versus SOI photonic wire technology A silicon-on-insulator (SOI) layer stack consists of a silicon waveguide layer on top of a buried SiO_2 layer, fabricated on a silicon substrate. Two types of silicon-on-insulator waveguides are used.

Large core rib SOI waveguides consist of a silicon waveguide layer, which is multiple material wavelengths thick. Lateral confinement is obtained by defining a rib waveguide geometry. By carefully adjusting the etch depth and the width of the waveguide, single-mode operation

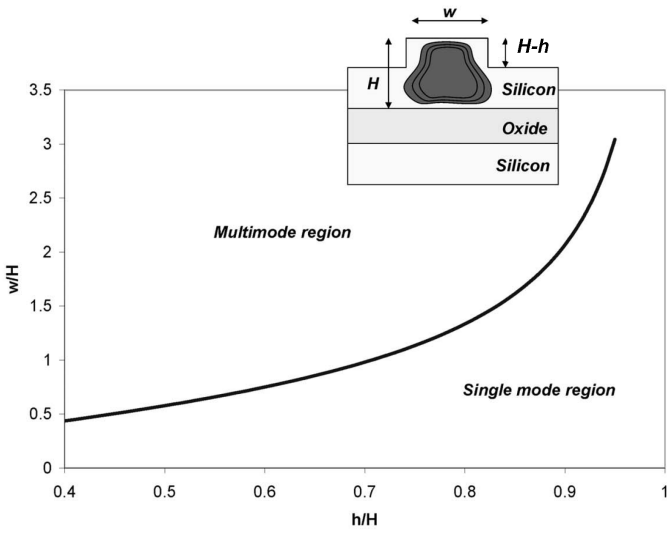


Figure 1.5: Design criteria for the monomodal operation of a rib SOI waveguide

can be achieved, as shown in figure 1.5 [12]. This requires shallow etching of the waveguides, reducing the lateral refractive index contrast. While the increase of the minimal waveguide radius due to this low refractive index contrast, can be countered by the use of total internal reflection mirrors, the pitch of the waveguides remains large. The general understanding is that this waveguide system allows to fabricate optical circuits with low polarization dependence, low propagation loss and a low fiber insertion loss.

In SOI photonic wire technology, a silicon waveguide layer thickness on the order of half a material wavelength is used and the lateral confinement is achieved by completely etching through the silicon waveguide layer. In this way, a large omni-directional index contrast is achieved ($n_{Si} = 3.45$,$n_{SiO_2} = 1.45$), which allows large density integration of optical functions. The criterion for monomodal operation of an SOI photonic wire is depicted in figure 1.6, for a 220nm silicon waveguide layer thickness. The effective index of the lowest order modes are plotted as a function of waveguide width. In order to avoid radiation into the oxide buffer layer, n_{eff} should be higher than n_{SiO_2}. Waveguide widths smaller than 500nm are necessary to obtain single-mode operation. Due to the large discrepancy in mode size between photonic wire waveguides and optical fibers, fiber coupling structures have to

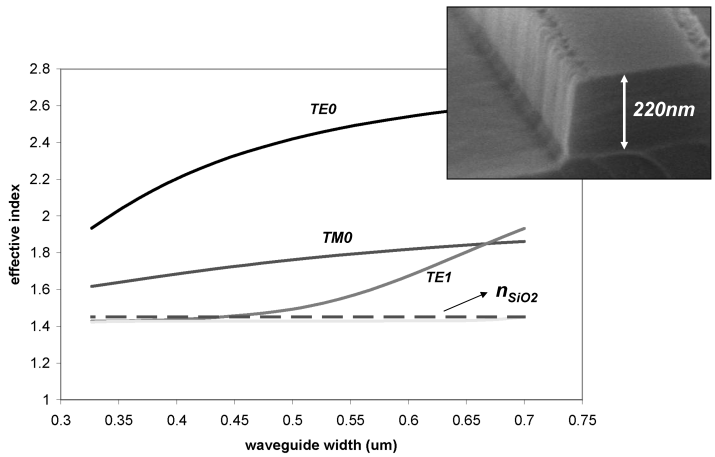


Figure 1.6: Modal effective index of an SOI wire (220nm silicon layer thickness) as a function of the waveguide width (λ=1.55μm)

be designed that accommodate this difference. This will be discussed in section 4.6.

Fabrication of silicon-on-insulator waveguides The advantage of using silicon-on-insulator for fabricating integrated optical devices (using large core waveguides or photonic wire waveguides) is that one can take advantage of the enormous CMOS infrastructure and processing capacity available. Moreover, the available lithography tools meet the typical requirements of feature sizes above 100nm. The industry standard silicon manufacturing processes enable integration and can bring volume economics to optics [13].

Density of integration The density of integration that can be achieved using silicon-on-insulator photonic wire technology is enormous. For example, in literature 0.004dB excess loss was measured on a 90 degree bend with a radius of 5μm, while a bend radius of 1μm resulted only in a loss of 0.09dB per 90 degrees for SOI photonic wires with 220nm silicon waveguide layer thickness [14]. The waveguide pitch that can be obtained is shown in figure 1.7, for various waveguide dimensions (the silicon waveguide layer thickness h and the waveguide width). The achievable pitch is defined as the minimum pitch required to keep the crosstalk between waveguides below -20dB for a pair of 1cm long

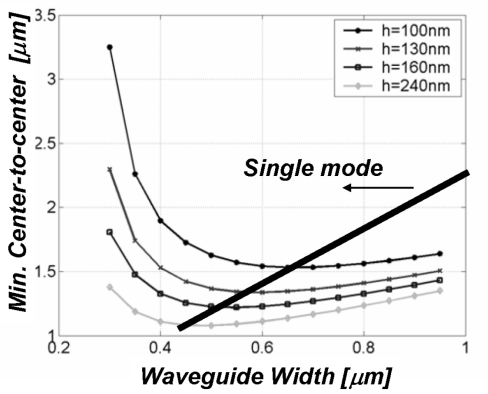


Figure 1.7: SOI photonic wire pitch as a function of the waveguide dimensions

waveguides. To further increase the density of integration, waveguide crossings can be used to make more complex routing possible.

Silicon photonics

Integration on a silicon platform As discussed above, the integration of optical functions has several advantages in terms of cost (especially due to the reduced amount of fiber interfaces) and performance. The integration of the optical functions on a silicon platform gives the additional advantage of using the in-depth developed CMOS technology. In general, different types of optical components need to be integrated on the photonic integrated circuit. Besides passive functions (wavelength selective components, waveguiding, power splitting, fiber couplers), the integration of active optical functions on the silicon platform is an active area of research. This implies the integration of silicon-based modulators, SiGe photodetectors and silicon light sources. In order to add intelligence to the system, besides the integration of passive and active optical functions, also electronics can be integrated. In the next paragraphs we will briefly outline the state-of-the-art in silicon photonics.

Silicon waveguide devices There is a broad research interest in the development of passive optical devices in the silicon-on-insulator material system. Both the optimization of the optical waveguide fabrication process and the fabrication of wavelength selective components

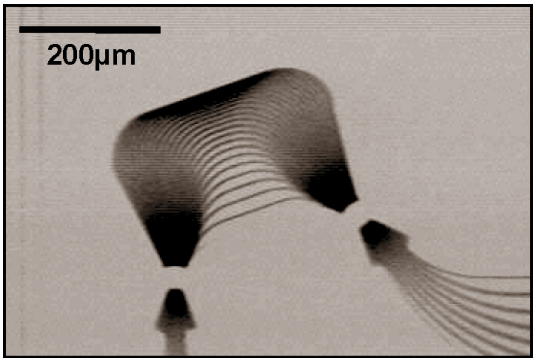


Figure 1.8: Image of a compact arrayed waveguide grating fabricated in SOI, performing (de)multiplexing operation (from [16])

like ring resonators [15], arrayed waveguide gratings [16, 17] and Mach-Zehnder interferometers [14] are under investigation. This yields very compact and high-performance optical devices, like the arrayed waveguide grating shown in figure 1.8, being the basic component for multiplexing in WDM communication systems. Besides these wavelength selective components, also the interfacing of the photonic integrated circuit with the outside world is an important area of research. This will be discussed in more detail in section 4.6.

Silicon modulators Besides the passive optical components, also SOI-based optical modulators were developed. In [18], a high speed silicon Mach-Zehnder modulator was developed with an intrinsic bandwidth of 10GHz. The device is based on the free carrier plasma dispersion effect. The phase shifting elements of the Mach-Zehnder interferometer are metal-oxide-semiconductor (MOS) capacitors, embedded in a silicon rib waveguide. An applied voltage induces an accumulation of charge near the gate dielectric of the capacitor, which changes the optical phase of light passing through the waveguide. As the MOS capacitors only operate in accumulation, the device bandwidth is not limited by carrier recombination in silicon.

In [19], a ring-resonator-based modulator was developed. The modulator consists of a ring resonator coupled to a single waveguide. The device is based on the tuning of the resonance wavelength of the ring resonator by injecting electrons and holes, using a pin-junction embedded in the ring resonator. Although pin-devices based on the injection of carriers are considered to be relatively slow compared to MOS ca-

pacitors, the resonating nature of the modulator removes this limitation: as the input-output transmission versus voltage resembles a step like function (compared to a sinusoidal function in the case of a Mach-Zehnder modulator), a higher modulation voltage can be used in order to reach an optical steady-state far before the electrical steady-state is reached. With this type of devices, a bit rate higher than 10Gbit/s was obtained [20]. Also, devices based on carrier depletion instead of carrier injection, which provide higher obtainable modulation rates, are being developed [21]. In [22], a SiGe/Si quantum well optical modulator was designed. The device is based on the variation of the (complex) refractive index, due to the change in hole density in the SiGe wells, induced by applying a reverse bias on a pin-diode. The speed is determined by the time necessary for holes to leave the wells by thermionic emission, which is about 10 ps for a 10nm thick well.

As the silicon crystal structure has inversion symmetry, no linear electro-optic effect exists in silicon. This makes very high speed and low-power optical modulation in silicon challenging. Recently, it was found however that breaking the symmetry of the crystal by depositing a straining layer on top of it, creates this linear electro-optic effect [23]. The effect can be enhanced by using a low group velocity waveguide mode in a photonic crystal waveguide. This development opens the way to new types of optical modulators in silicon-on-insulator with the promise of very high speed operation.

Silicon photodetectors As silicon has an (indirect) band gap of about 1.12eV, only light with a wavelength shorter than 1.1μm can efficiently be detected. The detection of light at telecommunication wavelengths requires the integration of different materials on the silicon platform. A CMOS compatible material that can be used for this purpose is germanium. As will be discussed in more detail in section 7.3, there are three main approaches that have been proposed to integrate germanium, each based on a different type of active layer: $Si_{1-x}Ge_x$/Si heterostructures, SiGe or Ge quantum dots on silicon layers and the use of pure Ge. In [24], interdigitated metal-germanium on silicon-metal photodetectors for operation at 1300nm and 1550nm were fabricated. Bandwidths of 35GHz were reported. In [25], the integration of germanium photodetectors with silicon waveguides was reported. A fully CMOS processed Ge pin-photodetector, integrated with a silicon waveguide on an SOI platform, showing a high responsivity of 1.0 A/W at a wavelength of 1520nm and a bandwidth of over 4.5GHz, was demonstrated.

In [26], Ge-on-silicon vertical incidence photodiodes with 39GHz bandwidth were reported.

An alternative approach is to use micro-structured silicon obtained by laser irradiation in an SF_6 atmosphere. By doing this, still a strong photoresponse was obtained at wavelengths longer than 1.1μm. A responsivity of 0.02A/W at 1.55μm was obtained [27]. Recently, the use of Si^+-implanted SOI waveguides for photodetection at telecom wavelengths was proposed [28].

Silicon light sources: silicon LED and silicon laser Silicon is an indirect band gap material. Therefore, light emission is a phonon-mediated process with low probability (radiative recombination lifetime in the milliseconds range). In standard bulk silicon, the competitive non-radiative recombination rate is much higher than the radiative one and most of the excited electron-hole pairs recombine non-radiatively. This yields very low internal quantum efficiency for bulk silicon luminescence.

Several approaches have been proposed in literature to tackle the problem of light emission in silicon. In [29], high-purity silicon was used to reduce the non-radiative recombination rate. Additional measures were taken in order to increase the external efficiency of the light emitting diodes. The surface of the silicon was texturized with inverted pyramids to increase the extraction efficiency (with an additional anti-reflection coating on top), while at the backside of the structure, a metal mirror was applied. The doping levels were kept low in order to avoid substantial free carrier absorption. Surfaces were passivated with high quality thermal oxide to reduce surface recombination. These forward biased high-performance solar cells, made from ultra-pure silicon with a carrier lifetime of 1ms, showed silicon light-emitting diode power conversion efficiencies of over 1 percent. While interesting from a fundamental point of view, the direct modulation speed of the device is limited by the long lifetime of the excited carriers.

In [30], a reduction of the non-radiative channels was achieved by exploiting the strain produced by localized dislocation loops, formed by implantation of boron, to form energy barriers for carrier diffusion. This spatial confinement of the charge carriers enhances radiative decay, by localizing them in defect free regions. Free carriers injected through the top electrode are not able to diffuse away and are constrained to recombine in the near junction region. An external quan-

tum efficiency of 10^{-3} was reported without additional measures to improve the extraction efficiency.

In [31], porous silicon was used to spatially confine electrons and holes in silicon crystallites. An external quantum efficiency larger than 1 percent was obtained from a 1μm thick porous silicon layer, which was electrochemically oxidized. Electrons were injected in the crystallites through an n-type Indium-Tin-Oxide (ITO) contact. Since high electric fields are set across the silicon crystallites, holes may be generated in porous silicon by tunneling of electrons out of the valence band into the conduction band of neighboring crystallites or into the substrate conduction band. As the electroluminescence time response is around 30μs, due to the large capacity of the oxidized porous silicon, the applicability of this type of light source in optical communication is limited.

In [32], field-effect electroluminescence in silicon nano-crystals was observed. While photoluminescence in silicon nano-crystals was studied before, no good electrical injection scheme was available due to the SiO_2 host matrix in which the nano-crystals were contained. In [32] Fowler-Nordheim tunneling of electrons and holes through the SiO_2 host matrix was used. Under appropriate bias conditions, the silicon nano-crystals in the gate oxide of a transistor could be supplied with electrons from an inversion layer or with holes from the channel in accumulation. As the charge injection in neutral nano-crystals requires about 100μs, again applications in optical communication are limited.

Besides the use of silicon crystallites to spatially confine electrons and holes, superlattices of silicon and SiO_2 can be used as well. The photoluminescence of visible light in these superlattices was reported in [33]. It was shown that the light emission can be explained in terms of quantum confinement of electrons in the silicon layers.

While the devices discussed above showed electroluminescence or photoluminescence around the band gap wavelength of silicon (1.1μm) or at shorter wavelengths due to the quantum confinement, light emission at telecommunication wavelengths can be obtained by incorporating erbium impurities in the silicon matrix [34] or by using SiGe, Ge [35, 36] or $FeSi_2$ [37] for light emission.

The use of impurities relaxes the momentum conservation rule as the presence of an impurity leads to a spatial localization of an electron and to a delocalization of the wave function. This spreading partially fulfills momentum matching between the conduction band and valence band edges in silicon. Rare-earth ions, specifically erbium, have played

an important role in the development of optical communication technology. Erbium has an incomplete 4f electronic shell that is shielded from the outer world by closed 5s and 5p shells. As a result, rather sharp optical intra-4f transitions can be achieved from erbium-doped materials, while the energy of this transition (0.8eV or a wavelength of 1.55μm) is relatively independent of host material and temperature. In [34], erbium implantation in a silicon host substrate was used to obtain electroluminescence at 1.55μm. A quantum efficiency of 0.01 percent was obtained.

The performance of SiGe light emitting diodes is limited by non-radiative recombination, as in the case of silicon. In [35], quantum efficiencies of $10^{-5} - 10^{-4}$ of strained SiGe light emitting diodes were reported. In [36], electroluminescence from germanium quantum dots in a silicon matrix was measured with a power conversion efficiency of 0.14 percent.

In [37], $FeSi_2$ precipitates implanted in a silicon p-n junction near the depletion region of the diode, were used to obtain light emission at 1.54μm. $FeSi_2$ is a direct band gap material, therefore providing an efficient and fast radiative recombination route. Electroluminescence was measured and a quantum efficiency of 0.1 percent was reported, which is rather low, but could be optimized by improving the device design and material quality.

In order to achieve lasing through electrical injection (and therefore gain) in a silicon-based device, the same problem of the indirect band gap of silicon needs to be tackled. Moreover, efficient Auger recombination processes ($C = 10^{-30} cm^6/s$) and free carrier absorption processes ($\alpha \approx 2.4 \times 10^{-18} N_{fc}$) can prevent reaching population inversion or nett gain.

The same methods to alter the light emission properties of silicon for the fabrication of light emitting diodes can be used to achieve a silicon injection laser diode.

In [38], stimulated emission in a nano-structured silicon p-n junction using current injection was observed. As a limit to efficient light generation in silicon is the short non-radiative lifetime, the idea was to avoid carrier diffusion and spatially localize free carriers in a small device region, where non-radiative recombination centers can be easily saturated. Carrier localization was achieved by doping using a mixture of a spin-on dopant and silica nano-particles, which locally mask the diffusion of boron in the silicon. A change from a broad emission spectrum associated with band-to-band emission below threshold,

to sharp peaks due to stimulated emission above threshold at room temperature, is observed. A threshold current density of 1.05kA/cm^2 for 1mm long devices is obtained and 0.013 percent external quantum efficiency was measured, which is rather low. The measured laser peak is attributed to two-phonon mediated indirect transitions and lies around 1.2μm. While this is the first demonstration of a silicon injection laser, the low external quantum efficiency and the emission wavelength, which is not compatible with telecommunication, are the major drawbacks of this device. Moreover, since the publication of these results, to our knowledge, no further improvement or application of the laser structure has been reported.

In [39], optical gain and stimulated emission was observed in nano-patterned crystalline silicon. The below band gap 1278nm emission peak is attributed to A-centre mediated phononless direct recombination between trapped electrons and free holes. These so called A-centre defects are attributed to silicon vacancies in the nano-patterned silicon due to the processing of the nano-holes, to form so called emissive structural deformation zones. The nano-patterned layer was optically pumped and lasing was observed up to 80K. The external efficiency is in the order of $10^{-6} - 10^{-5}$. Due to the long electronic life time in such defects and the low absorption of the silicon in the sub band gap wavelength region, lasing could be achieved. While this is also clear evidence for the occurrence of lasing action in silicon, the low temperatures required, the low external efficiency and the fact that the device is optically pumped, makes this type of device not readily applicable for telecommunication applications.

In [40], optical gain was observed in silicon nano-crystals. The crystals were 3nm in size and dispersed in an SiO_2 host matrix. Gain was observed around wavelengths of 800nm and is attributed to the radiative emission from a silicon/oxide interface state in the boundary layer between the silicon nano-particle and the SiO_2 host matrix. Radiative lifetimes in the microsecond range were measured. Although gain was observed, no lasing action was reported.

In the previous approaches for achieving lasing or optical gain in silicon, the spectral range for light emission was located around 1.2μm or at shorter wavelengths for silicon nano-crystals. An approach for achieving lasing at 1.55μm by incorporating erbium impurities in silicon nano-crystals is discussed in [41]. The main problem for achieving lasing with erbium impurities in pure silicon is the back transfer of energy from the erbium ions to the silicon host. This is due to a res-

onant level, which appears in the silicon band gap due to the erbium doping and which couples with the erbium levels. This back transfer can be reduced by increasing the band gap of the host such that the resonance is lost, thereby leading to the use of silicon nano-crystals. It turns out that the silicon nano-crystals are very efficient sensitizers of the erbium luminescence. Electron-hole pairs that are created in the silicon recombine and excite the erbium, which then radiatively recombines (when the energy back transfer is decreased). Moreover, the erbium can be placed in the SiO_2 host matrix, which is their chemically most favorable environment. In [42], an internal gain of 7dB/cm in an erbium-doped waveguide amplifier (EDWA) has been measured. This opens the way to a silicon laser at 1.55μm. Optical pumping was used in the experiments however. In this respect, it is worth noting that toroidal microcavities formed in erbium-doped silica have demonstrated optically pumped lasing at 1.54μm [43]. An alternative approach based on silicon slotted waveguides filled with erbium-doped SiO_2 has been proposed in [44]. Current injection in the silicon nano-crystals through the dielectric matrix remains an area of investigation. In [45] current injection was achieved, based on tunneling between silicon nano-crystals and Fowler-Nordheim tunneling. The obtained current density ($0.2A/cm^2$) at high voltage (50V) is very low however. The same order of magnitude was obtained in [46].

A different type of silicon laser that was reported in literature is the silicon Raman laser [47]. The stimulated Raman scattering effect refers to a non-linear optical effect in which a laser pump photon induces the creation of a phonon (lattice vibration) and a photon of lower energy. The emitted photons make up the signal beam. While already demonstrated in SiO_2, the problem of stimulated Raman scattering in silicon is the creation of electron-hole pairs by an unwanted non-linear optical side effect, namely two-photon absorption. These carriers have a relatively long lifetime and absorb the pump and signal light through free carrier absorption. This problem can be solved by adding a lateral reverse biased pin-junction, which reduces the free carrier lifetime by sweeping the carriers away from the waveguide rib area. Using this approach, continuous wave Raman lasing in a silicon waveguide structure was observed [47, 48]. Of course, the use of a non-linear optics phenomenon means that optical pumping will always be required.

Broadband optical gain in a silicon waveguide through four-wave mixing (FWM) is reported in [49]. In four-wave mixing, two pump photons with energy $h\nu_{pump}$ are converted to a signal and idler photon such

that $2h\nu_{pump} = h\nu_{signal} + h\nu_{idler}$, which can lead to amplification of the signal wave. The phase mismatch of the pump, signal and idler determines the optical bandwidth over which gain can be observed. While optical gain due to the Raman effect only has an intrinsic bandwidth of 1nm, a 28nm bandwidth FWM-gain was demonstrated. As this mechanism again relies on the use of a non-linear optics phenomenon, optical pumping will always be required.

Integration of CMOS and optics Besides the integration of optical functions, intelligence can be integrated onto the silicon-on-insulator platform by incorporating electronics besides the optical circuits. Laser diode drivers, transimpedance amplifiers and modulator drivers can be integrated close to the optical component to reduce device parasitics. Besides this type of essential components, also digital logic can be implemented, for example to tune an optical filter characteristic (thermo-optic tuning or tuning by carrier injection or depletion) or an electronic decision circuit for fiber optic communication. An example of monolithic integration of optical and electronic functions was reported in [21]. The choice remains wether the CMOS is integrated in the same layer as the optical functions (monolithic integration) or a hybrid approach is used in which the electronics is flip-chipped onto the photonic carrier (or vice versa).

III-V semiconductors

III-V material systems In opto-electronics, III-V semiconductors are predominantly used due to their direct band gap, which enables efficient light generation. For optical communication purposes, mostly the InP/InGaAsP material system (emission wavelengths around 1300nm and 1550nm) and GaAs/AlGaAs (emission wavelengths around 850nm and 980nm) are used. Besides these two basic material systems, a whole myriad of other alloys are used or are under development for other wavelength ranges or for better performance. As the main focus is on telecommunication applications, the fabrication of photonic integrated circuits in the InP/InGaAsP material system will be discussed.

InP/InGaAsP passive waveguides integrated with active devices Passive optical waveguides can be formed on an InP substrate by growing a lattice matched InGaAsP layer on top, which has a higher refractive index and lower band gap energy than the InP substrate. Although

the vertical index contrast is low, high lateral index contrast can be obtained by etching the waveguide through the waveguide core. The InP/InGaAsP material system naturally lends itself for integration of active and passive optical functions. Different strategies can be applied to achieve this. Multiple-core waveguide structures can contain both an active and a passive waveguide layer, vertically stacked. Coupling between both waveguide layers is typically achieved by adiabatic transformation of the waveguide mode [50] or by evanescent coupling [51]. Another option is to modify the properties of the InP/InGaAsP waveguide layer over the photonic integrated circuit using regrowth techniques [52], selective area growth [53] or quantum well intermixing [54]. This allows butt-coupling of active and passive waveguide structures, without significant reflection or loss at the interface. These techniques are outlined in figure 1.9. In the epitaxial regrowth technique, a planar active (passive) layer structure is grown, after which it is etched away again in the areas requiring a passive (active) layer structure. The required layer structure is then locally grown in the etched areas. In selective area growth, multi-quantum well layer structures are grown on a host substrate carrying a predefined mask layer. As the width of the mask opening determines the local growth rate, the thickness of the quantum well structures can be locally modified to allow both passive (higher growth rate) and active (lower growth rate) layer stacks. In the quantum well intermixing technique, an active multi-quantum well layer structure is grown, after which the quantum well structure is locally disordered, for example by ion implantation or photoabsorption induced disordering, which shifts the absorption spectrum of the structure.

While any optical function for telecommunication wavelengths can be achieved using monolithic integration in InP/InGaAsP and all state-of-the-art active devices are fabricated in this material system, the monolithic integration of active and passive optical functions in InP is an expensive technology. Further scaling of device size, which could reduce cost, is hampered by technological difficulties and the monolithic integration with electronics is not achievable.

Systems-on-chip

Heterogeneous integration From the discussion above, we can conclude that both the use of silicon as a photonic material and the use of InP/InGaAsP has its distinct advantages. While the use of silicon has

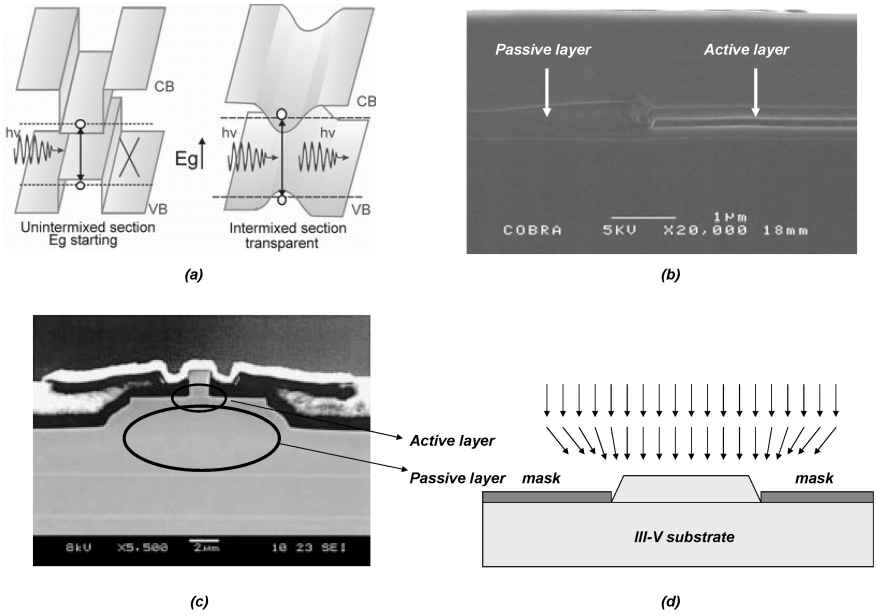


Figure 1.9: Active-passive integration in the InP/InGaAsP material system: quantum well intermixing [54] (a), regrowth [52] (b), multi-layer stacking [50] (c) and selective area growth [53] (d)

the advantage of the ability to use the existing and massive CMOS technology base and the ability of fabricating low-cost photonic integrated circuits, it lacks a good solution to the problem of light generation and amplification through electrical injection. As the state-of-the-art active opto-electronic components are fabricated in InP/InGaAsP, one can argue that it makes sense to heterogeneously integrate both material systems, to exploit the advantages of both. In order for this approach to be industrially viable, ideally all processing steps should be wafer-scale processing steps and the heterogenous integration process should not affect the yield of the final devices.

One question to be answered is wether one uses preprocessed III-V devices to be integrated onto the silicon host substrate. This would have the advantage of having the ability to test the InP/InGaAsP devices in advance, but requires an accurate alignment during integration, which is labor-intensive and therefore costly. Another question is wether to use full 2 to 4 inch InP wafers that are to be integrated or use separate dies. Using full wafers has the advantage of reducing the number of substrates that need to be integrated onto a full 8 inch silicon wafer, but can lead to inefficient use of the costly InP/InGaAsP material, as the InP/InGaAsP might only be needed in designated areas. This can be circumvented by using individual dies, which however increases the time and cost of integration, as this is a sequential process.

In this work, we propose the use of unprocessed InP/InGaAsP dies that are to be integrated on top of an SOI waveguide wafer or a CMOS wafer. The use of dies can decrease the consumption of the InP/InGaAsP material, while the fact that the dies are unprocessed makes the positioning of the dies tolerant to misalignment and can therefore be done quickly and cost effectively. In order to maintain high yield, the quality of the integration process and the post-integration processing of the InP/InGaAsP material needs to be assessed.

SOI waveguides and III-V devices The proposed integration scheme for heterogeneously integrating silicon-on-insulator waveguide devices and InP/InGaAsP opto-electronic devices, is schematically depicted in figure 1.10. In this integration scheme, individual unprocessed dies are rapidly pick and placed onto the silicon-on-insulator waveguide wafer with the epitaxial layer structure oriented downwards. After the collective removal of the InP substrate of the dies, only the InP/InGaAsP epitaxial layer structure remains attached to the SOI waveguide structure. This layer structure can then be processed on a wafer-scale and

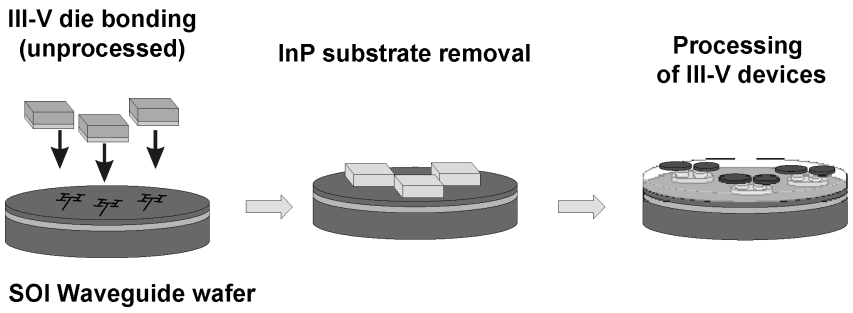


Figure 1.10: Heterogeneous integration of III-V devices and SOI waveguide circuits - process flow

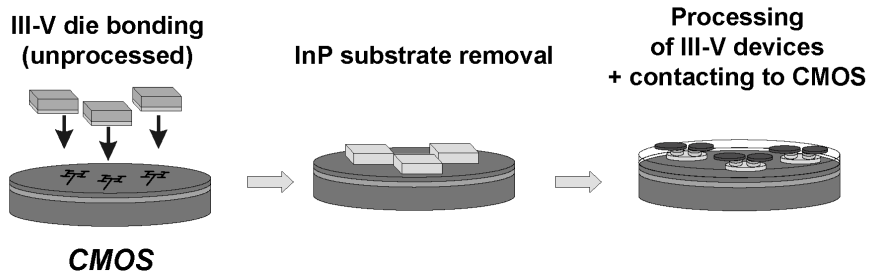


Figure 1.11: Heterogeneous integration of III-V devices and CMOS - process flow

devices can be fabricated, lithographically aligned to the underlying SOI substrate.

Various applications of this technology can emerge, for example for use in optical communication and integrated optical sensors.

CMOS and III-V devices Besides integration on top of an SOI waveguide circuit, the same type of integration process can also be used to integrate active opto-electronic components on top of CMOS circuits as shown in figure 1.11. The additional step in this processing scheme is the electrical contacting of the opto-electronic devices to the underlying electronic circuit.

Various applications of this technology can emerge, for example parallel optical interconnects between electronic integrated circuits, optical transceivers or high sensitivity infrared cameras to name a few.

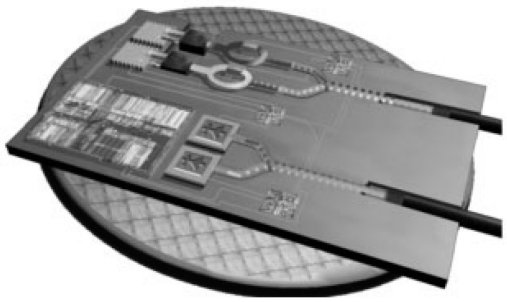


Figure 1.12: Artist impression of the integration of SOI waveguide circuits with III-V devices and CMOS electronic circuits (from [3])

SOI waveguides, III-V devices and CMOS The ultimate goal is to reach the integration of both electronic and optical functions in silicon, combined with the integration of InP/InGaAsP devices, fabricated on a wafer-scale, as shown in the artist impression in figure 1.12. Different ways of achieving this can be envisioned, ranging from the integration of silicon photonics and electronics in the same device layer and integrating the InP/InGaAsP on top, to fabricating a silicon waveguide layer on top of the CMOS circuit and integrating the opto-electronic components above this waveguide layer.

1.5.3 Layer transfer for double-sided processing

Besides for the fabrication of optical systems-on-a-chip, the InP/InGaAsP epitaxial layer transfer process proposed in the previous section can also be used to increase the device fabrication flexibility.

In standard planar waveguide technology, the epitaxial layer structures can only be accessed from the top as the carrier substrate prevents processing the bottom of the layer stack. By applying the layer transfer process as presented in the previous section to top side processed layer structures, thereby transferring the processed layer stack to a host substrate, the backside of the layer structure can be processed or optically accessed after removal of the original carrier substrate, as schematically depicted in figure 1.13. Applications of this double-sided processing will be discussed in section 6.2.2 and in chapter 8.

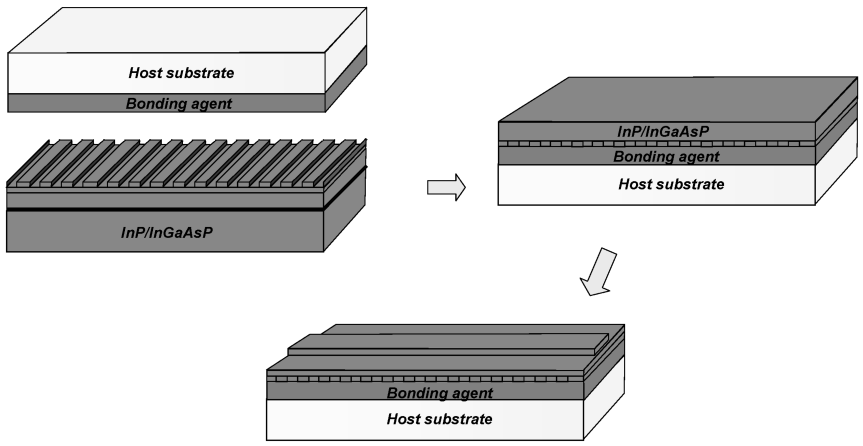
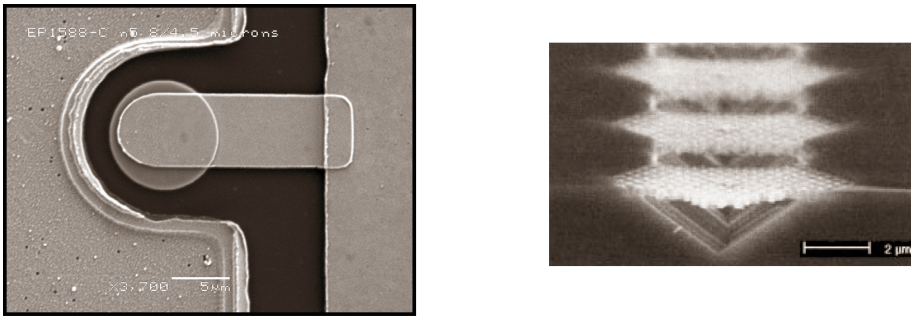


Figure 1.13: Double-sided processing scheme

1.5.4 Layer transfer for high vertical index contrast membranes

In the classical III-V material systems only a small refractive index difference can be achieved by varying the material composition. While this is not a problem for low density integrated optical circuits, this can become an issue for further scaling of the size of integrated optical components. Especially the radiation towards the substrate in sharp waveguide bends or in photonic crystal waveguides operating above the light line [55] can be a problem. Moreover, the low vertical index contrast reduces the vertical confinement of the light. This requires relatively thick epitaxial layer structures, which in their turn require deep etching to achieve high lateral confinement of the waveguide mode, which is technologically difficult to achieve, both in terms of aspect ratio (in photonic crystals for example) and in smoothness of the waveguide walls. This low refractive index contrast also restricts the confinement factor of a mode to a certain layer of interest, for example the quantum well gain layers in a laser stack.

Therefore, modified III-V material systems were proposed to achieve a high vertical index contrast. The oxidation of an AlAs layer in a GaAs/AlGaAs layer stack, to form a low refractive index AlO_x layer, was proposed in [56]. In [57], the selective underetching of InP/InGaAsP layers was used to achieve suspended InP/InGaAsP membranes surrounded by air. The layer transfer process proposed in this work can



(a) (b)

Figure 1.14: Small volume cavity lasers: microdisk lasers [58] and photonic crystal membrane lasers [59]

also be used for this purpose by transferring the epitaxial layer structures to a low refractive index host substrate and removing the InP substrate.

This way, new types of photonic components can be fabricated, such as theoretically lossless photonic crystal waveguides in III-V membrane and small volume cavity lasers, leading to ultra-low threshold operation. This will be briefly discussed in section 6.4. Examples of an InP/InGaAsP microdisk laser fabricated by the layer transfer process described above, is depicted in figure 1.14 [58], while the selective underetch to achieve suspended membranes is also shown [59].

1.6 Outline of the work

From this introductory chapter, it is clear that the heterogeneous integration of silicon and III-V materials, gives added value in several applications of photonics. The development of this integration process and demonstrations of integrated devices based on the developed technology, will be discussed in this work. The various technologies for heterogeneous integration will be outlined in chapter 2. In chapter 3, the development of an adhesive bonding technology will be discussed, which enables the integration of InP/InGaAsP membranes on top of an SOI waveguide circuit. In chapter 4, several optical coupling schemes will be discussed, allowing an efficient optical coupling between the SOI waveguide layer and the active opto-electronic component fabricated in the InP/InGaAsP membrane layer. As this problem is strongly

related to the coupling of light from an optical fiber to an SOI waveguide circuit, this problem will be assessed as well. In chapter 5, the patterning and etching of the passive SOI waveguide circuits and active opto-electronic devices will be discussed. Especially, the fabrication and performance of two types of developed fiber coupling structures will be presented. In chapter 6, various types of integrated light emitting devices based on the developed adhesive bonding technology will be presented, while in chapter 7, the same technology will be used for integrating InP/InGaAsP photodetectors on top of the SOI waveguide circuit. Finally, in chapter 8, the developed bonding technology will be applied in order to create new types of integrated optical devices, due to the ability of double-sided processing, compared to standard planar technology.

1.7 Conclusions

In this introductory chapter, we discussed the advantages of using silicon-on-insulator as a platform for photonic integrated circuits. The lack of a silicon injection laser emitting at telecommunication wavelengths however urges the need for the heterogeneous integration of InP/InGaAsP on the photonic integrated circuit. This allows the integration of passive silicon-on-insulator waveguide functions, silicon-on-insulator modulators, InP/InGaAsP laser diodes and InP/InGaAsP or germanium photodetectors. The integration of these optical functions with CMOS electronic circuits is within reach. Besides for the creation of complex optic/electronic systems-on-a-chip, the layer transfer technology can also be used to fabricate new types of optical components through the increased flexibility of double-sided processing and the creation of a high vertical refractive index contrast in the layer stack.

Chapter 2

Heterogeneous integration technology

You want a bond with me tonight?
Zita Swoon

The various heterogeneous integration technologies described in literature will be outlined in this chapter and these technologies will be compared, which will result in the choice of adhesive bonding for applications in integrated optics.

2.1 Introduction

In the previous chapter, the use of silicon-on-insulator as a passive waveguide platform was discussed. The advantages of SOI both from an optical point of view and from a fabrication point of view were outlined. It was stated that heterogeneous integration technology, defined as the technology enabling the integration of different material systems onto a single substrate, can increase the functionality of the photonic IC, by integrating active optical functions on the passive SOI platform. In this chapter we will elaborate on the different technologies available to achieve this.

2.2 Hybrid integration

In hybrid integration technology, optimized components (both electronic, passive optical and opto-electronic) are individually mounted

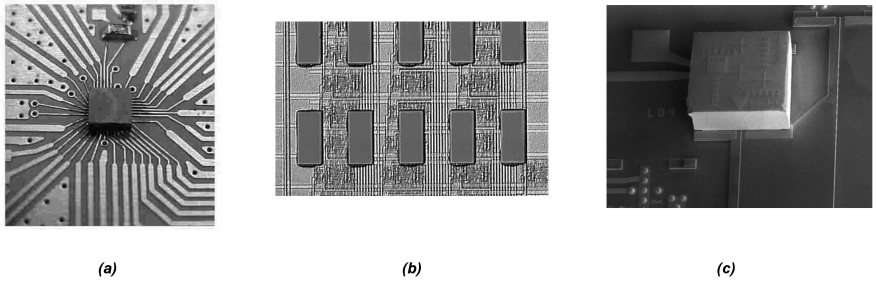


Figure 2.1: Flip-chip technology for hybrid integration: a CMOS die flip-chipped onto a PCB [61] (a), an opto-electronic die flip-chipped to CMOS [62] (b) and a laser diode flip-chipped onto an optical waveguide platform [60] (c)

on a common substrate. The process is also referred to as flip-chip bonding. This technology is often used to position finished electronic circuits onto a printed circuit board. Typically, gold or solder bumps are used to attach the dies to the substrate and at the same time provide an electrical contact. Although this technology was developed for micro-electronics, its use was extended to the integration of opto-electronic components onto a common substrate. An additional problem that needs to be assessed in the case of flip-chipping opto-electronic components, is the high precision alignment that is required, especially when coupled to single-mode integrated waveguides or single-mode optical fibers, for which typically sub 1μm alignment accuracy is needed. This leads to expensive and labor-intensive positioning techniques. Some solutions to this problem were suggested, mostly based on the surface tension in molten solder bumps, which automatically aligns both substrates with respect to each other. Other techniques are based on special mechanical alignment structures on the substrate and on the component that needs to be placed [60].

Three examples of the use of flip-chip technology are shown in figure 2.1. In (a) flip-chip technology was used to attach and electrically connect an electronic IC to a printed circuit board [61]. In (b) opto-electronic components were flip-chip bonded onto an electronic IC to form a laser and detector array on CMOS for parallel optical interconnects [62] and in (c) individual laser diodes were flip-chipped onto a large core SOI photonic integrated circuit [60].

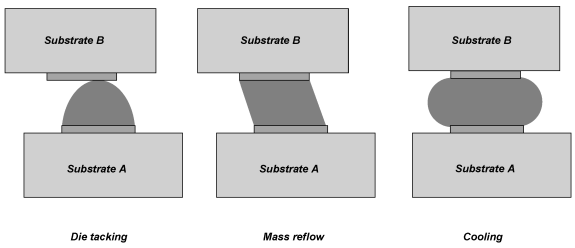


Figure 2.2: Self-aligning properties of the flip-chip process during reflow

Hybrid integration by flip-chip bonding

Of all hybrid integration processes, solder bump flip-chip has the longest production history. The solder bump flip-chip process may be considered as four sequential steps: preparing the wafer for solder bumping, forming or placing the solder bumps, attaching the bumped die to the electronic or photonic carrier, and completing the assembly with an adhesive underfill. In a first step, the under-bump metallization (UBM) is formed. This UBM consists of a solder wettable layer, which offers an easily wettable surface to the molten solder during assembly, for good bonding of the solder to the underlying metal. Solder bumps may be formed or placed on the UBM in many ways, including evaporation, electroplating, screen printing, jetting and stud bumping. Assembly operations include handling, placing, fluxing, and solder joining. One function of the solder bump is to provide some space between the chip and the substrate. In the last stage of assembly, this space is usually filled with a non-conductive underfill adhesive, joining the entire surface of the chip to the substrate. The underfill protects the bumps from moisture or other environmental hazards, and provides additional mechanical strength to the assembly. However, its most important purpose, particularly with solder bumps connections on large die or to organic substrates, is to compensate for thermal expansion differences between the chip and the substrate. In solder bump flip-chip processes, reflow of the bumps is often used to self-align substrate and chip due to the surface tension of the molten solder bump. This is schematically depicted in figure 2.2.

Many other types of flip-chip bonding exist, differing by the materials used to provide the electrical contacts and the way the dies are attached to the substrate. Most commonly used in opto-electronics is

AuSn bump bonding. Besides AuSn bumps, pure gold bump thermo-compression bonding is also used.

In ultrasonic bonding, after accurate alignment and placement of the chip to the substrate, the chip is activated by ultrasonic power into a one direction oscillation. Mainly gold is used as interconnect material, as well for the bump as for the substrate pad surface. Supported by force and heat, the chip bumps are scabbing on the surface of the substrate pads, thereby creating a connection between bumps and pads, through the formation of gold to gold metallic bonds.

In adhesive flip-chip technology, an anisotropic conductive film (ACF) is used to electrically connect the die to the substrate and to mechanically attach the die. Using anisotropic conductive adhesive, the electrical contact is restricted to the vertical direction. Typically, high bonding forces are needed to crush the conductive particles within the ACF-material to create the conductivity.

Advantages and disadvantages of flip-chip bonding for optical applications

Flip-chip technology provides various advantages, both for the integration of optical components and for electronic components. As it is a well known technology, it is the most rugged. It supplies an electrical, thermal and mechanical connection at once and allows testing of the die to be placed in advance.

For integration of opto-electronic components it has some distinct disadvantages too however. As typically very accurate alignment is needed (sub 1μm alignment tolerance), the hybrid integration process is difficult, slow and costly. Moreover, as this is done on a die-per-die basis, the process time is further increased. In the case of integration on a photonic IC, a separation of multiple micrometers between both ICs is created, which makes optical coupling between the photonic IC and the flip-chipped opto-electronic components difficult. The component density is also limited by the pitch and size of the bumps.

2.3 Hetero-epitaxial growth

2.3.1 Direct III-V growth on silicon

A radically different approach is the direct epitaxial growth of III-V material on silicon and fabrication of opto-electronic components after-

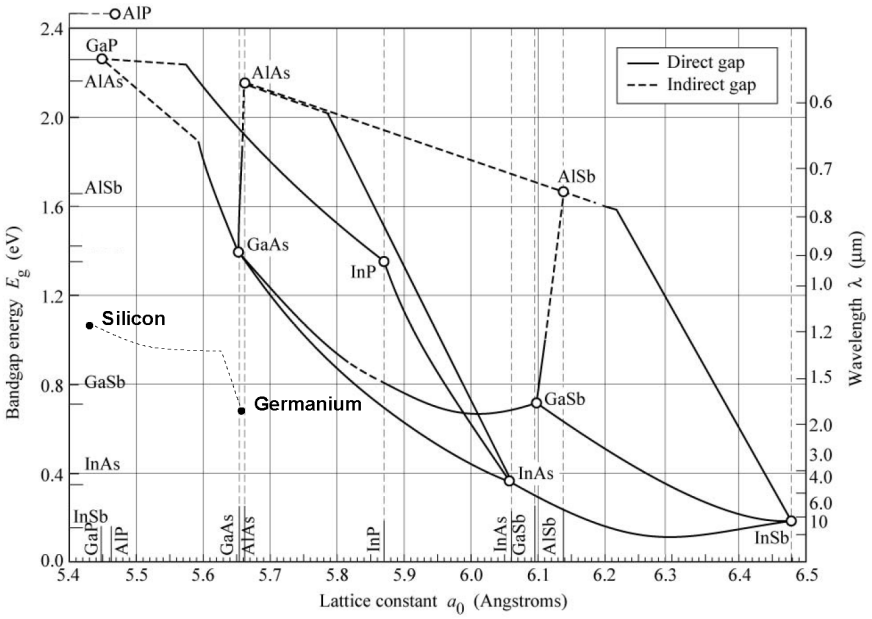


Figure 2.3: Lattice constant and band gap of various III-V semiconductors, silicon and germanium (from [65])

wards. Direct growth is very difficult however, due to the mismatch in lattice constant between III-V materials and silicon, the difference in thermal expansion coefficient and the fact that a polar layer needs to be grown on a non-polar substrate. This can result in large threading and misfit dislocation densities, anti-phase domains and interdiffusion [63], severely degrading the optical properties of the grown layers. The mismatch in lattice constant is shown in figure 2.3. Moreover, contamination issues have to be tackled when combining hetero-epitaxy on silicon with the fabrication of CMOS electronic circuits. In [64], a monolithic, bufferless hetero-epitaxy of AlGaSb on silicon is presented. The growth method is fundamentally different from GaAs growth, since the strain energy due to the lattice mismatch is fully and immediately relieved at the III-V interface in two-dimensional arrays of misfit dislocations, that propagate in the interfacial plane rather than threading into the material. Low defect densities in the grown epitaxial layer structure were reported. As the band gap of GaSb is 0.726eV, laser emission at 1.55μm can be envisaged. The contamination problem for electronic circuit fabrication remains however.

2.3.2 Buffer layers

The use of buffer layers between the silicon and the active III-V layers can partly overcome the above mentioned problems. Motorola developed the growth of GaAs on silicon, by growing a crystalline $SrTiO_3$ (STO) layer on silicon, used as a buffer layer for GaAs growth. Molecular beam epitaxy on 300mm wafers was demonstrated in [66]. In [67] a combination of InGaP, low temperature grown GaAs, InP and a superlattice of InP/InGaAs was grown acting as a buffer layer to grow the device specific layers of InP and InGaAsP on silicon. This "quasi-substrate" shields the growth of crystal defects from the device epitaxial layers. In [68], the growth of graded $Si_{1-x}Ge_x$ on silicon was used to gradually evolve from epitaxial silicon growth to epitaxial Ge growth, which is nearly lattice matched with GaAs. In [69], GaN layers were grown on silicon using AlGaN and AlN buffer layers. In [63] it was acknowledged that the strain field induced by coherently strained quantum dots can inhibit the propagation of dislocations into the device layer grown on top, thereby leading to almost defect free quantum dot layers.

Although being an interesting field of research, most effort in the field has been concentrated so far on growth of GaAs instead of InP on silicon substrates. As the mismatch in lattice constants between GaAs and silicon is only 4 percent compared to the 8 percent mismatch between InP and silicon, the defect free epitaxial growth of InP/InGaAsP is further away. While obtained in [67], thick buffer layers were needed to create the quasi-substrate (about 8μm to obtain a high quality laser structure), which doesn't facilitate the processing and the optical coupling to an underlying waveguide circuit.

2.3.3 Epitaxial lateral overgrowth

Epitaxial lateral overgrowth techniques are used to grow high quality epitaxial InP on a silicon substrate, provided with a low quality InP seed layer. The principle is shown in figure 2.4.

A low quality layer is first grown on a silicon substrate after which only a part of the surface is exposed for growth, the remaining surface being masked for direct growth. Under these circumstances, the growth starts on the open surface but when the layer reaches a particular thickness, the layer starts to grow laterally from the opening on the masked region. This growth mode retains the defects in and near the mask opening, thereby creating high quality layers around. Although

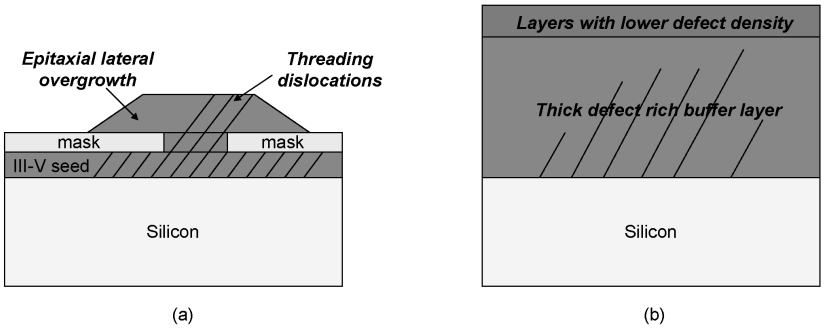


Figure 2.4: Epitaxial lateral overgrowth (a) and the use of thick buffer layers (or a "quasi substrate") (b) to prevent a large dislocation density in the active layer

high quality layers can be obtained, this process is not very versatile. Therefore, there are little reports on opto-electronic components created by epitaxial lateral overgrowth [70].

2.3.4 Poly-crystalline III-V layers

Besides the use of crystalline material, poly-crystalline material could be used as well for certain opto-electronic components. In [71], low temperature grown poly-GaAs on dielectric layers was used to fabricate metal-semiconductor-metal (MSM) photodetectors. The grain boundaries act as trapping and recombination centers. Thereby, using poly-crystalline material, the responsivity of the photodetector is decreased. The speed of the device is however positively affected due to the additional recombination of carriers at the grain boundaries.

2.4 Bonding techniques

2.4.1 Anodic wafer bonding

Anodic wafer bonding is a process in which a glass substrate or a glass layer is permanently joined to silicon without using adhesives. The physics of the anodic bonding process is outlined in figure 2.5.

A glass (mostly Pyrex) containing alkali-metals (typically sodium) is brought in contact with a silicon wafer. The wafers are heated (300C-

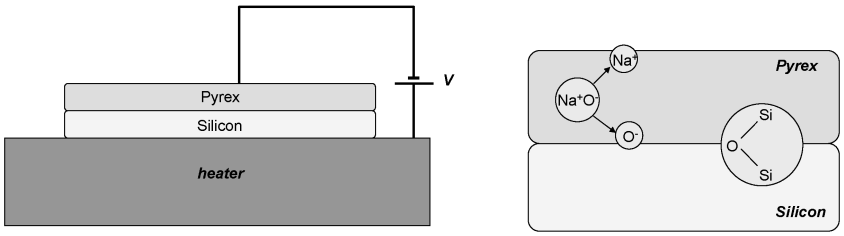


Figure 2.5: Anodic wafer bonding

500C) to dissociate and mobilize the sodium ions. A large voltage (1kV) is applied over the wafer pair resulting in electrostatic attraction and drift of the sodium ions, leaving a depletion layer with high electric field at the interface. In this process, the oxygen ions are drawn to the interface, creating permanent silicon-oxide bonds.

Typically, anodic wafer bonding of glass substrates to a silicon wafer is applied in MEMS and MOEMS packaging [72]. Also for the fabrication of fluidic channels for lab-on-a-chip applications it can be used [73]. As the use of anodic bonding is not restricted to using full glass substrates, a spin coated or deposited layer of glass on a III-V substrate could be used as well [74]. The high temperature and large voltage needed for anodic bonding are a drawback however.

2.4.2 Direct wafer bonding

Physics of direct wafer bonding

It is well known that electrically polarized atoms or molecules are attracted to each other by Van der Waals interaction. Van der Waals interaction originates from atomic and molecular electric dipoles whose orientations are correlated in such a way that they attract each other. This interaction determines the adhesion between the two surfaces. This is is a short-range force

$$f_v = \frac{H}{6\pi d^3}[N/m^2] \tag{2.1}$$

in which H is the Hamaker constant (on the order of $10^{-20}J$ dependent on the material system) and d is the separation of the surfaces.

As Van der Waals interaction requires an intimate contact between the wafer surfaces due to the short-range force, one has to be aware of

roughness and topography of the wafer surfaces, particles at the interface and contamination of the wafer surfaces [75].

A strong type of dipole-dipole attraction is hydrogen bonding in which the hydrogen atom in a polar molecule interacts with an electronegative atom of either an adjacent molecule or the same molecule. Water is a polarized molecule, which allows hydrogen bonding to form between water molecules themselves. If water is present, the linkage of water molecules may bridge two interacting atoms or molecules. In this way a long-range inter-molecular force can be realized.

Although in principle any material combination can be directly bonded [76], one often deposits an SiO_2 layer on both wafers to be bonded and a direct bond is created between those SiO_2 layers [77]. This reduces the amount of process development for a different material combination. In the case where the SiO_2 interface layer is not wanted, direct bonding between the bare wafers needs to be developed.

Surface activation

After removal of particles from the smooth wafer surfaces and removal of contaminants (see section 2.4.6), which could screen the bonds at the wafer surface, the surfaces need to be chemically activated. Both hydrophilic and hydrophobic bonding can be achieved [78]. A hydrophilic silicon (or rather oxidized silicon) surface can be achieved by finishing the surface cleaning by an SC-1 cleaning step (see section 2.4.6). Hydrophobic silicon surfaces can be obtained by immersing the wafer in a buffered HF solution. The evolution of the chemical structure at the bonding interface for both cases, can be seen in figure 2.6.

In the case of hydrophilic bonding, hydrogen bridges initially keep both wafers together. After annealing, H_2O is released from the bonding interface and a strong Si-O-Si covalent bond originates. In the case of hydrophobic bonding, the initial bonding is achieved by HF bridges, which reduce to strong Si-Si bonding after annealing. When using an intermediate SiO_2 bonding layer, a hydrophilic bonding mechanism will be used.

Bonding process

The direct bonding process start by mating the wafer surfaces at room temperature and initiating the bond at a certain point of the wafer surface, by locally exerting pressure on the wafer stack. A bonding wave

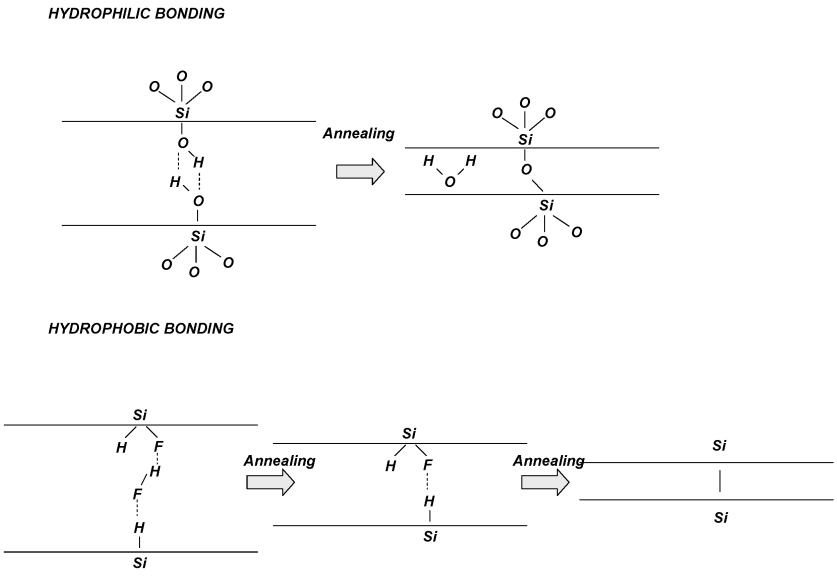


Figure 2.6: Hydrophilic and hydrophobic bonding mechanisms for (oxidized) silicon surfaces

propagates throughout the wafer area as shown in figure 2.7, attaching the wafers. As discussed above, an annealing step is required to increase the bonding energy after contacting.

2.4.3 Metallic wafer bonding

Metallic bonding is based on using a combination of metals as bonding agent. Two types of metallic bonding layers exist: hard and soft alloys. Hard alloys can easily elastically deform, but have a very limited plastic deformation. This makes the bond resistant to metal fatigue. Stresses in the structure can however not be taken up by the plastic deformation of the metal. Soft alloys deform plastically to relax the stress developed. This also means that they are subject to thermal fatigue, causing reliability problems.

Mostly eutectic alloys are used for bonding. An eutectic alloy is a mixture of two phases at a composition that has a single melting point (or a small plastic temperature range). Solid products of an eutectic transformation can often be identified by their lamellar structure, as

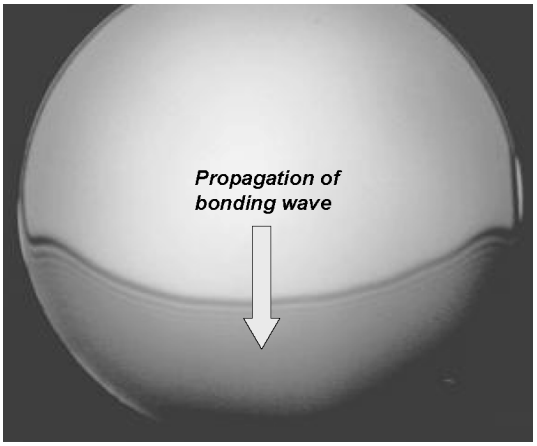


Figure 2.7: Infrared transmission picture of bonding wave propagation in direct bonding

Eutectic alloy	Melting temperature	Type
$Au_{80}Sn_{20}$	$278C$	hard
$Au_{19}Si_{81}$	$363C$	hard
$Au_{88}Ge_{12}$	$356C$	hard
$Sn_{63}Pb_{37}$	$183C$	soft
$In_{52}Sn_{48}$	$118C$	soft
$Pb_{60}In_{40}$	$195C$	soft
$Sn_{96.5}Ag_{3.5}$	$179C$	soft

Table 2.1: Properties of most used alloys for bonding

opposed to the dendritic structures commonly seen in non-eutectic solidification.

The requirements for an eutectic alloy for wafer bonding are to be lead free and allow for a fluxless bonding process (a flux is used to prevent the oxidation of the metals prior to bonding). The alloy should have a sufficiently low melting temperature, depending on the temperature the structures to be bonded can sustain, but not too low to allow sufficient thermal budget for post-processing. Reliability is another important issue: slow growth of intermetallic compounds at the bonding interface can reduce the strength of the bond and finally cause breakage of the bond due to thermally induced stress.

A review of the most common eutectic alloys used for bonding is shown in table 2.1, together with their melting temperature and type of alloy. Besides for use in flip-chip technology as bump material, these alloys can also be used for full sheet bonding of two wafer surfaces.

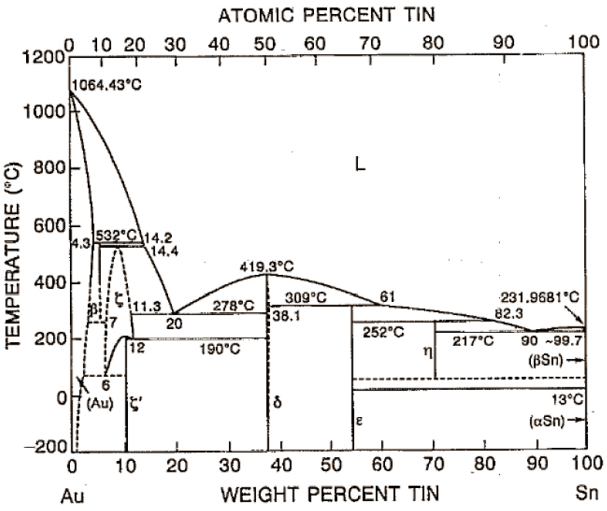


Figure 2.8: AuSn phase diagram

The most commonly used alloy is $Au_{80}Sn_{20}$. As it is a hard solder, it cannot take up a large amount of stress, which could lead to die cracking if the dies are large. The advantages are the high melting temperature, the ability to solder without flux, the formation of a hermetic seal and excellent thermal, mechanical and electrical properties. The AuSn binary phase diagram is shown in figure 2.8. The other eutectic alloy, $Au_{10}Sn_{90}$ will not produce reliable solder joints due to the formation of a brittle $AuSn_4$ intermetallic compound within the solder joint [79]. Although the $Au_{80}Sn_{20}$ eutectic alloy is most commonly used, non-eutectic AuSn compositions have also been used to create reliable metallic bonds [80].

2.4.4 Wafer bonding using an adhesive layer

Physics of adhesive wafer bonding

An adhesive is defined as a material capable of holding two materials together by surface attachment, which resists separation. It typically concerns polymers, i.e. macromolecules that are formed by linking of many simpler molecules known as monomers (this process is referred to as curing). In general, polymers are able to spread and interact on the surface of the substrate material.

The interfacial bonding formation follows a sequence of wetting (i.e. a molecular contact between the adhesive and the adherent is es-

tablished at the interface by a flow process), adsorption (i.e. formation of the adhesive bonding across the interface) and cross-linking of the molecules. Interdiffusion can occur, when both the adherent and adhesive are polymers with similar solubility parameters.

Several theories of adhesion have been proposed. However, no single theory is capable of describing all types of adhesive interactions [81].

The adsorption theory relates adhesion to the interatomic or intermolecular attractive forces between the adhesive and adherent. According to this mechanism, the wetting of the adherent by the adhesive is a key factor in determining the strength of the adhesive bond and is determined by the surface energy of the adhesive and the adherent (see section 3.8). The surface energy of the adherent must exceed that of the adhesive by at least $10\mathrm{mJ/m^2}$ for adequate wetting of the surface. However, the surface energy of the substrate is reduced if there are contaminants (weakly absorbed organic molecules or condensed moisture) absorbed on the substrate, thereby reducing the adhesive bonding strength.

In the chemical bonding theory, the adsorption theory is extended by stating that besides adsorption also a chemical reaction occurs at the wafer surface.

The mechanical interlocking model attributes the origin of the adhesive bond to the surface roughness of the adherent. This provides a greater number of interlocking sites and a larger surface area for the bond. Such interlocking may take place in the case of adhesive flowing into troughs in the adherent surface or around protrusions on the surface.

While this being the most important theories, diffusion mechanisms (primarily for the bonding of thermoplastic materials), electrostatic attraction theory and weak boundary layer theory (attributing the maximum adhesion strength to the occurrence of weak boundary layers of low molecular weight) are also described in literature [81].

Depending on the type of polymer, the curing of the polymer can be done in different ways. Heat or UV light are the most common methods for curing the adhesive. Besides these activation methods also drying adhesives (polymers dissolved in solvents that harden when the solvent is evaporated), two-component epoxies, anaerobic adhesives (which cure in an oxygen free environment) and adhesives that cure in the presence of moisture are used [82].

Surface modification for adhesion improvement

As was discussed in the previous section, hydrocarbon contamination can reduce the adhesive bonding strength, due to a reduction in surface energy of the adherent (adsorption theory) or due to the fact that it can be considered as a weak boundary layer (weak boundary layer theory). This contamination can be removed by plasma treatment [83, 84], wet chemical etching of the surface [84] or by UV/ozone treatment [85].

An exception is the application of an organic adhesion promoter to the surface, which improves the bonding strength due to the formation of chemical bonds between the adhesive and the adhesion promoter molecule (see section 3.3.1), which is in accordance with the chemical bonding theory.

2.4.5 Glass frit bonding

Frit bonding is a fusion process, in which a glass frit (a slurry of fine glass particles in an appropriate carrier liquid) is applied to the surfaces to be bonded and then heated to a molten state, while the surfaces are held in close contact. Bonding occurs upon cooling and solidification of the glass through a combination of wetting and chemical reaction between the molten glass and the substrate material. Typically, bonding layers are a few tens of micrometer thick. The glass frit can be structured on the wafer surface using a screen printing technique [86].

2.4.6 Substrate preparation

Surface planarization

As in the various bonding techniques described above, an intimate contact between both wafer surfaces is needed, surface roughness and surface topography can be critical to achieve a successful bonding. The difference between surface roughness and topography is the spatial frequency: topography has a low spatial frequency, while roughness has a high spatial frequency.

Different topography planarization techniques exist, as shown in figure 2.9. A standard technique involves the thermal flow of borophosphosilicate glass (BPSG), deposited by a chemical vapor deposition process, which can be used to partially planarize a topography. Additional layers can be used to further planarize the topography, either by applying an etch back process (sacrificial layers) or without applying an

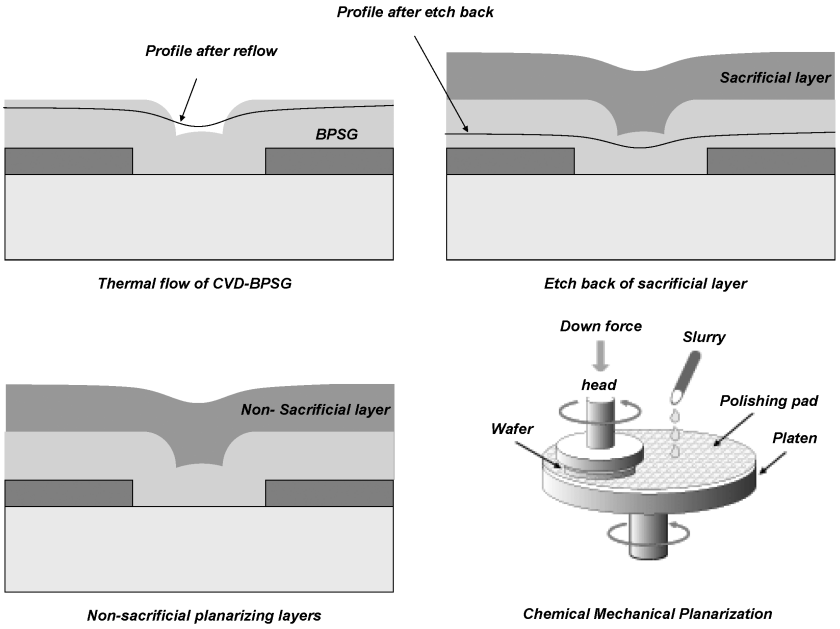


Figure 2.9: Topography planarization techniques: thermal flow of BPSG, etch-back of a sacrificial layer, non-sacrificial planarizing layers and chemical mechanical planarization

etch back process (non-sacrificial layers). However, chemical mechanical polishing (CMP) is the only technique that can planarize on a global scale. Besides planarization of the surface topography, the maximum surface roughness requirements for direct bonding (typically 6 angstrom RMS roughness [84]) can be achieved using CMP.

CMP uses a polishing pad and slurry, dependent on the surface to be polished. The CMP mechanism is a two step process: a chemical reaction of the surface with the slurry chemistry forms a wafer surface layer that is relatively easy to remove. This layer is mechanically removed by the slurry's abrasive component, due to the applied pressure and relative velocity of the polishing pad.

The rate of polishing R is given by Preston's equation [87]. The removal rate is proportional to the applied pressure and relative velocity v between wafer and polishing pad

$$R = kPv \tag{2.2}$$

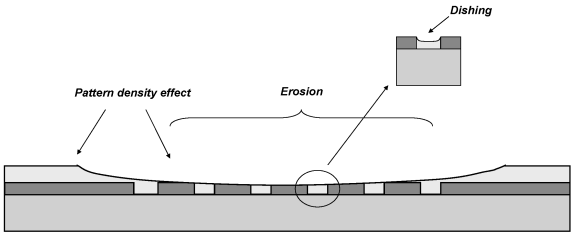


Figure 2.10: Dishing, erosion and pattern density effect in CMP

in which k is a constant depending on the tool and process conditions. The applied pressure depends on the area that is in contact with the polishing pad. As explained in [87], a local pattern density needs to be defined, in order to determine the polishing rate at a particular point, taking into account the pattern density in an area (the size of which depends on the tool) surrounding that point on the wafer.

However, problems can occur when using chemical mechanical polishing. Dishing, erosion and pattern density effects are typical phenomena occurring during CMP. These are schematically shown in figure 2.10. Pattern density effects originate from the variation of polishing rate, caused by a variation in local pattern density. Erosion may also occur, typically when soft materials are present (showing a higher removal rate). Also, local dishing might occur. Dishing is a reduction in the thickness of a material towards the center of the feature. The hardness of the pad determines the amount of dishing due to bending of the pad into the soft material.

While polish stop stubs can be used to accurately determine the thickness of the resulting polished layer, in direct wafer bonding often a blind polish stop is needed, for example in the case of SiO_2 direct bonding, where a controlled SiO_2 bonding layer thickness is needed. To achieve this, time-based polishing (most widespread but resulting in thickness deviations between wafers) or in-situ interferometric thickness measurements can be used.

Particle contamination and wafer cleaning

Besides the planarization of the original topography, the occurrence of unwanted topography in the form of particles pinned to the surface must be avoided. Although cleanrooms are specially equipped to reduce the airborne particle concentration, perfect particle-free operation

Class	Official	0.1μm	0.2μm	0.3μm	0.5μm	1.0μm	5.0μm
	ISO1	10	2				
	ISO2	100	24	10	4		
1	ISO3	1000	237	102	35	8	
10	ISO4	10000	2370	1020	352	83	
100	ISO5	100000	23700	10200	3520	832	29
1000	ISO6	1000000	237000	102000	35200	8320	293
10000	ISO7				352000	83200	2930

Table 2.2: Number of particles per cubic meter for different classes of cleanrooms

cannot be obtained. In table 2.2 the particle concentrations per cubic meter for different classes of cleanrooms are listed.

When a particle gets pinned to a surface, a large debonded area will occur upon bonding of the wafers, as the wafers have to elastically deform to compensate for the particle topography. For the case of direct bonding, the radius R of the bonding defect that originates from a particle with height $2h$ was derived in [84] to be given by

$$R = \left[\frac{1.3E_1't_1^3E_2't_2^3}{\gamma(E_1't_1^3 + E_2't_2^3)}\right]^{1/4} h^{1/2} \tag{2.3}$$

with $E_i' = \frac{E_i}{1-\nu_i^2}$ the biaxial Young's modulus (E_i is the Young's modulus and ν_i is the Poisson ratio of wafer i). t_i represents the thickness of the wafers and γ is the bonding energy. This equation is valid for sufficiently large defects. If the R calculated by equation 2.3 gets too small an elastomechanical instability occurs leading to a different equation for the defect radius given by [84]

$$R = \frac{h^2(E_1' + E_2')}{6\gamma} \tag{2.4}$$

These functions are plotted in figure 2.11, for different bonding energies in the case of a 500μm thick Pyrex wafer directly bonded to a 750μm thick silicon wafer. As can be seen from the plots, typically a particle with height $2h$ leads to a defect size of about $R \approx 10000h$.

Although the description of the influence of particles at the bonding interface in the case of adhesive bonding is identical to the case of direct wafer bonding, the influence is reduced by the planarizing action of the adhesive coating, as is shown in figure 2.12. The thicker the adhesive bonding layer becomes, the better the bonding layer can accommodate for particles at the bonding interface. This is an important advantage of adhesive bonding over direct bonding, as it relaxes the required surface

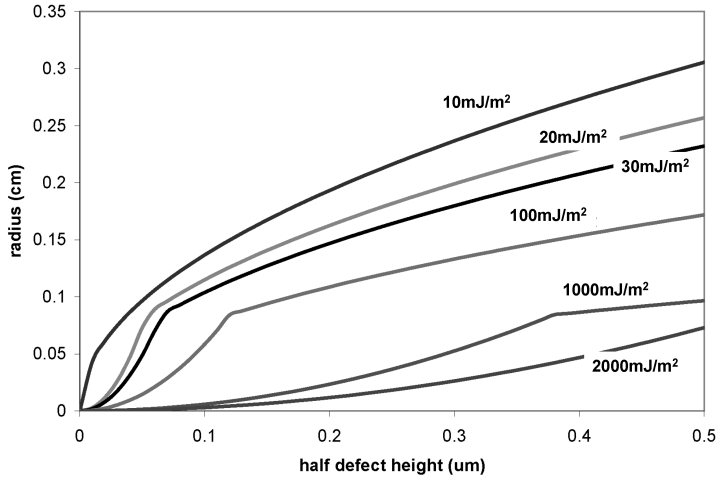


Figure 2.11: Bonding defect radius as a function of particle size for a silicon wafer bonded to Pyrex

cleanliness. Although in principal a surface can be made particle-free prior to bonding, still spikes can occur on the grown surfaces due to the incorporation of particles in the epitaxial layer stack during growth. These can also be accommodated for by imprinting the spikes in the adhesive bonding layer, provided that the bonding layer is sufficiently thick.

From the discussion above, it is clear that a crucial step in achieving a high quality bond is to remove the particles from the wafer surface prior to bonding. In the cases where a CMP polishing process is used, some abrasive particles from the CMP process may have clustered on the wafer surface and need to be removed. This is done using a scrubbing process, in which the wafer is fed to a system of rotating brushes, which mechanically remove the particles without damaging the wafer surface. Although the surface may be particle-free after scrubbing, the handling of the wafer and the exposure to cleanroom air can invoke a redeposition of airborne particles on the wafer surface.

In order to remove these particles, several cleaning methods can be used. CO_2 snow cleaning is based upon the expansion of either liquid or gaseous CO_2 through an orifice. This expansion leads to the nucleation of small dry ice particles and a high velocity gas carrier stream. Upon impact with a contaminated surface, the dry ice removes particles

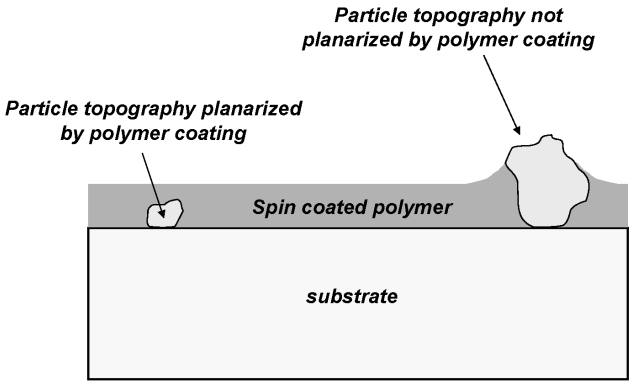


Figure 2.12: Planarization of topography caused by particles by spin coating of a polymer bonding agent

by momentum transfer and hydrocarbons via a transient solvent mechanism. The high-velocity gas stream blows the contaminants away [88].

Wet chemical removal of particles on a silicon wafer can be done using a Standard Clean 1 solution (SC-1), which is a mixture of NH_4OH, H_2O_2 and H_2O. This is an alkaline solution, capable of removing particles and organic materials. For particles, it primarily works through oxidation of the particle and electrical repulsion. H_2O_2 is a powerful oxidizing agent that oxidizes the wafer surface and the particle. The NH_4OH slightly etches the wafer surface and undercuts beneath the particle. This can lift off the particle from the surface. Actually, an electrical repulsion of the particle is achieved. The NH_4OH builds up a negative charge on the particle and the wafer surface, which serves to repulse the particle from the surface.

This electrical repulsion is described by the Zeta potential of a particle in a solution, as shown in figure 2.13. The development of a nett charge at the particle surface affects the distribution of ions in the neighboring interfacial region, resulting in an increased concentration of ions of charge opposite to that of the particle close to the surface. Thus an electrical double-layer is formed in the region of the particle-liquid interface (Stern layer). The double-layer may be considered to consist of two parts: an inner region, which includes ions bound relatively strongly to the surface (including specifically adsorbed ions) and an outer, or diffuse, region in which the ion distribution is determined by a balance of electrostatic forces and random thermal motion. The po-

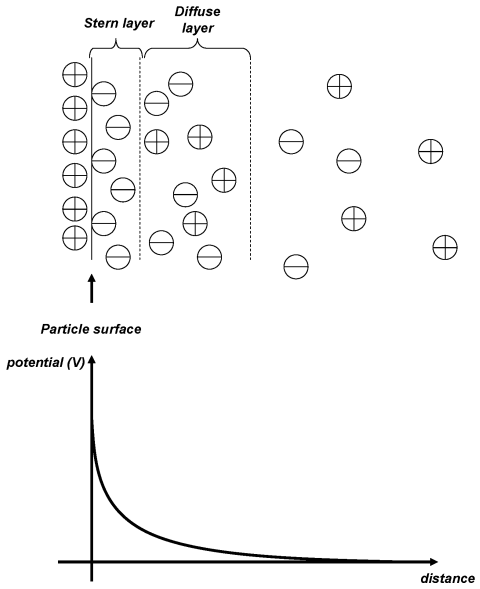


Figure 2.13: Wafer particle removal - charge distribution around a particle in a solution and the definition of the Zeta potential

tential in this region therefore decays as the distance from the surface increases until, at sufficient distance, it reaches the bulk solution value.

The Zeta potential of a type of particle in a solution can be measured by electrophoresis measurements. The Zeta potential is a strong function of the pH of the solution in which the particles are present. It turns out that only for very alkaline solutions (high pH) or very acidic solutions (low pH) , the sign of the Zeta potential of the most common type of particles that exist on the wafer surface is the same. In these type of solutions, particles are repulsed from each other and from the wafer surface that is also present in the solution, which prevents redeposition of the lifted particles back on the wafer surface.

Metal contamination can be removed using a Standard Clean 2 solution (SC-2), a mixture of HCl, H_2O_2 and H_2O. SC-2 is not effective at surface particle removal. However, it may impact particle redeposition. Both silicon and SiO_2 have relatively low Zeta potential in acidic solutions, therefore SC-2 is not effective at preventing redeposition.

Megasonics can be used to increase the particle removal efficiency. Megasonic cleaning uses acoustic energy with frequencies near 1MHz during the clean process. Particle removal is achieved by shock waves

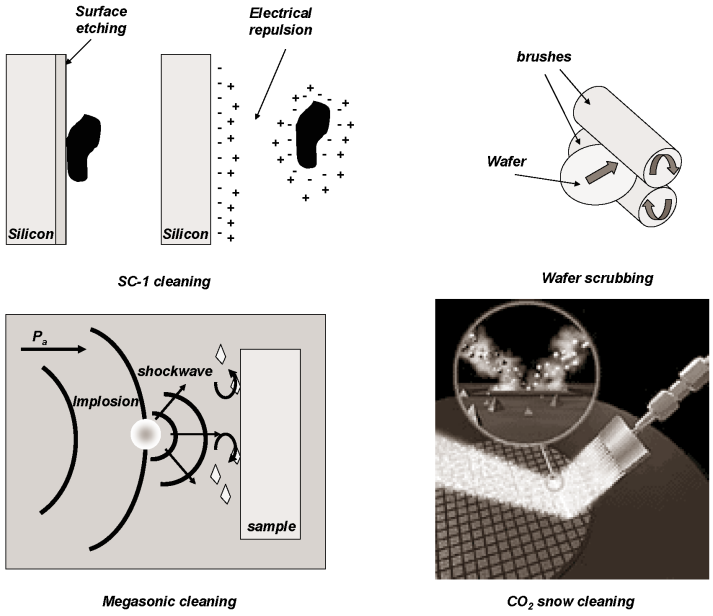


Figure 2.14: Wafer particle removal mechanisms: SC-1 cleaning, wafer scrubbing, megasonic cleaning and CO_2 snow cleaning

originating from cavity implosions in the cleaning solution, due to the presence of the ultrasound waves. High frequencies are required, because the stagnant boundary layer in the cleaning fluid near the wafer surface becomes thinner as the frequency is increased. Effective cleaning requires a boundary layer thinner than the minimum particle size being cleaned for. The different cleaning mechanisms are presented in figure 2.14.

2.4.7 Substrate removal

How a substrate is removed after bonding depends on the material used and the applied bonding technique. Three types of substrate removal techniques are used: the epitaxial lift-off process, mechanical grinding / chemical etching and the SmartCut process.

Epitaxial lift-off

Epitaxial lift-off is the separation of single crystal epitaxial compound semiconductor layers from a lattice-matched growth substrate, through

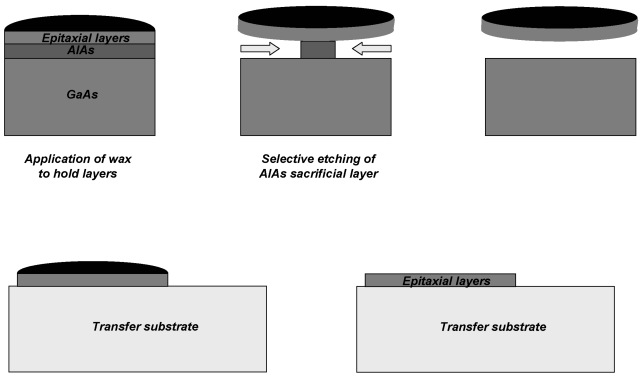


Figure 2.15: Epitaxial lift-off process

selective etching, prior to bonding. Using handling layers and transfer techniques these thin film materials can be handled with tweezers after separation, processed on both sides, aligned and bonded onto arbitrary host substrates.

The fabrication of InP-based epitaxial lift-off thin film material has developed along two paths. A non-lattice matched AlAs layer can act as a sacrificial etch layer [89] or the growth substrate can be completely dissolved until an etch stop layer is reached [90]. InP buffer layers are needed in the first case, in order to have sufficient epitaxial layer quality due to the lattice mismatch.

Samples typically are coated with Apiezon wax as a handling layer. After substrate removal and bonding of the sample, the Apiezon wax is removed in trichloroethylene (TCE). The process is schematically described in figure 2.15.

As Apiezon is opaque, a transfer diaphragm technique was developed in which the epitaxial layers were bonded to a transparent polyimide film suspended on a silicon ring prior to bonding [91].

Mechanical grinding and chemical etching

The most common technique used to remove the substrate from a bonded epitaxial layer is using a combination of mechanical grinding and chemical etching. The mechanical grinding uses an abrasive slurry (typically an AlO_x suspension) to thin the substrate. The size of the abrasive particles, the pressure exerted on the samples during grinding and the rotation speed of the platen has to be optimized for each type of

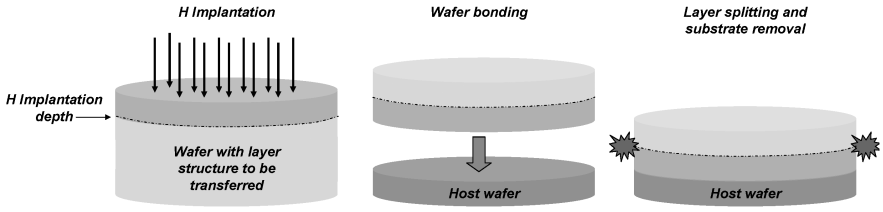


Figure 2.16: Layer splitting by the SmartCut-process

material. After mechanical grinding, the final part of the substrate removal can be done using wet chemical etching, with an etchant that has very high etching selectivity to a grown etch stop layer. This typically is HCl for InP [92] (with InGaAs as an etch stop layer) , KOH for silicon [93] (with SiO_2 as an etch stop layer) and NH_4OH:H_2O_2 for GaAs (with AlGaAs as an etch stop layer) [92]. Complete chemical etching of the substrate is also possible in some cases. This could however increase the substrate removal time and also increases the time the bonding interface is exposed to chemicals. To avoid this, the additional mechanical grinding step is added. In particular cases, this grinding can also help to avoid wet etching edge effects due to the typically anisotropic nature of the etching process (see section 3.5.6).

SmartCut process

The Smarcut process is based on hydrogen-implantation before bonding [84, 94]. This leads to hydrogen-filled micro-cracks induced by the precipitation of the implanted hydrogen during a heating step after bonding and leads to a splitting of the wafers. After layer splitting the wafer surface needs to be polished. The advantage of this technique is the possibility for reuse of the splitted wafer. In the so called SmarterCut process [84], co-implantation of boron is used to reduce the time and temperature required for splitting considerably.

2.4.8 Wafer-to-wafer bonding versus die-to-wafer bonding

Wafer-to-wafer bonding

In literature and industry, most technology development is done on wafer-to-wafer bonding, for example direct bonding for the fabrication

of silicon-on-insulator wafers [84] (see section 5.1.1) and germanium-on-insulator wafers [95], Pyrex to silicon anodic or adhesive bonding for MEMS/microfluidics [72] and the adhesive bonding of a GaAs wafer to a silicon wafer [96] for opto-electronic applications . The wafer-to-wafer bonding technology enables the creation of new types of substrates. An efficient use of wafer area requires that both wafers have the same dimensions. An additional advantage of wafer-to-wafer bonding is that the use of full wafers enables the use of standard equipment for wafer handling, cleaning and bonding.

In the case of bonding of III-V wafers onto silicon, some considerations have to be made. Although GaAs substrates are available up to 6 inch in diameter, InP wafers are limited in size to 4 inch. Nowadays silicon wafers are typically 8 or 12 inch in diameter resulting in a huge discrepancy in wafer size. Although this can be accounted for by bonding multiple InP wafers onto a single silicon wafer, this would result in a huge cost, due to the high price of the InP epitaxy. This cost can be drastically reduced, by only bonding InP in the areas where it is needed.

Die-to-wafer bonding

Die-to-wafer bonding is required when bonding is only wanted in designated areas. Although more cost effective in terms of material usage, no established solutions exist to clean, handle and bond dies. Cleaving or sawing of dies can invoke chipping of the die edges, leading to imperfect bonds. Also, the presence of small particles can completely detach small dies, as will be discussed in chapter 3.

2.5 Comparison of different integration techniques

In table 2.3, the different integration techniques are compared by their versatility, particle sensitivity, etc. For the application of heterogeneous integration of InP/InGaAsP active layer structures on silicon-on-insulator waveguide circuits, as discussed in chapter 1, it can be argued that adhesive bonding is the preferred bonding method. This is due to its high versatility, the lower particle and surface roughness sensitivity, the low bonding temperature and low cost of the technology. Moreover, a large range of bonding layer thicknesses can be achieved, which makes it an even more versatile process. The drawbacks of the technology are

Property	Flip-chip	Epitaxial	Anodic	Direct	Adhesive	Glass frit	Metallic
versatility	very good	poor	poor	very good	very good	very good	very good
particle sensitivity	low	medium	medium	very high	medium	low	high
surface roughness sens.	low	low	low	very high	low	low	low
bonding temperature	low	high	high	low	low	medium	low
hermetic seal	no	yes	yes	yes	no	yes	yes
substrate separation	μm range	none	none	1nm-1μm	20nm-50μm	20μm	0.1-few μm
thermal conductivity	high	high	high	high	low	low	high
optical transparency	yes	yes	yes	yes	yes	yes	no
cost	high	high	low	medium	low	low	low

Table 2.3: Comparison of integration techniques

the low thermal conductivity of the adhesive and the fact that little is known on the long-term stability of the adhesive bond.

An emerging technology is the use of direct wafer bonding, especially for the fabrication of new types of substrates like silicon-on-insulator or germanium-on-insulator. As in these cases one can rely on highly developed processing and cleaning technology, direct wafer bonding is the preferred choice. It avoids the use of organic materials at the bonding interface, which might improve the long-term stability of the bond. As the bonding of III-V epitaxial layer structures is concerned, the quality of the wafer surfaces is lower, resulting in an advantage of adhesive wafer bonding over direct wafer bonding.

In current commercial devices, flip-chip processes are used [21], which are also versatile, less sensitive to particles and surface roughness and show a low bonding temperature. Moreover, bonded devices have a low thermal resistance, due to the high thermal conductivity solder bumps connecting the devices to the substrate. A drawback of this process is the high cost however, due to the required alignment accuracy between die and substrate. Also, a relatively large spacing between the bonded die and the substrate is needed, making optical coupling between the die and substrate more difficult (see chapter 4).

2.6 Conclusions

Die-to-wafer bonding technology is an enabling technology for integrating expensive III-V material on a host substrate. Adhesive bonding has some distinct advantages over other bonding methods: it is a low temperature process that is flexible with regards to wafer material. The planarizing properties of the adhesive spin coating process and the reduced requirements for surface quality (at least for thick bonding layers) is an additional advantage compared to direct wafer bonding.

Especially, it is a low-cost and fast process compared to flip-chip technology.

Chapter 3

Die-to-wafer bonding process development

It has got to be perfect
Fairground Attraction

In this chapter, we will discuss the development of an adhesive die-to-wafer bonding process. Following a review of the various types of adhesives used in literature, we will focus on the development of a bonding process using DVS-BCB and spin-on glass carried out in the context of this PhD. Especially, the use of a sub-micron bonding layer thickness will be discussed. The characterization of the bonding interface and the stress distribution in the bonded layer stack will be discussed. Finally, possible routes for extending the developed single die-to-wafer bonding process to a multiple die-to-wafer bonding process will be presented.

3.1 Introduction

As discussed in the previous chapter, different technologies are available for heterogeneous integration. We concluded that adhesive bonding has some distinct advantages over other integration methods. As the choice of the adhesive depends on the application, we will start with a literature review of the various types of adhesives used, to come to the selection of two types of adhesives for bonding, suitable for the heterogeneous integration application. The literature review is not exhaustive. An extensive review of adhesive wafer bonding can be found in [82].

3.2 Literature review

In literature, thermoplastic, elastomeric and thermosetting materials are used for adhesive bonding. As thermoplastics remelt when heated sufficiently, the post-bonding thermal budget for processing of devices is limited in these cases. This is not the case for thermosetting materials, for which the temperature stability of the material will determine the post-bonding thermal budget. Elastomers (often referred to as rubbers), typically show viscoelastic behavior: they exhibit the characteristics of a viscous liquid and an elastic solid at elevated temperature.

In [97], 1 μm thick polymethylmethacrylate (PMMA, a thermoplastic material) was used to bond two 1 inch silicon wafers. The bonding was performed at 160C, followed by an annealing step at 180C. The bonding force was high, as a writing technique was used, implying the use of a pen to write over the bonded stack to locally contact the wafers. In the experiment no post-bonding temperature excursions were made. 3MPa tensile strength of the bond was reported.

In [98], 1 to 5μm thick polyparaxylylene (Parylene, a crystalline thermoplastic material) was used to bond 3 inch silicon wafers. The bonding was performed at temperatures between 160C and 200C. The parylene was deposited on the wafer surfaces using a chemical vapor deposition process (CVD). The applied bonding force varied between 0.9MPa to 1.5MPa. No post-bonding temperature excursions were made, while it was stated that the glass transition temperature is below 90C (melting temperature 290C). 13MPa die shear strength was measured for a 2μm thick bonding layer.

In [99], 10 to 25μm thick poly-dimethylsiloxane (PDMS, an elastomeric material) layers were used to bond two 1 inch PMMA substrates. The bonding was performed at 90C. The applied bonding pressure was about 50kPa. In the experiment, no post-bonding temperature excursions were made. 15kPa tensile strength was reported.

In [100], 1.5 to 2.3 μm thick (thermosetting) Shipley photoresist S1818 layers were used to bond 2 inch silicon wafers. The bonding was performed at 120C using 300kPa bonding pressure. In the experiment, no post-bonding temperature excursions were made. The reported bonding strength was low compared to other thermosetting adhesives used, like polyimide and DVS-BCB.

In [101], 20 to 45 μm thick SU-8 epoxy layers (thermosetting) were used to bond a 4 inch silicon wafer onto a 4 inch Pyrex wafer. The bonding was performed at 120C using 300kPa bonding pressure. In the ex-

periment, no post-bonding temperature excursions were made. 8MPa die shear strength was reported. In [102], a silver-loaded conductive epoxy (Epo Tek H20E) was used to bond 2 inch GaAs wafers. The thickness of the bonding layers used in the experiments was not specified. The bonding was performed at 120C, while the bonding pressure was not specified. In this experiment, post-bonding processing was performed: the original GaAs substrate was removed using a combination of mechanical grinding and chemical etching and LEDs were processed in the bonded epitaxial layer.

In [100], Dupont polyimide PI2610 (a thermosetting material) was tried as an adhesive, to bond two 4 inch silicon wafers. Large unbonded areas resulted due to the presence of voids at the bonding interface. This is attributed to the creation of by-products during the imidization-process, which get trapped at the bonding interface, and to the large volume shrinkage upon cure, which might affect the adhesion due to high stresses in the polymer coating.

Spin-on glass (SOG) was used in [103] to bond 1cm^2 InP/InGaAsP VCSEL epitaxial layer structures to a silicon substrate. The bonding layer thickness varied from a few tens of nanometer to 300nm by varying the pressure exerted on the wafer stack. In this case, the spin-on glass was spin coated very slowly in order to remain liquid after spin coating. After mating of the surfaces, a bonding pressure between 10 and 60kPa was applied on the wafer stack. The wafer stack was cured at 400C. Two types of spin-on glass were used for the experiments: all samples bonded with silicate SOG tended to separate when trying to cut them using a dicing saw. Experiments with siloxane SOG, spin-on glass with a higher organic content, were successful. This difference is attributed to the large shrinkage of the silicate SOG upon cure, resulting in a large film stress, and the low cracking resistance of the silicate SOG. In [104], 100mm and 150mm silicon wafers were bonded using SOG. A high bonding strength was measured after room temperature bonding, due to the chemistry at the SOG/silicon interface, resulting in bonding at room temperature. Thermal annealing was performed at 200C for 18 hours. Defect free bonded wafer pairs were obtained. This process was also used for the fabrication of GaAs/silicon heterostructures. Annealing temperatures were limited to 225C in order to avoid debonding and shattering of the GaAs wafer. After thinning the GaAs substrate to a remaining thickness of 10μm, the bonded pair was heated to 450C without debonding or void generation at the bonding interface.

In literature, there are many reports available on the use of DVS-BCB (divinylsiloxane-bis-benzocyclobutene, a thermosetting polymer, also referred to as BCB) as an adhesive bonding agent. In [100], DVS-BCB was compared to other types of adhesives (photoresist and polyimide) for the bonding of 4 inch silicon wafers. High bonding strength and void free bonds were obtained with DVS-BCB. This was attributed to the low volume shrinkage of the adhesive. After spin coating of a 1.2μm thick DVS-BCB layer, the polymer was pre-baked to evaporate the solvent. After evaporation, the wafers were joined in a vacuum environment. A bonding pressure of 200kPa was used to mate both silicon wafers. The wafer stack was cured at 250C to obtain a fully polymerized DVS-BCB layer. In [104], 8.3μm DVS-BCB layers were used to bond 200mm silicon wafers. DVS-BCB was spray coated onto the silicon surface and the bonding procedure was identical to the previously discussed method. In [100], DVS-BCB was used to bond structured wafer surfaces, using multiple micron thick bonding layers. Structured silicon wafers were bonded both to unpatterned silicon wafers and Pyrex wafers. Many other papers report on the properties (bonding strength, residual stress, bonding quality) of DVS-BCB bonding [105, 106, 107].

3.3 Material Selection

As will be discussed in chapter 4, sub-micron bonding layers are required for efficient optical coupling between an SOI waveguide layer and the bonded III-V layer stack. From the literature study presented above, we focused on two types of bonding agents to achieve this. DVS-BCB was chosen for its high bonding strength and superior bonding quality [100], its high degree of planarization, its high resistance to all sort of chemicals used in standard III-V processing and the fact that no by-products are created during curing. Sub-micron bonding layer thicknesses were however not yet demonstrated prior to this work. Spin-on glass was chosen as very thin layers are achievable using commercially available solutions and bonding using these very thin layers was already demonstrated [103]. This was however only demonstrated on planar substrates. Both materials have a high glass transition temperature, supplying sufficient thermal budget for the post-bonding device processing and both are known materials in CMOS industry as they have been used as an inter-layer dielectric (ILD) in CMOS metallization stacks [108, 109].

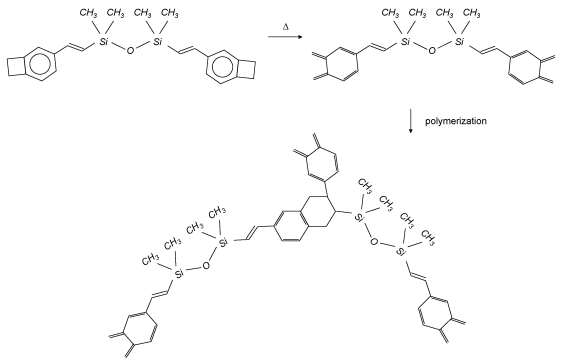


Figure 3.1: DVS-BCB polymerization reaction - no by-products are created upon cure

3.3.1 DVS-BCB properties

The divinylsiloxane-bis-benzocyclobutene (DVS-BCB) monomer is depicted in figure 3.1. It is a symmetrical molecule consisting of a silicon backbone terminated by two benzocyclobutene rings. The monomer can be B-staged, this means that it is partially cured to form an oligomer. An oligomer solution is made by adding mesitylene. The achievable layer thickness by spin coating of the solution is determined by the amount of mesitylene solvent added and the degree of polymerization of the oligomer in the solution. Upon curing, the benzocyclobutene ring thermally opens to form o-quinodimethane. This very reactive intermediate readily undergoes a so called Diels-Alder reaction with an available vinylsiloxane group, to form a three-dimensional network structure as is shown in figure 3.1 [110, 111]. As is clear from this reaction mechanism, no by-products are created during the polymerization.

Besides the oligomer solution, several adhesion promoter solutions were developed to improve the adhesion of the polymer to a wide range of surfaces. Adhesion promoter molecules for use with silicon wafers often have the generalized chemical formula G-Si(OR)$_3$ [112, 113], where R can be hydrogen, methyl, ethyl or other more complex groups. The resulting silanol group is understood to react with free hydroxyl groups on an oxidized surface. The G-group consists of a moiety with favorable interaction with the polymer. The operation of the simple adhesion promoter vinyltrihydroxysilane on an oxidized silicon surface is shown in figure 3.2.

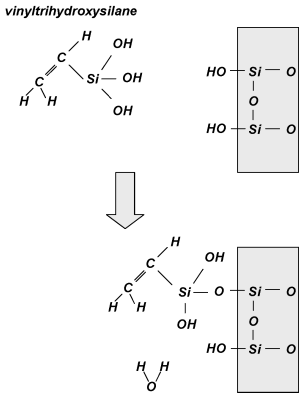


Figure 3.2: Adhesion promoter operation on an oxidized silicon surface

The electrical, optical, mechanical and thermal properties of DVS-BCB [110, 114] are listed in table 3.1. Most important for our application are the low optical loss at telecommunication wavelengths, the low shrinkage upon cure (as this can be the origin of void formation at the bonding interface), its high glass transition temperature (allowing a large post-bonding thermal budget) and its excellent planarization properties. From a device point of view, the major drawback is the low thermal conductivity, which will be discussed in chapter 6.

Upon curing, the DVS-BCB goes through some transformations at a rate, which depends on the temperature used for curing. This can be graphically represented in a time-temperature-transformation isothermal cure diagram as shown in figure 3.3. The main features of such a diagram are obtained by measuring the times to events to occur during isothermal cure at different temperatures. This includes the monitoring of the degree of polymerization and the onset of gelation and vitrification.

Gelation corresponds to the incipient formation of an infinite molecular network, which gives rise to long-range elastic behavior in the macroscopic fluid. It occurs at a definite degree of polymerization for a given system, according to Flory's theory of gelation [115]. After gelation, the material consists of normally miscible sol (finite molecular weight) and gel (infinite molecular weight) fractions, the ratio of the former to the latter decreasing with conversion.

Electrical properties	
Dielectric constant	2.5 at 10GHz
Dissipation factor	0.002 at 10GHz
Breakdown voltage	5.3MV/cm
Optical properties	
Refractive index	1.543 at 1.55μm
Optical loss	$<$ 0.1dB/cm at 1.55 μm
Mechanical properties	
Tensile modulus	2.9GPa
Intrinsic stress	28MPa
Tensile strength	89MPa
Poisson ratio	0.34
Shrinkage upon cure	0.05
Thermal properties	
Glass transition temperature	$> 350C$
Thermal expansion coefficient	42ppm/K
Thermal conductivity	0.29W/mK
Other properties	
Planarization	very good
Moisture uptake	very low

Table 3.1: Various properties of DVS-BCB (from [110] and [114])

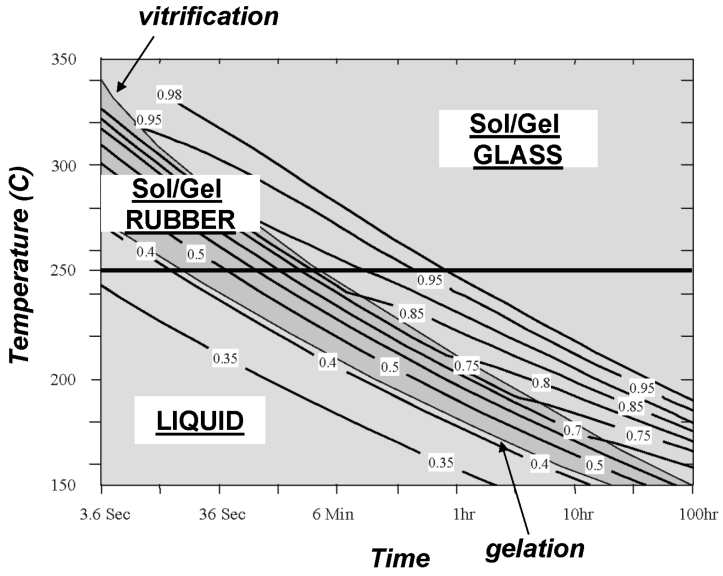


Figure 3.3: Time-Temperature-Transformation plot for DVS-BCB (from [110]) - the isothermal cure line at 250C is also shown

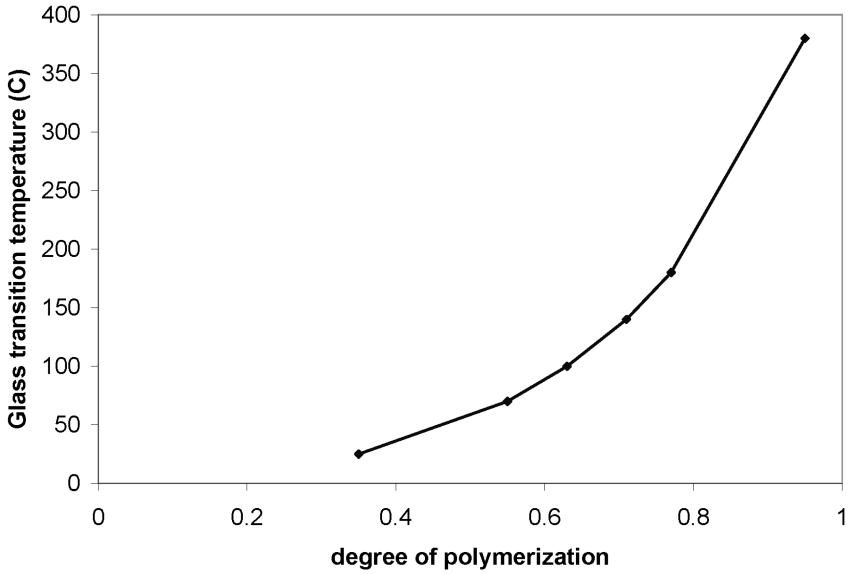
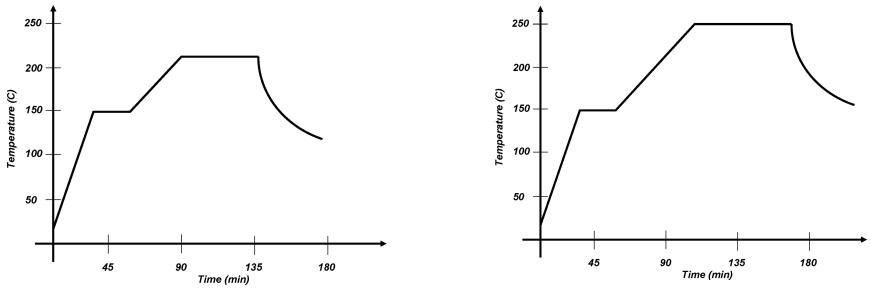


Figure 3.4: Glass transition temperature as a function of the degree of polymerization for DVS-BCB

Vitrification occurs when the glass transition temperature T_g rises to the isothermal temperature of cure. The material is liquid or rubbery when $T_{cure} > T_g$. It is glassy when $T_{cure} < T_g$. Vitrification retards further chemical conversion. The glass transition temperature can be defined as the temperature below which the molecules have little relative mobility. Above T_g, the secondary, non-covalent bonds between the polymer chains become weak in comparison to thermal motion, and the polymer becomes rubbery. Therefore, it can be understood that the glass transition temperature of a polymer increases with increasing degree of polymerization as shown in figure 3.4.

Two cure profiles for DVS-BCB are commonly used: a soft-cure process and a hard-cure process. The soft-cure process leads to a 75 percent polymerization of the DVS-BCB and a hard-cure process leads to a degree of polymerization higher than 95 percent. The curing ramps of the soft-cure and hard-cure process are depicted in figure 3.5. A maximum temperature of 210C for 40 minutes is used for soft-curing, while a maximum temperature of 250C for 60 minutes is used for hard-curing the DVS-BCB. The curing has to be performed in an atmosphere con-



(a) (b)

Figure 3.5: DVS-BCB soft-cure (a) and hard-cure (b) temperature profile

taining less than 100ppm oxygen, to prevent the oxidation of the DVS-BCB. To achieve this, nitrogen is purged through the curing chamber. The rapid thermal curing of DVS-BCB has also been reported in literature [110] using peak temperatures as high as 315C and cure cycle times lower than 5 minutes. Although this works fine for as deposited DVS-BCB layers, rapid thermal annealing of DVS-BCB used as a bonding agent, always resulted in delamination and failure of the bond in our experiments. This is probably related to the fact that an intimate contact between the DVS-BCB and the bonded die (through wetting) can only be achieved by slowly polymerizing the DVS-BCB. Therefore, we will no longer consider this rapid thermal annealing process for our application.

B-staged DVS-BCB solutions are formulated and commercialized by Dow Chemicals as the CYCLOTENE 3022 product series. It is photo-insensitive, but can be dry etched using a gas mixture of SF_6 and O_2 [116]. The commercially available layer thicknesses are shown in figure 3.6, ranging from 1μm to 25μm.

For some applications, thinner DVS-BCB layers are required. Therefore, in this work a custom DVS-BCB solution was formulated by adding mesitylene to the CYCLOTENE 3022-35. The effect of this dilution on the layer thickness is shown in figure 3.7, in which the resulting layer thickness for a spin speed of 5000rpm is plotted as a function of the amount of added mesitylene [117]. The use of strongly diluted solutions requires ultrasonic agitation prior to application to obtain reproducible layer thicknesses.

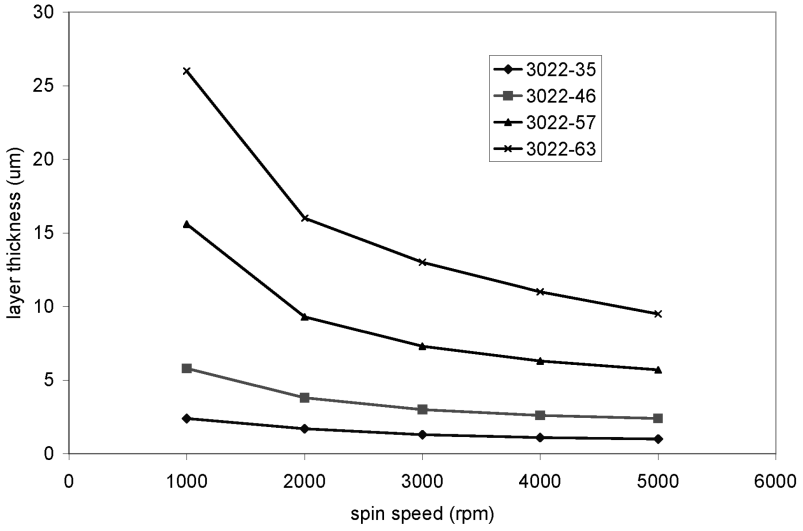


Figure 3.6: Commercially available DVS-BCB formulations and layer thicknesses

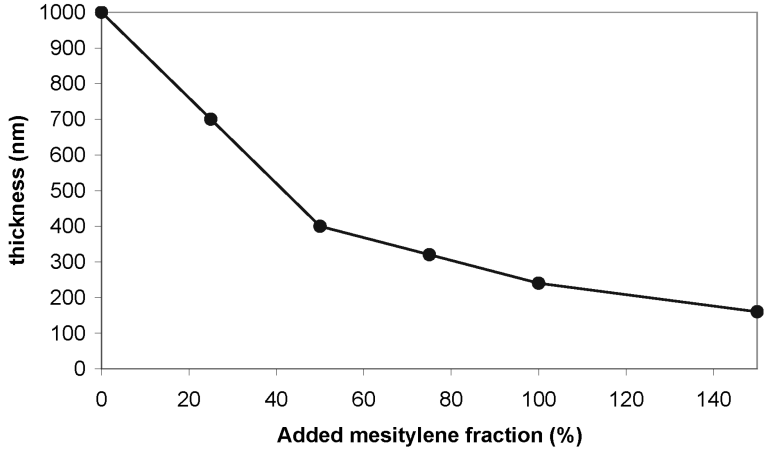


Figure 3.7: Influence of the degree of dilution of the DVS-BCB on the resulting layer thickness when spin coated at 5000rpm

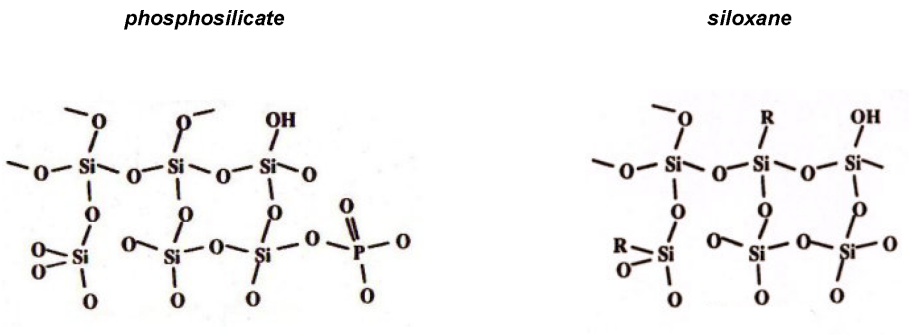


Figure 3.8: Phosphosilicate and siloxane spin-on glass

3.3.2 Spin-on glass properties

Different types of spin-on glass are formulated and are commercially available. The basic silicate SOG forms a strong Si-O network after curing. The large film shrinkage upon cure creates a high tensile stress, which may lead to a cracking problem. In order to obtain an OH free network, high curing temperatures (800C-900C) are needed. Silicate SOG may be doped with phosphorus, which modifies the Si-O network. This reduces the film stress, which helps against the cracking problem. A phosphosilicate SOG network is shown in figure 3.8.

The organosilicon compound SOG or siloxane SOG contains organic dopants (R groups in figure 3.8) to modify the Si-O network. This also lowers the film stress. The viscosity and molecular weight are slightly higher than that of the silicate SOG. This means that films are thicker and its planarization properties are better. In order to avoid thermal decomposition of the organic groups, curing temperatures must be kept low (typically 400C). Increasing the organic content will further reduce the film stress and improve the crack resistance and planarity. However, it was found that the mechanical strength of this material is low.

Besides the SiO_2-based compounds, a class of boron compound spin-on glasses were developed. This class of materials is often used for diffusion applications in which the dopant-organic compound decomposes on heating and the boron diffuses into the silicon substrate onto which the dopant-organic compound was spin coated, to act as an acceptor.

Sol-gel coating technology is applied to deposit the SOG layers onto a substrate. A sol-gel process involves a solution (single phase liquid)

that undergoes a sol-gel transition after which it has become a rigid, porous mass. This transition is mostly achieved by simple spin coating of the SOG, after which a rigid two-phase system of solid and solvent-filled pores is formed on the substrate. This is called a two-phase alcogel. Once through the sol-gel transition, the solvent phase is removed by evaporation, to create xerogels. At this point, the gel is a microporous oxide. By heating, the tacky gel is transformed into a hard gel. The hard gel may be heated to various degrees of collapse of the microporous structure.

The Honeywell Accuglass T11-311 methylsiloxane spin-on glass was chosen for our experiments. A layer thickness of 250nm can easily be achieved by spin coating. The T11-311 SOG has a cracking resistance up to 600nm as it is a siloxane SOG with a high organic content (it contains 10 weight percent CH_3 groups bonded to Si atoms in the Si-O backbone). It has good planarization properties, as it was especially formulated for use as an inter-level dielectric for electronic integrated circuits. Narrow gaps (down to 0.3μm wide and with an aspect ratio of 4) are filled without void generation while planarizing multi-level metal stacks. The SOG is fully cured at 400C for 1 hour.

3.4 Planarization by adhesives

3.4.1 Planarization behavior

As stated in chapter 2, one of the advantages of adhesive bonding is the fact that by spin coating the adhesive onto the host substrate, planarization of the topography (be it an intentional topography or the presence of particles) can be obtained without using chemical mechanical polishing techniques. The degree of planarization that can be obtained using an adhesive depends on the adhesive layer thickness, the ability of the adhesive to flow upon curing, the molecular weight of the oligomer (determining the film viscosity) and the shrinkage upon cure [118]. In order to characterize and model the planarization behavior of DVS-BCB, in this work DVS-BCB was spin coated onto an isolated step in a topography and the resulting DVS-BCB topography was measured. By differentiating this function, a one-dimensional impulse response function can be derived, which can be used to simulate the planarization behavior of a one-dimensional topography by convoluting this impulse response with the topography function. The impulse response function for a topography of 220nm high and for two types

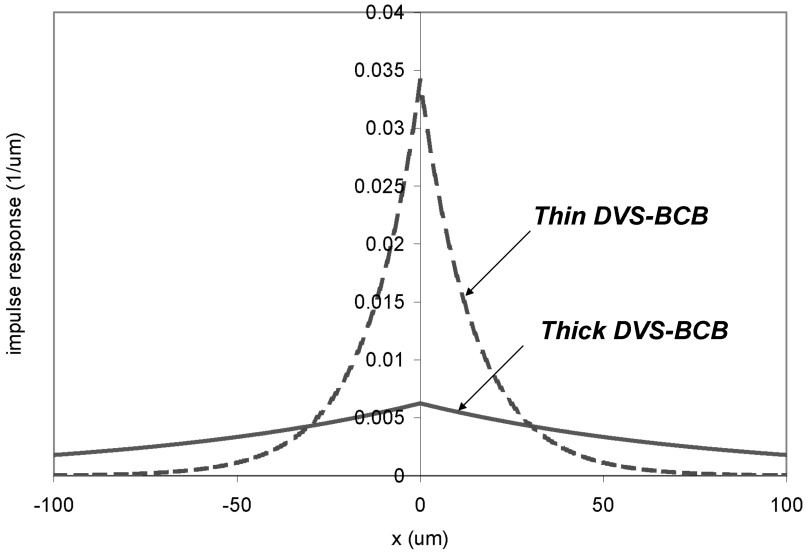


Figure 3.9: Impulse response of the DVS-BCB spin coating process for a topography of 220nm high

of DVS-BCB coating (a CYCLOTENE 3022-35 solution spin coated at 5000rpm resulting in a layer thickness of 1μm, referred to as "thick DVS-BCB" and a double layer coating of a DVS-BCB:Mesitylene 2:3 solution, spin coated at 5000rpm, with an aggregate layer thickness of 300nm, referred to as "thin DVS-BCB") is shown in figure 3.9. The impulse response functions are symmetrical and consist of two exponentially decaying tails. The higher degree of planarization of the thick DVS-BCB layer is clear from this figure. By Fourier transformation of the impulse response function we obtain the low pass filter response characteristic of the DVS-BCB spin coating process. This filter function is shown in figure 3.10 for the double layer coating process ("thin DVS-BCB").

The two-dimensional impulse response function can however not be derived from a step response, as there is no unique two-dimensional impulse response function to match the step response function, even with the restriction of circular symmetry [87]. Another approach is to determine the fourier transform of the impulse response function by taking the ratio of the fourier transform of the topography after planarization and the fourier transform of the topography before spin

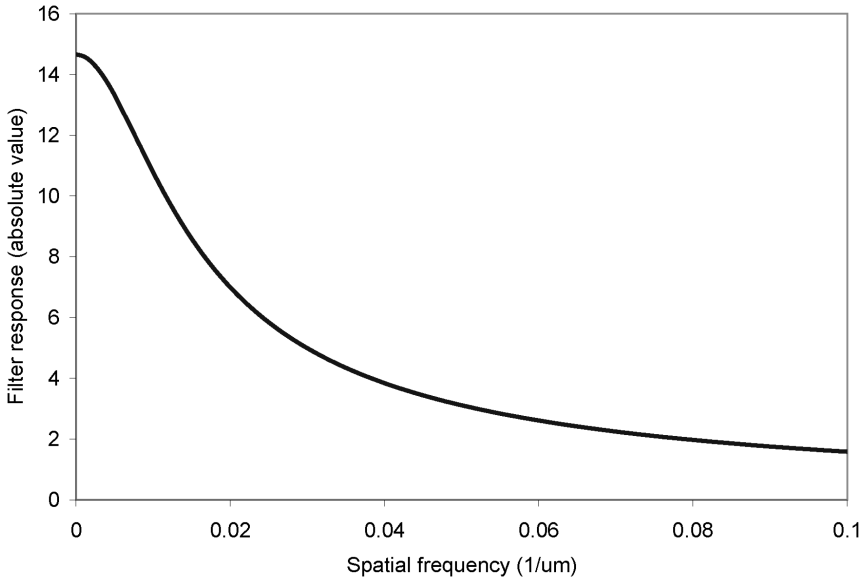


Figure 3.10: Filter characteristic of the ”thin DVS-BCB” spin coating process for a topography of 220nm high

coating. However, this is difficult to carry out directly, as the layout of the topography rarely is rich enough to avoid zeros in the fourier transform of the original topography [87]. Therefore, the approach adopted here, is to consider a circular symmetric function with exponentially decaying tails, in which we choose the decay constant to match the one-dimensional step response.

The planarization of two types of topography was simulated using this approach, as shown in figure 3.11, for the two DVS-BCB coating processes studied. While the first topography is relatively complex, the second topography consists of 10μm wide and 220nm deep trenches on a pitch of 30μm and 120μm. A cross-section of the simulation result for the second type of topography and the double coating process (indicated by the dashed line) is shown in figure 3.12, revealing a local degree of planarization of 90 percent for 10μm wide 220nm deep trenches on a 30μm pitch and a local degree of planarization of 70 percent for the same trenches on a pitch of 120μm. These simulation results will be compared with experimental measurements in section 3.6. As

can be seen from the simulated cross-section, no global planarization is obtained.

The obtained impulse response functions in figure 3.9 should be compared to the impulse response function obtained for chemical mechanical polishing. This impulse response function was derived in [87], where it was shown that the effective pattern density needed for calculating the local polishing speed (and thereby determining the degree of planarization), as was discussed in section 2.4.6, is obtained by convoluting the real pattern density with an elliptic impulse response function, with a planarization length (being the full width at half maximum of the impulse response function) of 1 to 3mm, depending on the process. Comparing this with the typical planarization lengths obtained by adhesive spin coating (typically a few tens of microns) it is clear that it is more likely to obtain global planarization using a CMP process than with a spin coating process. However, by carefully designing the original topography, locally a high degree of planarization can be obtained using a spin coating process (e.g. the 10μm trenches on a pitch of 30μm in figure 3.12).

3.4.2 Gap closing

During die-to-wafer bonding, each substrate is elastically deformed to achieve conformity of the two substrates. Non-perfect planarization can be compensated by this gap closing effect. The height of the gaps h that can be closed depends on their period $2R$, the bonding energy γ and the biaxial Young's modulus of the substrates E' (it is not dependent on the thickness of the wafers if the spatial period $2R$ is lower than the total thickness of the wafer stack) and was derived in [84] to be given by

$$h < 3.5 \left(\frac{R\gamma}{2} \right)^{1/2} (\frac{1}{E'_1} + \frac{1}{E'_2})^{1/2} \tag{3.1}$$

with E' the biaxial Young's modulus.

Equation 3.1 is schematically shown in figure 3.13 for a InP/silicon wafer pair bonded with a bonding energy of 30mJ/m^2. In the case of adhesive bonding, the adhesive can still deform, which results in even larger gap heights that can be closed.

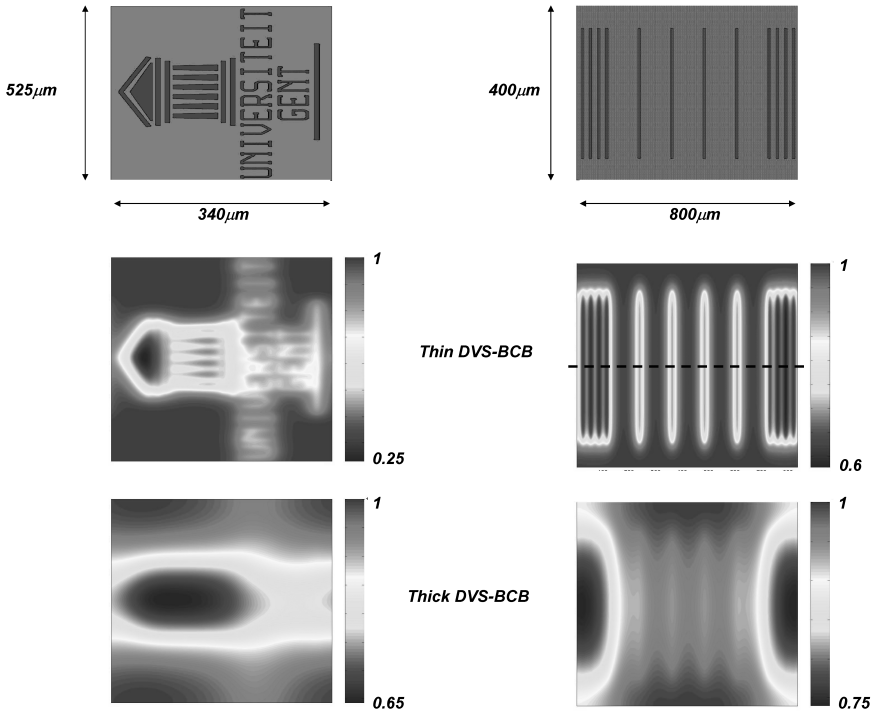


Figure 3.11: Simulated topography profile after planarization using DVS-BCB (220nm high topography)

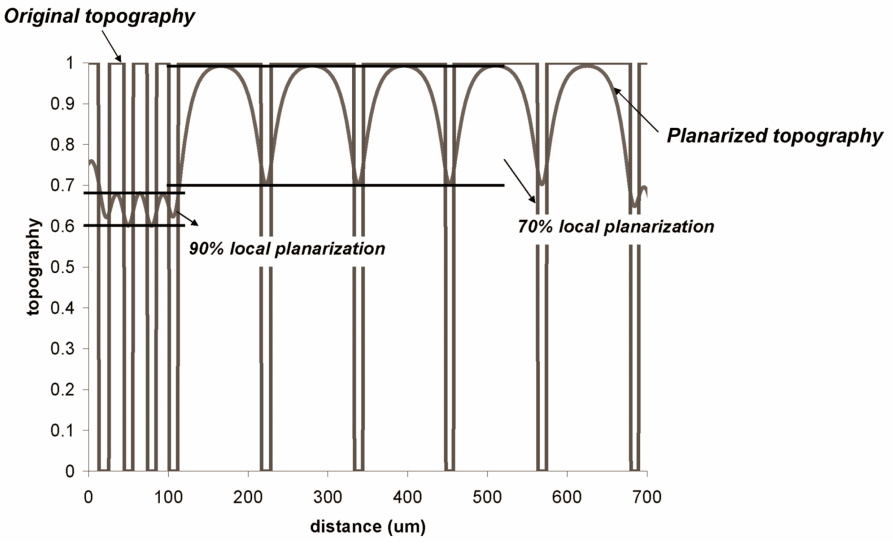


Figure 3.12: Cross-section of the simulated trench profile after planarization by ″thin DVS-BCB″

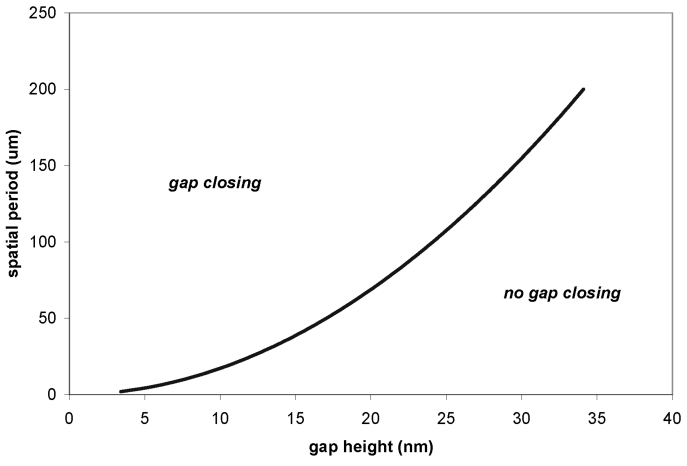


Figure 3.13: Gap closing condition

3.5 Standard DVS-BCB bonding process development

3.5.1 Standard DVS-BCB bonding

Standard DVS-BCB bonding is defined as the bonding process involving bonding layers that can be achieved using the commercially available CYCLOTENE series. It concerns layer thicknesses ranging from 1μm to 25μm. For these thicknesses, planarization of a topography of 220nm height is less a cause for concern and the quality of the surfaces to be bonded (i.e. the presence of particles at the bonding interface) can be relaxed.

3.5.2 Surface preparation

Although, as discussed above, the required quality of the surfaces to be bonded can be relaxed, it is always good practice to clean the wafer surfaces prior to bonding. Especially large particles and chips can occur on the surface due to cleaving or dicing of the dies. Moreover, hydrocarbon contamination (due to storage in plastic boxes and exposure to air) on the die surface can reduce the adhesion of the DVS-BCB and thereby decrease the bonding strength.

The cleaning of the substrate depends on the type of substrate. Hydrocarbon contamination can be removed from the silicon-on-insulator dies by immersing the sample in a Piranha solution, a warm mixture of $3H_2SO_4$:$1H_2O_2$. The mixture is a strong oxidizer and will remove most organic matter and leave the surface hydrophilic. In a second step particles can be removed by using a Standard Clean 1 solution, as explained in section 2.4.6. After surface cleaning, the commercially available adhesion promoter AP3000 is applied by spin coating.

In this work it was found that the cleaning of the InP/InGaAsP dies can best be done by removing a pair of sacrificial InP/InGaAs layers by selective wet etching using 3HCl:H_2O and $1H_2SO_4$:$3H_2O_2$:$1H_2O$ respectively. This etch lifts off foreign particles and etches down and lifts off InP/InGaAsP particles, created by the cleaving or dicing operation. This will be explained in more detail in section 3.6. No adhesion promoter is applied to the III-V surface, as this would require spin coating of the individual cleaved dies, which is very time intensive and leads to the formation of an edge bead. Instead, the effect of immersing the dies prior to bonding in various chemicals or applying a plasma treatment (which can be a collective process) on the bonding strength was

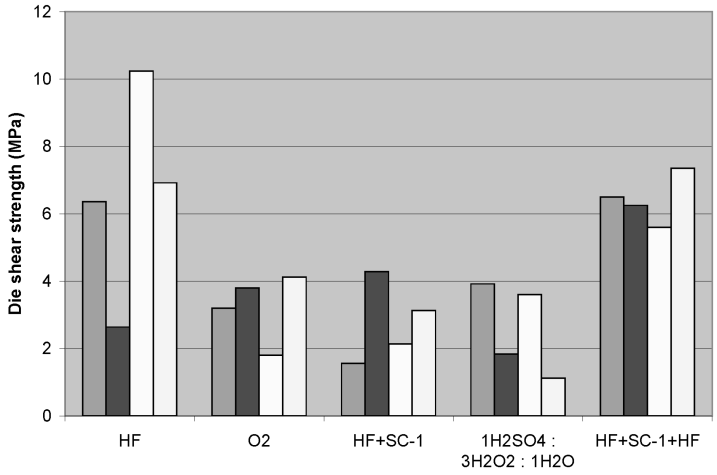


Figure 3.14: Surface conditioning of InP dies for DVS-BCB bonding: bonding strength optimization

assessed here. Note that, as InP has a polar interface, the adhesion to this surface is in general better than to a non-polar surface.

The results of this experiment are shown in figure 3.14, in which the die shear strength of a bonded die for various surface treatments is plotted. The measurement method is outlined in section 3.8. From this measurement, it is clear that the HF treatment of the InP surface, which renders the surface hydrophilic, gives the highest bonding strength. This is due to a change in the chemical state of the surface, as can be seen by comparing the results of the HF, HF+SC-1 and HF+SC-1+HF treatment, and not due to an additional particle removal effect.

3.5.3 DVS-BCB precure

After surface cleaning and conditioning, the DVS-BCB is deposited on the silicon-on-insulator wafer surface by spin coating. Although most of the mesitylene solvent already evaporated during the spin coating process, some solvent is still remaining in the spin coated film, which is evaporated by a thermal treatment at 150C for 1 minute. This thermal treatment also causes a reflow of the DVS-BCB, which improves its planarizing properties.

3.5.4 Sample attachment

After cleaning, surface conditioning and thermal treatment of the DVS-BCB layer, both samples are to be brought into contact. Attachment is done at 150C, as DVS-BCB has about the lowest viscosity at this temperature [107] and keeping the DVS-BCB at this temperature nearly doesn't increase the degree of polymerization for at least an hour (see figure 3.3).

Attachment can be done in several ways. In this work, samples were initially attached manually using tweezers. This approach has several drawbacks: the alignment of the die to the host substrate could only be done with 500μm precision. Often there were air bubbles trapped at the bonding interface (reducing the bonding yield) and the handling with tweezers damaged the die to be bonded. The problem of air trapped at the bonding interface was solved in this work, by etching trenches in the die to be bonded, as is shown in figure 3.15. Air gets only trapped inside the trenches (due to a slight shifting of the sample also DVS-BCB got trapped in the trenches, resulting in air bubbles surrounded with DVS-BCB), while the rest of the bonding interface is void free.

The alignment problem was tackled in this work by using a mask aligner setup to accurately attach both dies. Alignment accuracy of 50μm can easily be achieved. The setup is shown in figure 3.16(a). The sample to be bonded is temporarily fixed to a glass carrier and the host substrate lies on a translation stage allowing accurate alignment. Once the dies are aligned, they are brought in contact. The biggest issue with this kind of approach is the influence of the wedge error due to the fact that both surfaces are not perfectly parallel. This nearly always results in an unbonded area.

In order to avoid the wedge error problem and to avoid the inclusion of air on planar substrates, a vacuum bonding tool was developed in this work, which is depicted in figure 3.16(b) and 3.17. Using this tool, good quality bonding could be obtained with limited alignment accuracy. However, as we will show in section 3.10, an alignment accuracy of a few tens of microns should be obtainable, using a slightly adapted bonding tool. The operation principle of the vacuum bonding tool is depicted in figure 3.16. The die to be bonded to the host substrate is temporarily attached to a flexible silicone membrane, while the host substrate is positioned on a heated chuck. By evacuating the bonding chamber, the flexible silicone membrane deforms and both samples are contacted in a low vacuum environment using a uniform pressure of 1

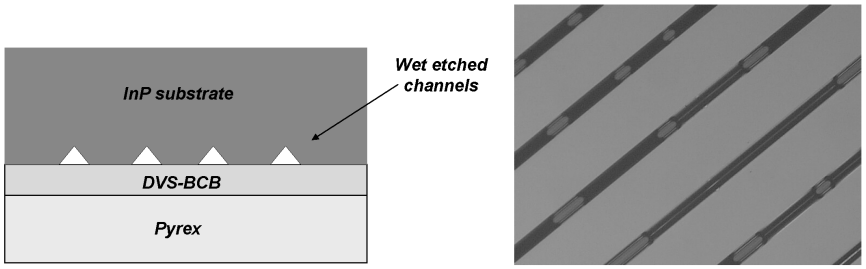


Figure 3.15: Bonding of a sample with etched trenches - cross-sectional view and optical inspection of the bonding interface

bar. When a higher bonding pressure is wanted, excess nitrogen can be purged in the nitrogen pressure chamber.

The use of a flip-chip process to bond the dies was not investigated, due to the fact that no machines are currently available, which allow bonding in a vacuum environment. The wedge error problem and alignment accuracy are however no longer a concern in this approach. An alternative approach based on temporary gluing of the dies will be discussed in section 3.10.

3.5.5 Curing

After sample attachment, the DVS-BCB needs to be cured. As stated in section 3.3.1, several curing programs can be chosen. When using rapid thermal annealing, delamination of the InP/InGaAsP film occurs when removing the InP substrate, indicating a low quality bonding. The soft-curing process only partially polymerizes the DVS-BCB (to about 75 percent), which reduces the glass transition temperature to about 200C, thereby limiting the post-bonding thermal budget. Better stability (a glass transition temperature over 350C) and mechanical properties are obtained by completely polymerizing the DVS-BCB. Therefore, we chose to use the hard-cure process to cure the DVS-BCB.

3.5.6 Substrate removal

After bonding of the InP/InGaAsP die, the InP substrate needs to be removed, to be able to access and process the InP/InGaAsP epitaxial layers. The InP substrate can be removed by complete wet chemical etch-

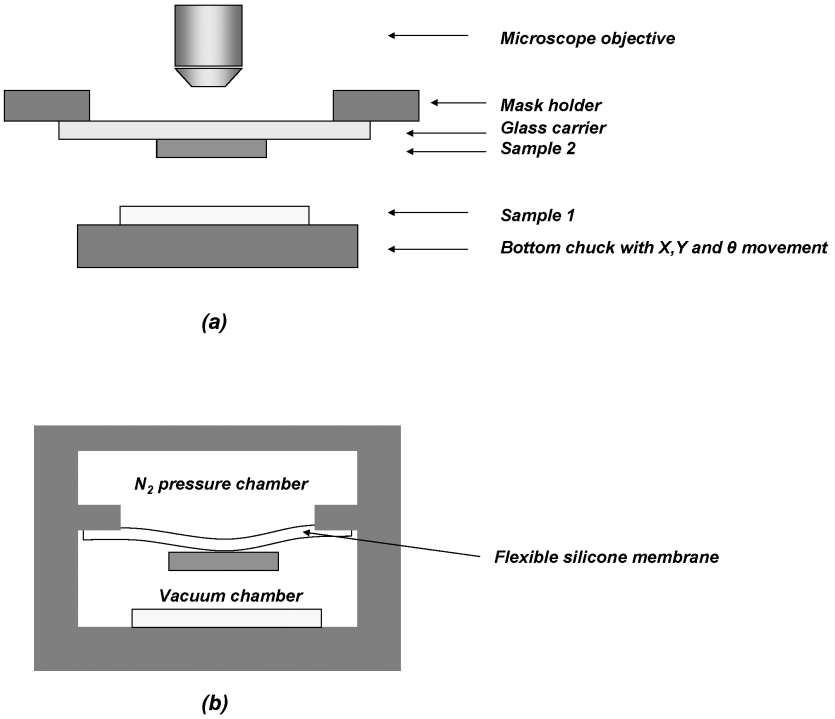


Figure 3.16: Sample attachment using a mask aligner setup or a vacuum bonding setup

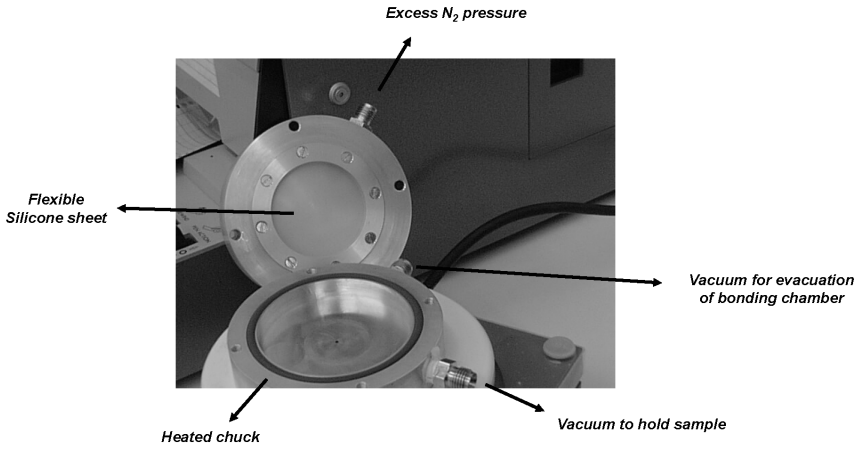


Figure 3.17: In-house made vacuum bonding setup

ing or by using a combination of mechanical grinding and wet chemical etching.

Complete chemical etching can be done using a mixture of HCl and H_2O. The chemical reaction that occurs during InP substrate removal is given by

$$InP + 3HCl \rightarrow InCl_3 + PH_3 \uparrow \tag{3.2}$$

The measured etch rate is plotted in figure 3.18. High etch rates can be obtained by using pure HCl. Although this leads to the shortest etching time, the use of pure HCl should be avoided, as the etching is vigorous and lots of gas bubbles are created. These can stick to the substrate and thereby mask the etching, which causes etching inhomogeneity. A good compromise between etching speed and etching quality is to use a 3HCl:1H_2O mixture. An InGaAs etch stop layer can be used, which shows nearly complete etching selectivity to InP [92].

It was found in this work however, that an important drawback of complete chemical etching using a HCl:H_2O etching solution is the arising of unetched ramps at two sides of the cleaved InP die due to the exposure of the (112) crystallographic plane, which forms an angle of about 35 degrees with the surface [119]. This is due to the fact that HCl is an anisotropic etchant and doesn't etch an exposed (0 1 -1) plane [120]. This plane is exposed by the cleaving of the dies. The origin of the ramps is graphically explained in figure 3.19 and a SEM cross-section of a ramp on a bonded substrate is shown in figure 3.20.

These ramps prohibit the contact between the mask and sample in the post-processing lithography, making the definition of fine features difficult for contact lithography.

As no isotropic but selective etching solution for InP is known, a combination of isotropic non-selective etching and anisotropic selective etching can be used to avoid the formation of the ramps. We successfully used a combination of HNO_3:HCl and 3HCl:H_2O to avoid the formation of the ramps. Good timing for changing the etch bath is needed in order to prevent the etching of the InP/InGaAsP epitaxial layers by the non-selective HNO_3:HCl etchant.

Besides the formation of ramps on two sides of the bonded die, undercutting of the epitaxial layer structure may occur on the other two sides, as will be shown in section 3.8. The length of the undercut zone depends on the etching time and therefore on the thickness of the original substrate. To reduce this undercut length and to reduce the height

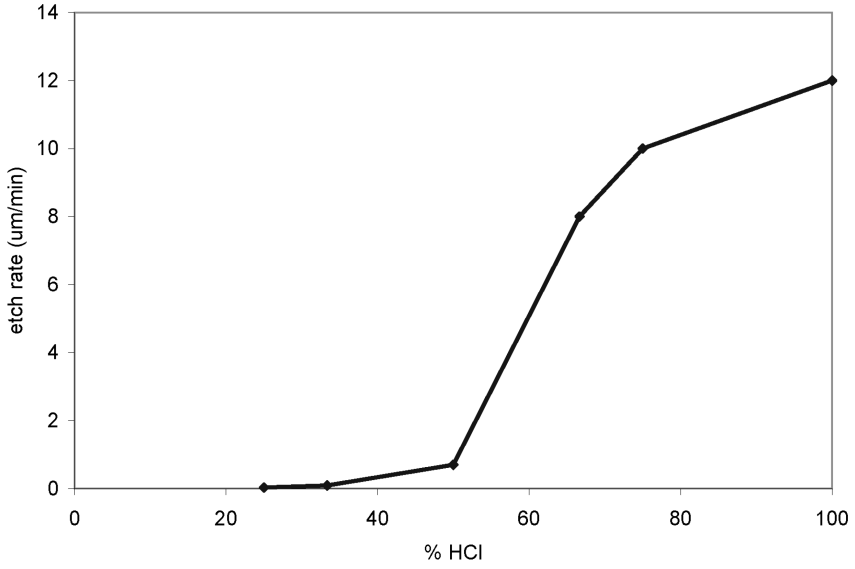


Figure 3.18: InP etch rate of a HCl:H_2O mixture at room temperature as a function of the volume percentage HCl in the etchant

of the formed ramps, we propose a combination of mechanical grinding and wet chemical etching to remove the InP substrate.

The mechanical grinding is performed by using a slurry consisting of a 10μm AlO_x powder suspension. The InP substrate is mechanically thinned to about 70μm. As the InP is very brittle, special precautions have to be made to prevent the formation of cracks. A thorough cleaning and preconditioning of the polishing pad is needed to prevent the presence of hard particles on the polishing platen, which can cause scratches in the InP substrate. As this mechanical grinding also slightly grinds the sides of the InP dies (illustrated by the chipping occurring in figure 3.20), no longer a pure crystallographic plane is exposed, which in turn reduces the height of the formed ramps (contrary to the case of complete chemical etching where the height of the ramps matches the original substrate height).

After mechanical grinding, the sample is cleaned to remove residual slurry and the thinned die is further chemically etched using 3HCl:1H_2O or a combination of 3HCl:H_2O and HCl:HNO_3.

Another way to avoid the formation of ramps is to saw the InP dies instead of cleaving them, thereby not exposing a crystallographic

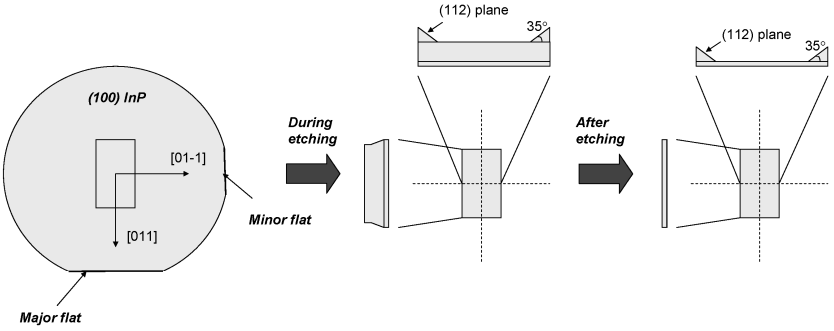


Figure 3.19: Anisotropic etching during chemical substrate removal

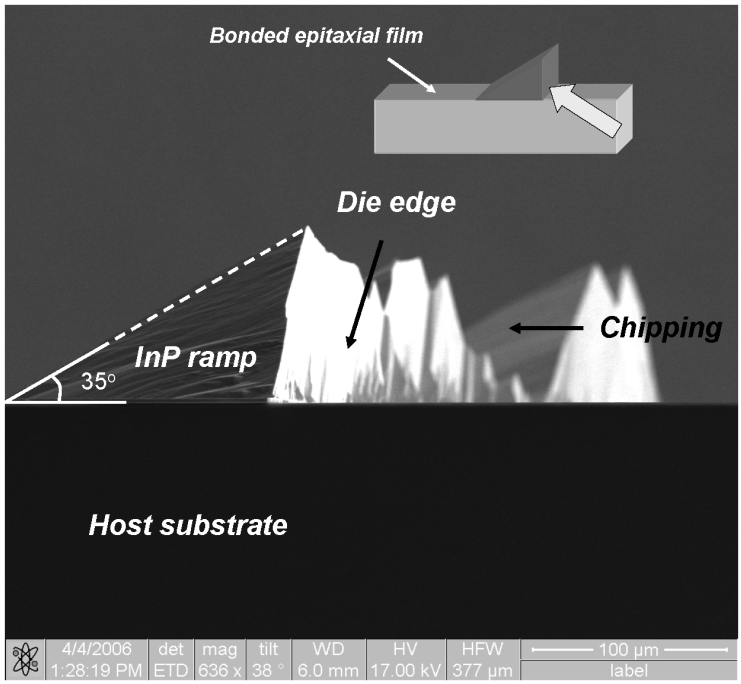


Figure 3.20: Ramp formation at the edge of a bonded die due to anisotropic wet etching of the InP substrate

Figure 3.21: Top view and cross-section of samples bonded using a thick DVS-BCB layer

plane. Eventually, still some ramp formation can remain, therefore the use of mechanical grinding is advisable.

3.5.7 Bonding results

A top view and a cross-sectional view of InP/InGaAsP epitaxial layers transferred to a processed and unprocessed substrate respectively, are shown in figure 3.21. In the top view image, the ramp formation at two sides of the die is visible. Void free bonding was obtained with die sizes up to 1cm^2. Due to the cost of the epitaxy, experiments with larger dies were not carried out.

3.6 Ultra-thin DVS-BCB bonding process development

3.6.1 Ultra-thin DVS-BCB bonding

Ultra-thin DVS-BCB bonding is defined as the bonding process involving bonding layers that are less than 500nm thick. These layer thicknesses cannot be achieved using commercially available CYCLOTENE and need to be formulated by dilution with mesitylene. For these thicknesses, planarization of a topography of 220nm height becomes a cause

of concern and the presence of particles at the bonding interface can be detrimental.

3.6.2 Degree of polymerization

For ultra-thin DVS-BCB layers, we found that the degree of polymerization prior to bonding is an important issue. From the time-temperature-transformation diagram in figure 3.3, it is clear that after application of the DVS-BCB it is still in the liquid phase. Attaching the die to be bonded to the host substrate can cause puncturing of the ultra-thin DVS-BCB layer and thereby cause delamination during InP substrate removal. By increasing the degree of polymerization, we can transform the liquid DVS-BCB layer into a sol/gel rubber or even into a sol/gel glass prior to bonding, as explained in section 3.3. We found that transforming the DVS-BCB to a sol/gel rubber, increases the rigidity of the DVS-BCB, thereby dramatically reducing the chance of puncturing the bonding layer. When the degree of polymerization has increased too much, a sol/gel glass is formed and the bonding layer is no longer sufficiently tacky (as it no longer is able to wet the InP surface), leading to sample detachment after contacting.

The degree of polymerization versus time at 250C is plotted in figure 3.22, illustrating the phases of the DVS-BCB layer and the resulting bonding quality obtained from our experiments. From these results we selected an optimal pre-bonding polymerization of 2 minutes at 250C (indicated by the box in figure 3.22). Again, this pre-polymerization has to be performed in a nitrogen ambient to prevent the oxidation of the DVS-BCB.

3.6.3 Degree of planarization

As was discussed in section 3.4, the ability of planarizing a topography depends both on the topography height and topography density of the substrate. In order to get a better understanding of the influence of the way the adhesive is applied to the substrate on its planarization properties, two types of topography were investigated in this work. A first topography (hereafter referred to as topography A) consists of 10 μm wide and 220nm deep trenches on a pitch of 30μm, while a second topography (hereafter referred to as topography B) consists of the same trenches, but on a pitch of 120μm. Four types of adhesive spin coating processes were used to planarize both topographies and the resulting degree of planarization was measured as shown in table 3.2. A single

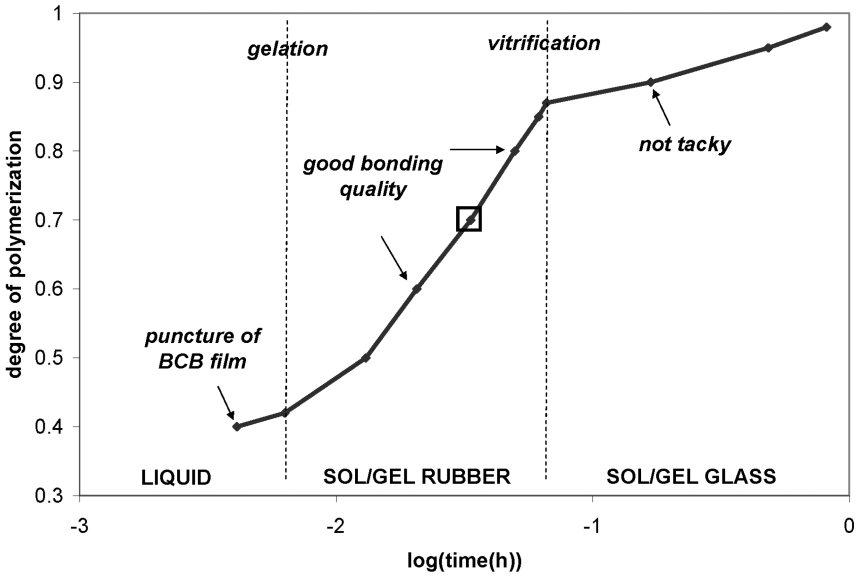


Figure 3.22: DVS-BCB precure optimization - degree of polymerization versus time at 250C

	topography A	topography B
150nm DVS-BCB (ramped)	0.84	0.66
150nm DVS-BCB (ramped) + 150nm DVS-BCB (ramped)	0.95	0.8
150mn DVS-BCB (ramped) + 150nm DVS-BCB (RTA)	0.91	0.75
thick DVS-BCB layer	0.925 (760nm)	0.945 (1μm)

Table 3.2: Degree of planarization of topography A and B for various DVS-BCB coating processes

DVS-BCB layer of 150nm, a double DVS-BCB layer with an aggregate thickness of 300nm and a thick DVS-BCB layer was used, the thickness of which is indicated in the table. The curing process was also varied: both a ramped soft-cure process (1.6C/minute to 210C and a dwell of 40 minutes) and a rapid thermal annealing (2 minutes at 250C) were used. The degree of planarization for both topographies is listed in table 3.2.

From these measurements several conclusions can be drawn. First, it is clear that the planarization of the 30μm pitch features is better than that of the 120μm features. Secondly, the superior planarization properties of double spin coated layers is clear: in the case of a 30μm pitch, even a higher degree of planarization can be obtained using an aggregate 300nm DVS-BCB layer than with a single 760nm thick DVS-BCB layer. The type of curing of the spin coated layer also plays a role.

Soft-curing the DVS-BCB by slowly ramping (indicated by "ramped" in table 3.2) gives a higher degree of planarization than a rapid thermal anneal (2 minutes at 250C) due to the reflow of the DVS-BCB in the case of slow ramping.

We can also compare these results with the simulation results obtained in section 3.4 for the case of a double layer spin coating process (first layer ramped curing and second layer rapid thermal annealing) on a topography, which corresponds with topography A and B. Simulation results (a local degree of planarization of 90 percent and 70 percent) and the experimentally measured values (91 percent and 75 percent) for topography A and B respectively are in good agreement, indicating that the simulation model described in section 3.4 can be used to predict in first order the resulting non-planarity after spin coating. It needs to be pointed out that when using the liquid DVS-BCB instead of the sol/gel rubber DVS-BCB, upon bonding a self planarizing effect can occur: by simply attaching the InP die, the liquid DVS-BCB can redistribute to completely planarize the topography. However, as discussed above, this is not a reproducible process due to the possibility of puncturing the DVS-BCB film upon attachment.

3.6.4 Bow and warp of substrates

Besides the influence of non-planarity of the DVS-BCB bonding layer, one also has to take into account the influence of the bow and warp of the substrates. The bow and warp of a substrate is defined in figure 3.23. It typically concerns a long-range waviness (multiple cm phenomenon) induced by imperfect polishing of the wafers or wafer bowing, due to the stress induced by deposited or grown layers. As the DVS-BCB is a sol/gel rubber, it is not as compliant with height variations compared to the case of liquid DVS-BCB. Therefore, no self planarization will occur and the substrates need to be elastically deformed to accommodate the waviness. Therefore, it was found in this work that the application of pressure during bonding, to intimately contact both substrates, is required. This pressure can also elastically deform the adhesive to allow better gap closing as discussed in section 3.4.2.

3.6.5 Particles

As bonding layer thicknesses are below 500nm, the presence of particles at the bonding interface is more critical than in the case of the standard DVS-BCB bonding process.

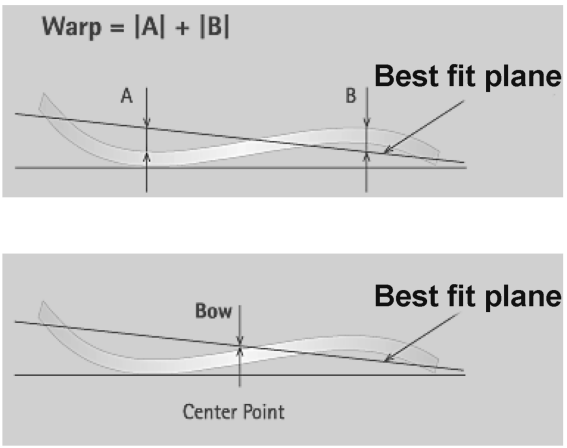


Figure 3.23: Definition of warp and bow of a substrate

Several causes for particles can be identified. Particles can be incorporated in the layer structure during the epitaxial growth process, airborne particles can fall onto the sample surface, the cleaving or sawing of the dies is a large source of particles and finally tweezer handling of the dies can create additional particles by scratching of the surface.

The bonding defect diameter as a function of particle size was calculated in section 2.4.2, for the case of direct wafer bonding. This analysis remains valid for the case of adhesive wafer bonding, if we decrease the particle height by subtracting the bonding layer thickness when the particle is higher than the bonding layer. This function is plotted in figure 3.24 for various bonding energies in the case a Pyrex (500μm thick) and silicon (750μm thick) wafer are to be bonded. From optical inspection, we can deduce the experimental defect radius and the height of the particle can be obtained by measuring the Newton interference fringes originating from the air wedge formed by the bonding defect, as will be explained in section 3.8. By plotting these experimental values on the theoretical curves we can obtain the bonding energy of the DVS-BCB bonding process, which is about 30mJ/m^2. This is substantially lower than in the case of direct wafer bonding (typical bonding energy in the range of 100mJ/m^2 to 2000mJ/m^2) and is related to the difference in bonding mechanism. While the direct bonding of an annealed wafer pair relies on a covalent bond with large bonding energy and a large number of bonds per unit area, adhesive bonding relies on

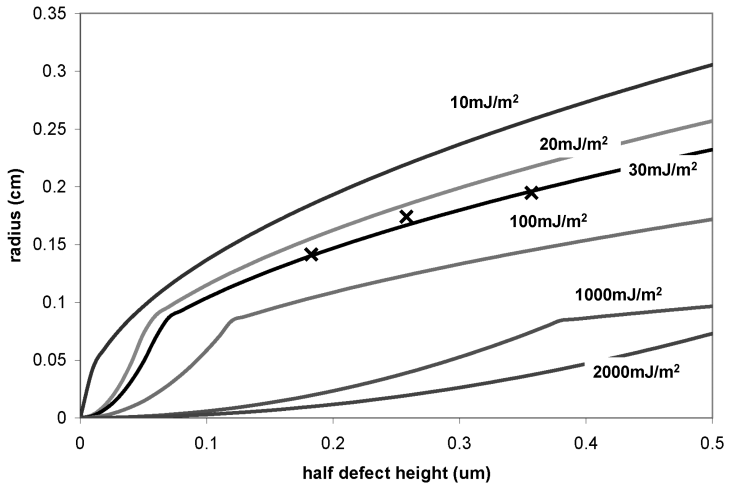


Figure 3.24: Bonding defect radius as a function of particle height - measurements for a silicon wafer bonded to Pyrex

the weaker dipole-dipole Van der Waals bonding as is shown in figure 3.25, in which the energy diagram of a covalent bond and a van der Waals dipole-dipole bond is plotted. Both curves in figure 3.25 reach a minimum, the depth of this minimum determining the bond energy, while the position of the minimum is determining the equilibrium distance between the attracted bodies.

The particle problem gets worse when considering small dies as explained in figure 3.26. When the bonding defect size due to the particle exceeds the dimensions of the die, no bonding occurs and the die remains partially unbonded, even when after curing (through the increase of the bonding energy) the hypothetical defect size is smaller than the dimensions of the die.

From the discussion above, it is obvious that particles need to be avoided. Therefore, we will outline the procedure for sample treatment prior to bonding we developed. Upon receiving the InP/InGaAsP epitaxial wafer, the areas containing incorporated particles are recognized through microscope inspection and neglected for further processing. After determination of the high quality epitaxy areas, dies are cleaved and temporarily glued to a host substrate (epi-side up), for example using photoresist, while paying attention not to damage the epitaxy during tweezer handling. After temporary die attachment, the die can be handled using the larger host substrate without affecting the die to

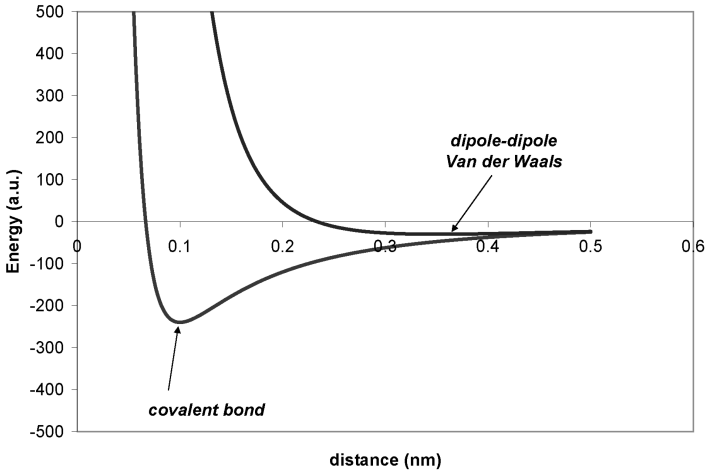


Figure 3.25: Energy of a covalent bond versus a Van der Waals dipole-dipole bond

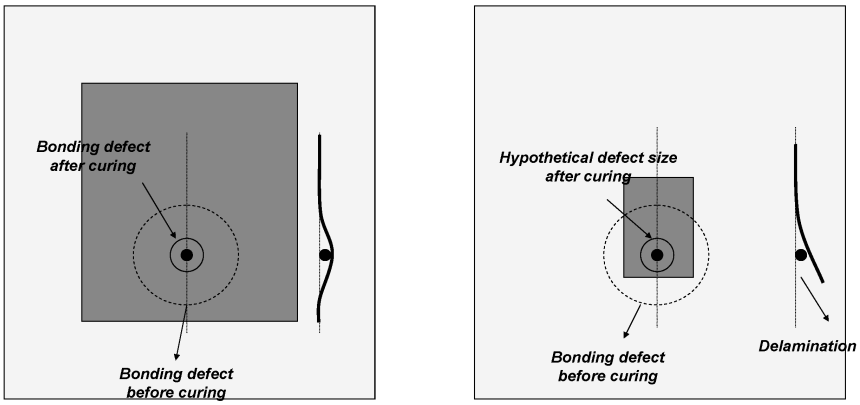


Figure 3.26: Die delamination mechanism

be bonded. As we will discuss in section 3.10, this approach can also enable the extension of the bonding process to multiple-die bonding.

Several wet cleaning methods were investigated in this work to remove the unavoidable particles at the bonding interface. Best results were obtained by sacrificial etching of an InP/InGaAs layer pair using 3HCl:H_2O and H_2SO_4:$3H_2O_2$:H_2O respectively. The particle removal efficiency was assessed by comparing the wafer surfaces before cleaning and after cleaning, using SEM inspection. The results of two types of cleaning are shown in figure 3.27. The use of an SC-1 procedure, as outlined in section 2.4.6 for silicon surfaces, is compared to the removal of the sacrificial layer pair. Although there is limited particle removal efficiency in the case of SC-1 cleaning, a nearly particle free surface can be obtained by sacrificial layer etching.

Besides the type of wet cleaning, also the drying method can have an important influence on the surface cleanliness. It was found in this work that the use of a nitrogen gun to dry the samples is not optimal as bursts of particles (originating from contamination of the nitrogen, contamination of the tubes or nozzle) can be blown over the sample, destroying the sample cleanliness. A better way to dry the samples is to use a spin drying approach.

For cleaning the silicon-on-insulator host substrate, SC-1 cleaning was used followed by spin drying.

3.6.6 Pressurized bonding

As stated before, pressurized bonding is needed to elastically deform the wafer surfaces to accommodate for non-parallelism of both surfaces (through non-planarity or through bow and warp of the surfaces). The apparatus used in this work for pressurized bonding is shown in figure 3.28. The spring is used for an accurate pressure control (in the setup used, the force increased 1N per wind). Typically a pressure of 300kPa is used to intimately contact both surfaces.

Although this setup could be placed in a nitrogen environment, the curing was performed in air, as the DVS-BCB underneath the bonded sample is not in direct contact with air.

3.6.7 Bonding process

The complete bonding procedure developed in this work is outlined in figure 3.29. In a first step, dies are cleaved, while sawing is an alternative. The InP die is attached to a carrier substrate and both InP die and

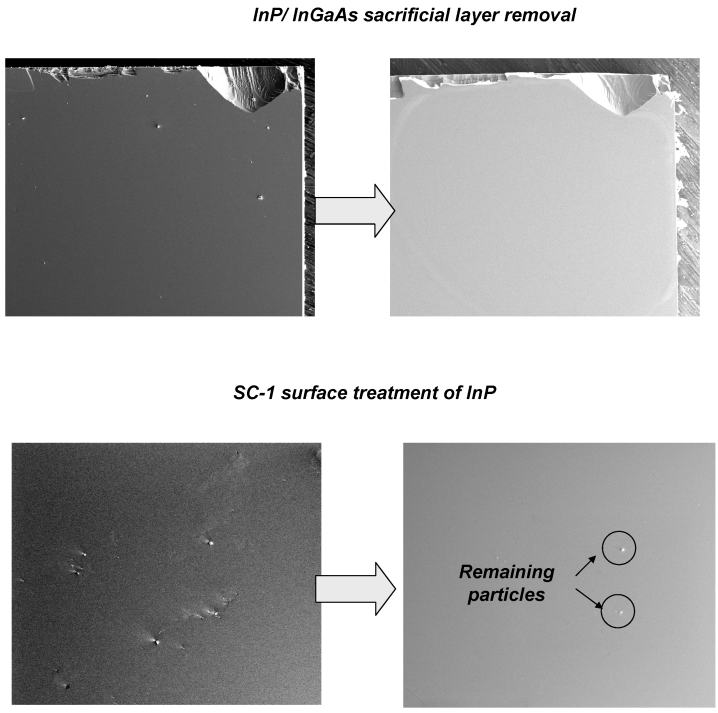


Figure 3.27: Sample surfaces before and after particle removal step: sacrificial layer removal and SC-1 surface cleaning

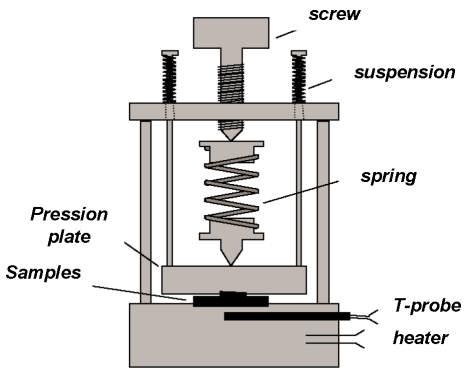


Figure 3.28: Apparatus used for pressurized bonding

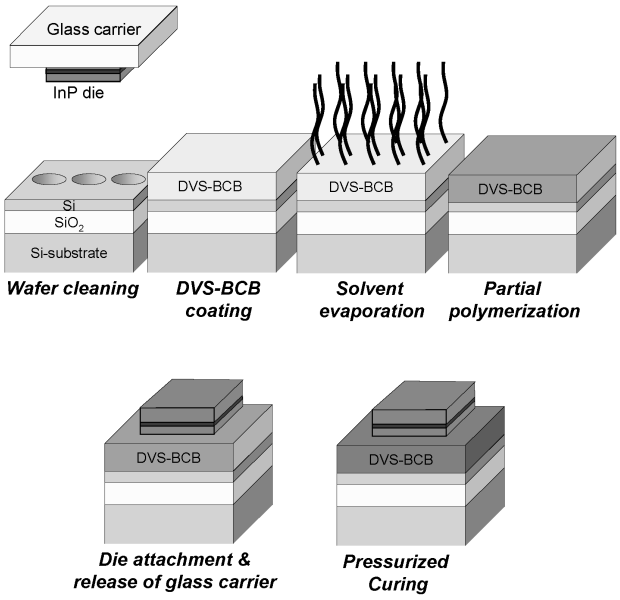


Figure 3.29: DVS-BCB bonding process

silicon-on-insulator host substrate are cleaned. DVS-BCB is spin coated on the silicon-on-insulator substrate, preferably using a double coating process, and the DVS-BCB is partially polymerized prior to bonding. Prior to bonding, the InP surface is conditioned by immersion in a HF solution, to increase the bonding strength, after which the die is attached to the silicon-on-insulator waveguide substrate at 150C, using the vacuum bonding tool described in section 3.5. During die attachment at 150C, the InP die is released from the carrier substrate. After die attachment and carrier release, pressurized hard-curing polymerizes the DVS-BCB, resulting in a void free bond.

3.6.8 Substrate removal

The substrate removal is identical to the case of standard DVS-BCB bonding. Mechanical grinding is advised to reduce the height of the unetched InP ramps.

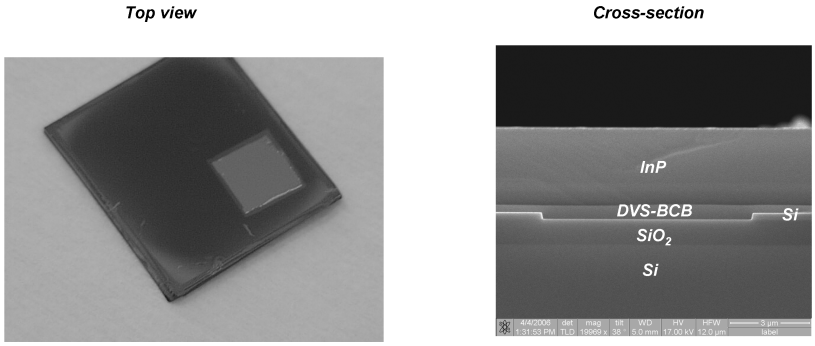


Figure 3.30: Top view and cross-section of ultra-thin bonding on an unprocessed and processed substrate respectively

3.6.9 Bonding results

A top view and a cross-sectional view of an InP/InGaAsP epitaxial layer structure transferred onto an unprocessed and processed silicon-on-insulator substrate respectively using the ultra-thin DVS-BCB bonding process is shown in figure 3.30. Good bonding quality is obtained and no voids can be seen at the bonding interface. Especially, the demonstration of the ability to use sub-micron bonding layer thicknesses on processed SOI substrates in this work, enables the integration of active opto-electronic components on top of the SOI waveguide circuit, allowing efficient coupling of light between both layers, as will be shown in the subsequent chapters.

3.7 Spin-on glass bonding process development

3.7.1 Spin-on glass as a bonding agent

Besides DVS-BCB, spin-on glass (SOG) was also evaluated as a bonding agent in this work. The use as a bonding agent was demonstrated in literature [103] on unprocessed substrates. Ultra-thin spin-on glass layers are commercially available and the material has a higher thermal conductivity (k_{SOG}=0.5W/mK) compared to DVS-BCB, which is beneficial from a device point of view. The use of spin-on glass is also motivated by the fact that bonding occurs at room temperature, thereby leading to a stress-free bonded stack after spin-on glass curing [104].

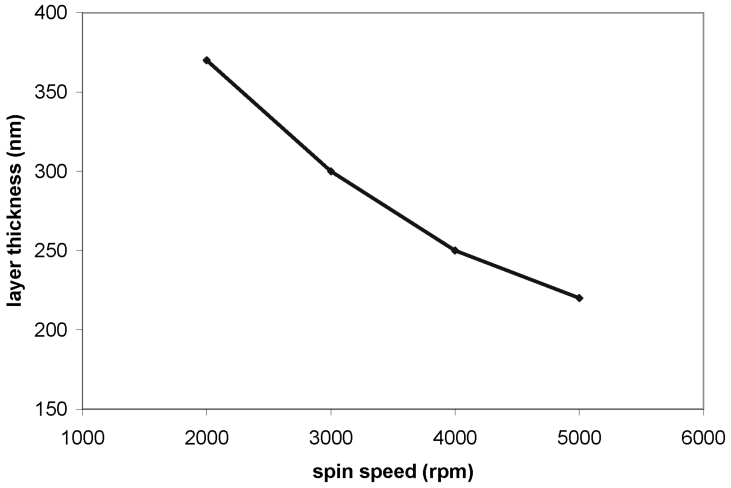


Figure 3.31: T11-311 spin-on glass layer thickness versus spin speed

The Honeywell Accuglass T11-311 methylsiloxane spin-on glass was chosen for our experiments. A layer thickness of 250nm can easily be achieved by spin coating. The bonding layer thickness versus spin speed is plotted in figure 3.31.

3.7.2 Bonding process

Different sample preparations were evaluated in this work. SC-1 cleaning was used to lift off particles from the silicon-on-insulator surface and leave a thin chemical oxide layer on the silicon surface, which improves the adhesion of the spin-on glass layer. Other surface treatments, like subjecting the sample to an O_2 plasma prior to bonding, were also investigated, not leading to better bonding results. After applying the spin-on glass by spin coating, a pre-bake at 150C for 5 minutes was performed to evaporate the remaining solvents in the spin coated layer. Although the cleaning process is identical to the DVS-BCB case, often comet-like defects were observed after spin coating. This is probably related to the rapid aging of spin-on glass, by which crystallites are formed in the spin coating solution. The samples (an InP/InGaAsP heterostructure die and a silicon-on-insulator waveguide die in this case) were manually attached and cured for 2 hours at 300C. After bonding, the InP substrate was removed using mechanical grinding and wet chemical etching using 3HCl:H_2O.

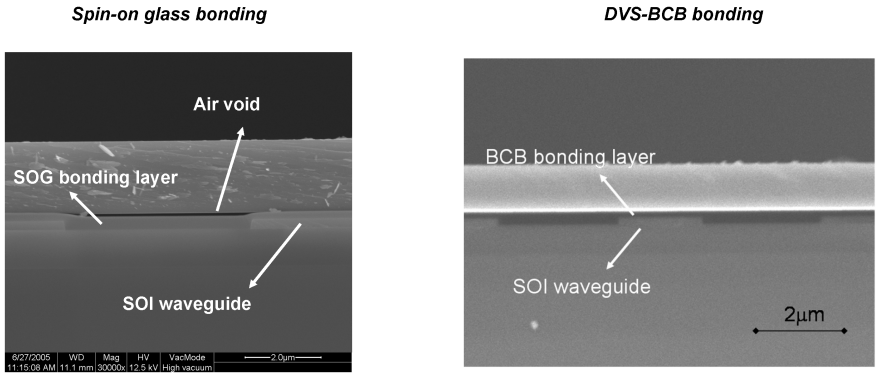


Figure 3.32: Comparison of a SOG bonded sample and a DVS-BCB bonded sample

3.7.3 Comparison with ultra-thin DVS-BCB

A comparison of a DVS-BCB bonded sample and a spin-on glass bonded sample is depicted in figure 3.32. The same topography on both silicon-on-insulator waveguide circuits was used for comparison and the bonding layer thicknesses is about the same. In the case of spin-on glass bonding an air void can be seen at the bonding interface due to the lower degree of planarization. No voids can be seen in the DVS-BCB bonding case. Due to the superior performance of the DVS-BCB, this material was further used in the fabrication of bonded devices.

3.8 Bonding process characterization

Good characterization methods to evaluate the quality of the bonding interface are required, both for process development as for device fabrication. In this section, we will outline a few methods that were used in this work to evaluate the chemical state of the surfaces to be bonded (contact angle measurements), the quality of the bonding interface (optical inspection, infrared transmission, scanning acoustic microscopy, scanning electron microscopy) and the strength of the bond (die shear testing, razor blade method).

Surface treatment	Contact angle (degrees)
InP as received	86
HF	36
SC-1	25
O_2	41
Acetone/IPA/DI	50
H_2SO_4:3H_2O_2:H_2O	39

Table 3.3: Contact angle measurements - results from different surface preparations of an InP die

3.8.1 Surface modifications: contact angle measurements

When a droplet of liquid rests on the surface of a solid, the shape of the droplet is determined by the balance of the interfacial liquid-vapor-solid forces. When a droplet of a high surface tension liquid is placed on a solid of low surface energy, the liquid surface tension will cause the droplet to form a spherical shape (lowest energy shape). The measurement of the droplet shape therefore provides information regarding the surface energy of the solid surface and surface tension of the droplet. Because of its simplicity, contact angle measurements have been broadly accepted for material surface analysis related to wetting, adhesion and the determination of the hydrophilic or hydrophobic nature of the substrate.

Figure 3.33 demonstrates the operation principle. A droplet of a liquid (this can be water for hydrophilic/hydrophobic nature measurements, an adhesive for wetting and adhesion measurements or any other kind of liquid for the determination of the surface energy of the substrate) is deposited on the substrate under investigation through a syringe. After deposition, the contact angle θ is measured, which relates the interfacial energies between liquid (l), solid (s) and vapor (v) state through Young's equation

$$\gamma_{SV} = \gamma_{SL} + \gamma_{LV}\cos(\theta) \tag{3.3}$$

When a water droplet is used, this angle determines how hydrophilic the surface is. Measurement results on an InP substrate obtained in this work, for various chemical treatments, are shown in table 3.3.

Although these measurements do not directly give insight in the chemical nature of the surface, it can give a clue, as a lot is known on the interaction of H_2O with a surface. When a DVS-BCB droplet is used, information can be obtained on the wetting and adhesion of the DVS-BCB to the surface. Moreover, the work of adhesion W_A, which is defined as the work required to separate the drop from the surface

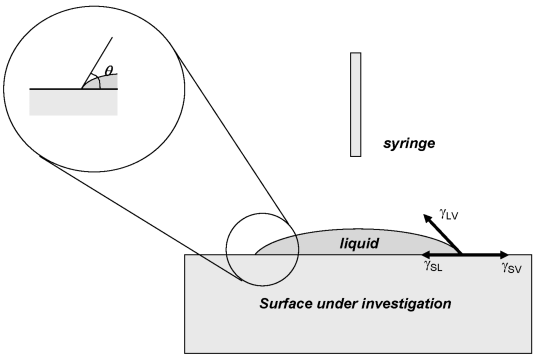


Figure 3.33: Contact angle measurement setup

$$W_A = \gamma_{SV} + \gamma_{LV} - \gamma_{SL} = \gamma_{LV}(1 + \cos(\theta)) \tag{3.4}$$

and which is directly related to the obtainable bond strength, is a function of this contact angle. When performing a series of experiments using various liquids, the surface energy of a solid can be determined. This was done for DVS-BCB in [121], resulting in a surface energy of 30mJ/m^2, which is consistent with the measured bonding energy in figure 3.24.

3.8.2 Optical inspection

While developing a bonding process, it is interesting to be able to investigate the quality of the bonding interface easily. This was done in this work by replacing the silicon-on-insulator substrate by a Pyrex glass substrate, which is transparent and happens to have a thermal expansion coefficient, which is about the same as that of silicon. The bonding interface and more in particular the presence and consequences of particles and air voids at the bonding interface, can be investigated by microscope observation through the Pyrex substrate.

An example of such an inspection measurement is shown in figure 3.34. It shows the presence of a particle at the bonding interface and the bonding defect that is created. Using optical inspection, we can determine the size of the bonding defect. The height of the particle can be deduced by counting the Newton interference fringes formed by the

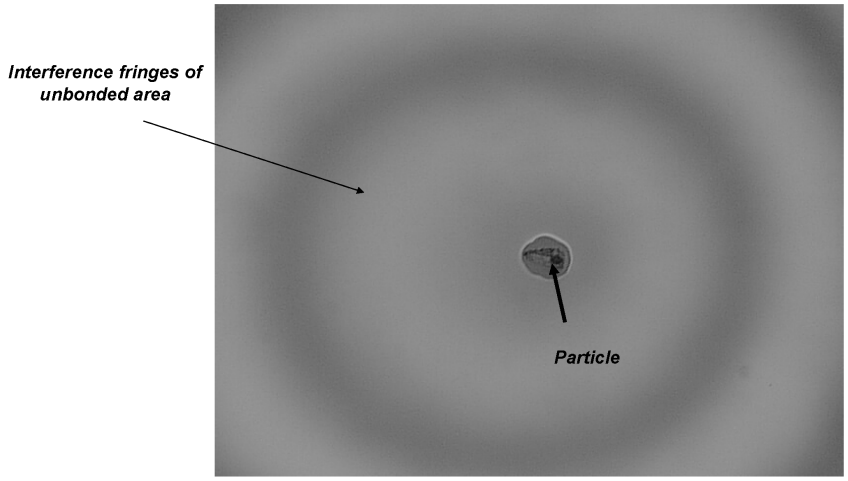


Figure 3.34: Bonding defect observed using optical inspection, showing the particle and the Newton interference fringes created by the wedge formed by the bonding defect

air wedge between both substrates. For an accurate measurement, this is preferably done using monochromatic light.

3.8.3 Infrared transmission

After process development, an inspection of the bonding interface when using dedicated wafer structures is still wanted. As the used materials (silicon-on-insulator and InP/InGaAsP) are opaque in the visible wavelength region, an infrared transmission setup was developed in this work. This setup uses an infrared light source (being in this case a simple halogen lamp) and a camera (silicon CCD or InGaAs IR camera) to visualize the bonding interface. The resolution typically is lower than in the case of optical inspection (especially when single side polished wafers are used). As no large magnification is applied in the setup, only macroscopic features can be resolved. An example of an infrared transmission measurement is shown in figure 3.36, where a change of the bonding interface upon curing is observed. The interference fringes observable in the top left image are due to air inclusion at the bonding interface. After curing, these interference fringes are no longer visible, indicating that the defect is removed (although still a small unbonded

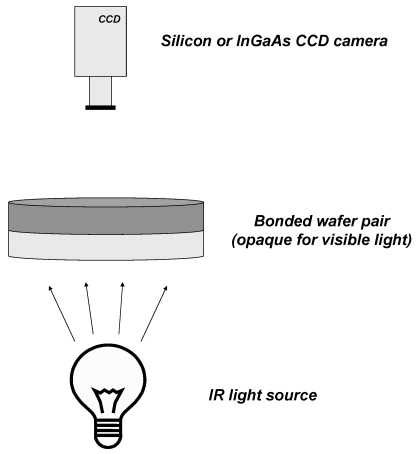


Figure 3.35: Infrared transmission setup

zone near the edge of the die can be observed). A second example shows an unbonded zone near the edge of the die, due to the warp of the die surface or due to a particle at the cleaved die edge. This defect is not affected by the curing process as can be seen from the lower right infrared image.

3.8.4 Scanning acoustic microscopy

Another way to evaluate the bonding interface quality is to detect the areas where film delamination occurs. This can be due to particles at the bonding interface, air inclusion upon die attachment or non-perfect planarization of the silicon-on-insulator topography. Scanning acoustic microscopy (SAM) is used for this purpose in this work. In a scanning acoustic microscope, an ultra-sound acoustical wave (typically 5 to 150MHz) is launched onto the sample by a transducer, using deionized water as a coupling medium. The echo of the pulse (which originates from changes in the acoustic impedance) is detected and interpreted. This is shown in figure 3.37. In particular, when the sound wave hits an air void, a distinct echo pulse originates due to the large difference in acoustical impedance between the solid medium and air, which can be detected. In this way, delamination features with lateral dimensions below 100μm can be detected.

An example of an obtained SAM measurement on a DVS-BCB bonded die is shown in figure 3.38. As the image is homogeneous over the

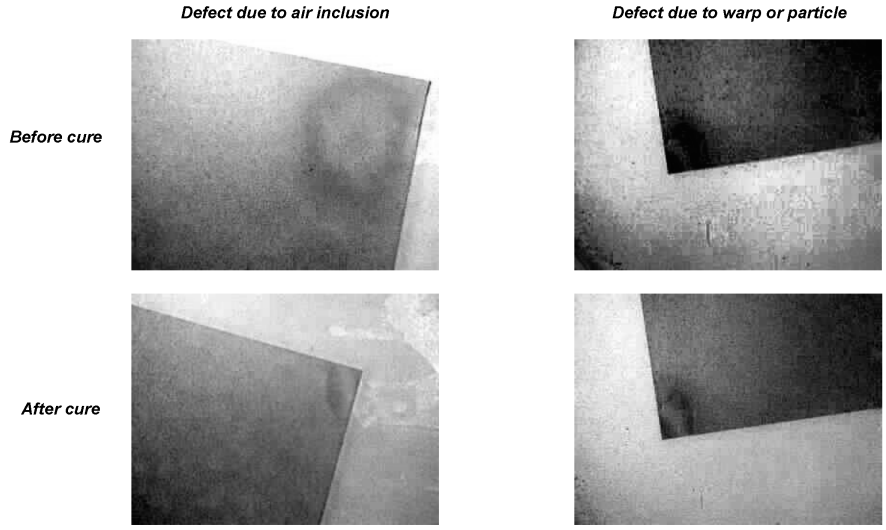


Figure 3.36: Infrared transmission measurements before and after curing

inner part of the die, we can conclude that the epitaxial layer is perfectly transferred. Edge effects due to ramp formation and undercut can be seen however (see section 3.5.6).

3.8.5 Shear strength measurements

The bonding strength can be assessed by measuring the shear force that has to be applied to detach the bonded sample. A needle is used to exert a linearly varying force in time on the sample, while the displacement of the needle is measured, as is shown in figure 3.39. This type of experiments was used in this work to optimize the surface preparation for DVS-BCB bonding, as was explained in section 3.5. As the critical die shear force also depends on the bonding quality (especially when using brittle materials like InP), a large spread in die shear forces can be observed, while evaluating nominally identical samples. When using the optimized surface preparation, a typical die shear strength of 6MPa is obtained (using 25mm^2 dies), which is comparable to the case of direct wafer bonding [122].

Besides die shear force measurements, also pull tests are described in literature. This type of experiments were not carried out, as bonding failure is rather expected to occur under a shear load (during mechanical grinding), as will be discussed in section 3.9.2.

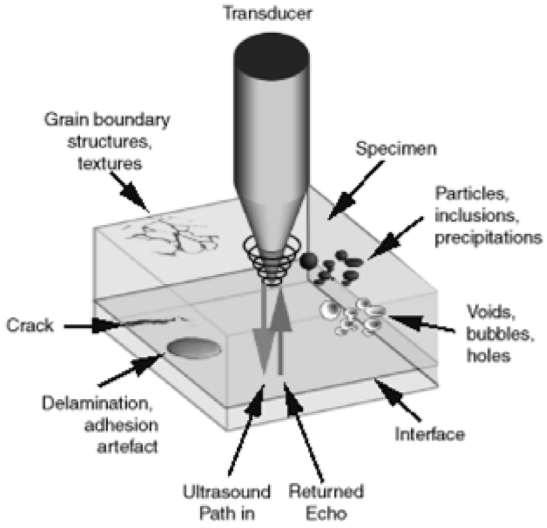


Figure 3.37: Scanning acoustic microscopy - operation principle

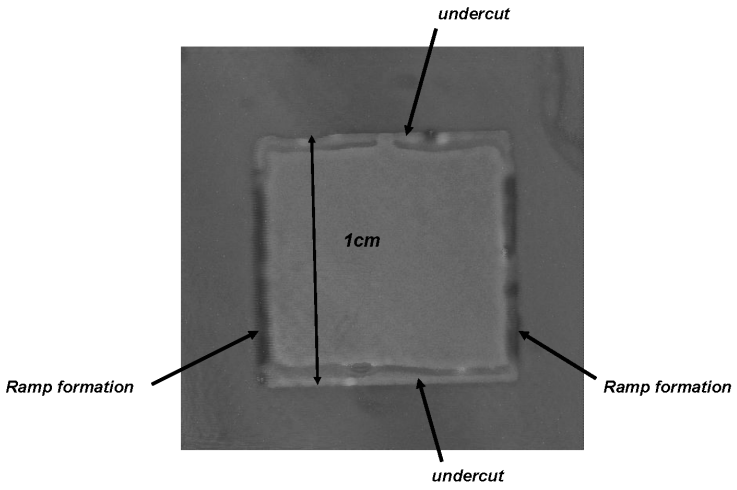


Figure 3.38: SAM measurement result of a bonded die, indicating a high quality layer transfer - edge effects due to ramp formation and undercut can also be seen

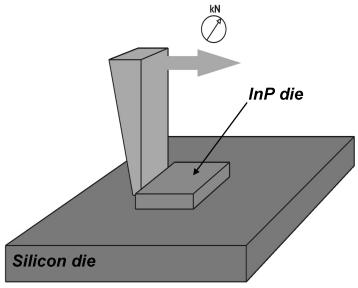


Figure 3.39: Die shear strength measurement setup

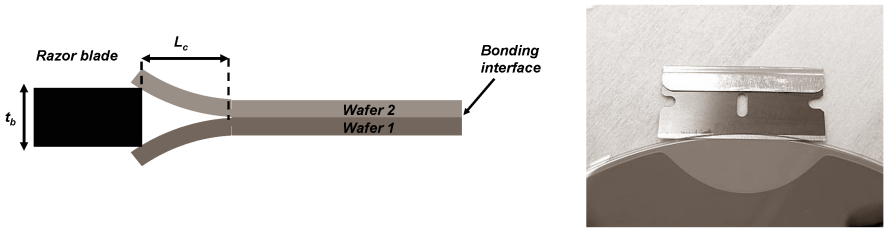


Figure 3.40: Razor blade method to determine critical adhesion energy

3.8.6 Razor blade method

Another method to evaluate the strength of the bonding (and more in particular the critical adhesion energy of the bond) is to use a razor blade insertion method (also referred to as the Maszara razor blade method) [123]. In this method a razor blade of known height is inserted at the bonding interface and the crack opening length is measured (this can be through optical inspection as is shown in figure 3.40 or through infrared transmission measurements when opaque substrates are used). The critical adhesion energy γ_{CAE} is related to this crack opening length by

$$L_c = \left[\frac{3t_b h_1 h_2 E_1 E_2}{8\gamma_{CAE}(E_1 h_1^3 + E_2 h_2^3)}\right]^{1/4} \tag{3.5}$$

in which t_b is the thickness of the razor blade used, h_1, h_2 and E_1,E_2 the thickness and elasticity modulus of both wafers respectively and γ_{CAE} the critical adhesion energy [124].

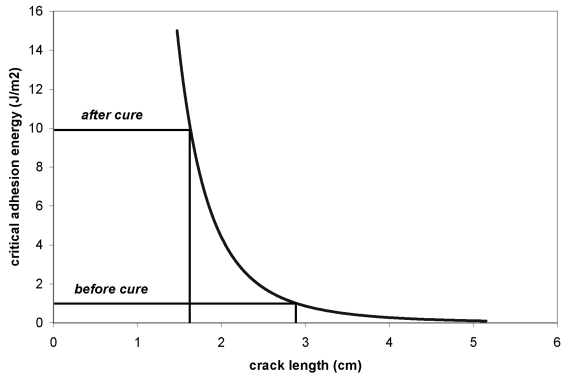


Figure 3.41: Results of the razor blade critical adhesion energy measurement

The obtained measurement results in this work of a DVS-BCB bonded Pyrex/silicon pair, before and after curing, are shown in figure 3.41, showing a large increase in critical adhesion energy upon curing. These large energy values cannot be compared to the case of direct bonding (in which the maximum obtainable adhesion energy is about $2J/m^2$, the breakage strength of silicon). This is due to the fact that the debonding mechanism in a direct bond is a brittle fracture, whereas in the case of adhesive bonding, a lot of energy is dissipated in plastic deformation of the adhesive). Moreover, the dissipated plastic energy linearly depends on the bonding layer thickness, so care has to be taken when comparing results in literature [106].

The razor blade method is the basic method to assess the bonding energy of a bonded wafer pair (or critical adhesion energy in the case of an adhesively bonded wafer pair). Due to the fourth power dependence of the bonding energy on the crack length, it is sensitive to errors in the measurement of the crack length.

Other, more robust methods exist to overcome this problem. In the blister test [84], the test sample consists of two bonded wafers with one wafer containing a hole. Hydrostatic oil pressure is applied through the hole in the bottom wafer and the critical pressure for debonding is measured, which is related to the critical adhesion energy.

The four-point bending method [106] is based on a theory of fracture mechanics in which delamination is modelled as a crack propagating along the interface between two materials. In a bonded specimen, a pre-crack is formed by sawing partially through one of the wafers. A four-point load is applied to the specimen, to bend the specimen. As the

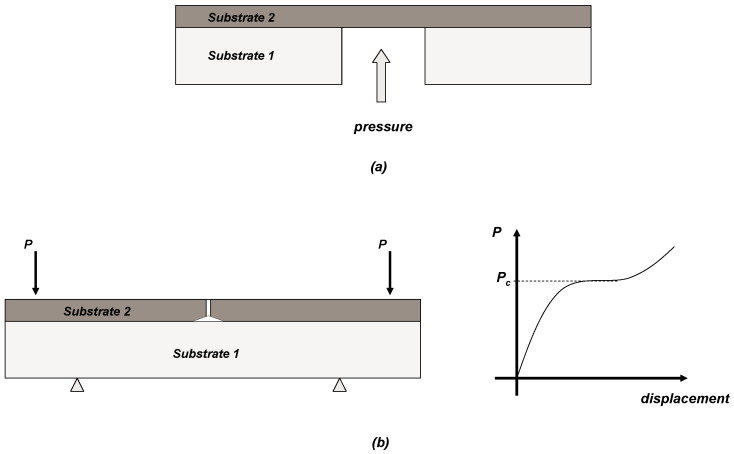


Figure 3.42: Alternative critical adhesion energy measurement methods: blister test (a) and four-point bending method (b)

load is applied, the bending moment in the pre-crack increases. When the applied load reaches a critical value, a bending-induced crack initiates at the tip of the pre-crack and propagates along the weak bonding interface. The displacement of the sample is measured while increasing the load. By measuring the plateau load region due to crack propagation along the bonding interface, the critical load is found, which is related to the bonding energy of the specimen. Both methods are schematically shown in figure 3.42. These methods were however not developed in the context of this PhD.

While both die bonding strength measurements (die shear strength and tensile strength measurements) and bonding energy measurements (razor blade method, blister test and four-point bending method) were described, it must be stated that there is no mathematical correlation between these measurements.

3.8.7 Scanning electron microscopy

An obvious way to evaluate the bonding quality is to make a cross-section of a bonded layer structure by cleaving and inspect the bonding interface through scanning electron microscopy. Eventually, a local focused ion beam (FIB) cross-section can be used to investigate a particular bonded area (as will be discussed in section 5.3). Two examples of scanning electron microscopy cross-section images are shown in figure

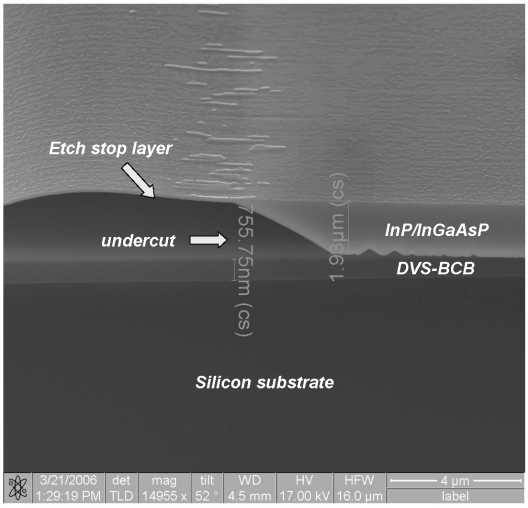


Figure 3.43: Undercut during chemical substrate removal

3.20 and 3.43. The ramps and the undercut formed during substrate removal are shown respectively.

3.9 Stress in bonded films

3.9.1 Influence of stress on optical properties

Stress in a layer structure can affect the optical properties of the material. A stress-induced electronic band shifting, as is shown in figure 3.44(a), leads to a shift in the emission wavelength and absorption edge of a material and to a polarization dependence of the gain and absorption coefficient. This can be desired (e.g. the case of strained quantum wells in laser diodes) or can be an unwanted effect. At large stress levels, dislocations can be created. The stress level at which these dislocations can be formed, depends on the substrate temperature and is empirically found to be

$$\sigma_{crit} = 1100 \exp(\tfrac{5934}{T}) \quad Pa \tag{3.6}$$

for InP/InGaAsP and is shown in figure 3.44(b) [125].

In the case of wafer bonding, stress is induced in the bonded stack, due to the difference in thermal expansion coefficients between the materials to be bonded. When stress levels are too high, even debonding

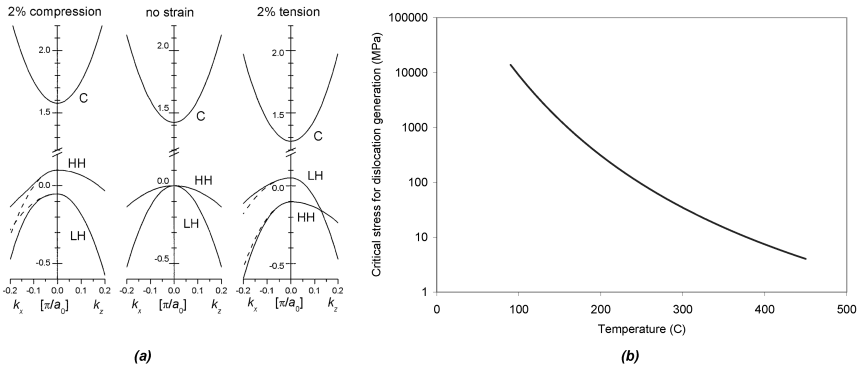


Figure 3.44: Influence of stress on the electronic band structure (a) and the generation of dislocations (b)

Material	TEC (ppm/K)	Elasticity modulus (GPa)	Young's modulus
Silicon	3.0	130	0.29
SiO_2	0.6	70	0.2
InP	4.6	100	0.36
DVS-BCB	42.0	3	0.36
Pyrex	3.3	65	0.2

Table 3.4: Thermal expansion coefficient (TEC), elasticity modulus and Young's modulus of commonly used materials for bonding

or shattering of the wafer pair can occur. Moreover, upon InP substrate removal, the silicon-on-insulator wafer nearly completely relaxes and all stress is concentrated in the InP/InGaAsP epitaxial layer. Therefore, a mathematical model for the stress in a multi-layer bonded structure will be derived and backed up by stress measurements in the next section.

In table 3.4, the thermal expansion coefficient α, elasticity modulus E and Young's modulus ν at room temperature of a set of commonly used materials for bonding are shown.

3.9.2 Mathematical models

In this section, we will develop an analytical model to predict the stress levels occurring in bonded structures. The in-plane stress in multi-layer structures will be analyzed, after which shear and peeling stress will be introduced. Finally, the influence of the die edge shape on the stress levels near the edge of the die will be discussed.

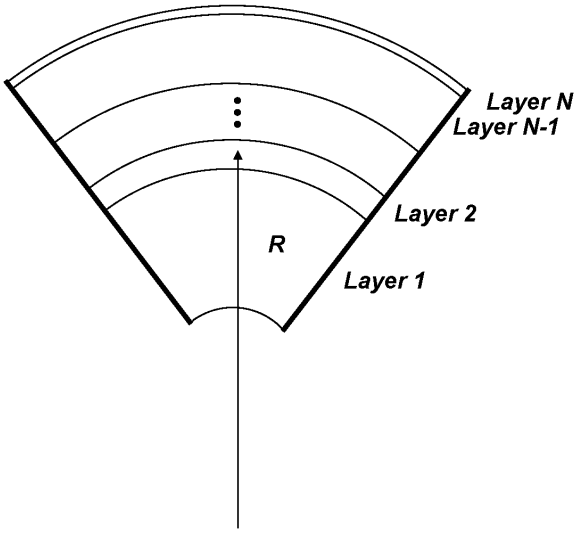


Figure 3.45: Bent multi-layer structure - circular shaped layers of equal radius are assumed

The analytic solution technique described here for the quantification of elastic strain in general N-layer laminar structures is based upon the theory of small deflections [126]. The source of strain that is considered, is the difference in thermal expansion coefficient between the different materials in the stack. The intrinsic stress, e.g. of deposited films, is not taken into account. It is assumed that low to moderate values of induced strain are accommodated elastically through the formation of in-plane stresses and bending strain relief, resulting in a global spherical deformation of the stack. The accommodation of larger strain by plastic deformation, delamination and mechanical failure is not taken into account.

A cross-section of a multi-layer composite structure that is spherically deformed, is shown in figure 3.45. Mechanical equilibrium demands that the sum of the net forces and the sum of the moments within each layer of the structure equal zero. This results in

$$\sum_{i=1}^{N} F_i = 0 \tag{3.7}$$

and

$$\frac{E_1' t_1^3}{12R} + F_1(\frac{t_1}{2}) + ... + \frac{E_n' t_n^3}{12R} + F_n(\sum_{i=1}^{N-1} t_i + \frac{t_N}{2}) = 0 \qquad (3.8)$$

in which F_i, E_i' and t_i denote the force acting on layer i, the biaxial Young's modulus of layer i and the thickness of layer i respectively. R is the radius of curvature of the wafer stack. In equation 3.8, $\frac{E_i' t_i^3}{12R}$ represents the bending moment of layer i.

Applying the boundary condition of interface strain continuity for any two adjacent layers, leads to

$$\begin{aligned}
&\tfrac{F_1}{E_1' t_1} + \tfrac{t_1}{2R} + \alpha_1(T_2 - T_0) = \tfrac{F_2}{E_2' t_2} - \tfrac{t_2}{2R} + \alpha_2(T_2 - T_0) \\
&... \\
&\tfrac{F_{N-1}}{E_{N-1}' t_{N-1}} + \tfrac{t_{N-1}}{2R} + \alpha_{N-1}(T_N - T_0) = \tfrac{F_N}{E_N' t_N} - \tfrac{t_N}{2R} + \alpha_N(T_N - T_0)
\end{aligned} \qquad (3.9)$$

Each equation represents the strain continuity at an interface in the bonded stack. The term $\frac{F_i}{E_i' t_i}$ represents the strain induced by the force acting on layer i through the definition of the biaxial Young's modulus. The second term $\pm\frac{t_1}{2R}$ is related to the tensile/compressive stress that originates from the bending of the wafer stack (compressive at the bottom of a layer and tensile at the top of the layer for a positive R). The third term, $\alpha_i(T_{i(+1)} - T_0)$, originates from the thermal expansion of layer i. T_i is the "deposition" temperature of layer i in the wafer stack, so it is assumed to be free of thermal expansion induced strain at this temperature. In the case of curing a double wafer stack (for example InP on silicon) using DVS-BCB this occurs when the DVS-BCB fixes both substrates (at this temperature the top wafer is "deposited" on the bottom wafer). It was experimentally determined in this work to occur around 230C (see section 3.9.3). As discussed above, this occurs at room temperature for the case of spin-on glass bonding. When multi-layered substrates are bonded, for example InP on SOI, this deposition temperature is assumed to be room temperature for the SOI layers. T_0 represents the temperature at which the stress in the wafer stack is analyzed.

This set of (N+1) equations for (N+1) unknowns (the N forces F_i and the bending radius R) can be cast in a matrix formulation as below

$$\begin{bmatrix} 1 & 1 & 1 & ... & 1 & 0 \\ \frac{t_1}{2} & t_1+\frac{t_2}{2} & & ... & \sum_{i=1}^{N-1} t_i + \frac{t_N}{2} & \sum_{i=1}^{N} \frac{E_i t_i^3}{12} \\ \frac{1}{E_1 t_1} & -\frac{1}{E_2 t_2} & 0 & 0 & ... & \frac{t_1+t_2}{2} \\ 0 & \frac{1}{E_2 t_2} & -\frac{1}{E_3 t_3} & 0 & ... & \frac{t_2+t_3}{2} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & ... & \frac{1}{E_{N-1} t_{N-1}} & -\frac{1}{E_N t_N} & \frac{t_{N-1}+t_N}{2} \end{bmatrix} \begin{bmatrix} F_1 \\ F_2 \\ F_3 \\ \vdots \\ F_N \\ \frac{1}{R} \end{bmatrix}$$
$$= \begin{bmatrix} 0 \\ 0 \\ -(\alpha_1-\alpha_2)(T_2-T_0) \\ \vdots \\ \\ -(\alpha_{N-1}-\alpha_N)(T_N-T_0) \end{bmatrix} \tag{3.10}$$

After solving for F_i and R, the maximum stress in layer i can be calculated as

$$\sigma_{i,\max} = \frac{F_i}{t_i} + \frac{sign(F_i)}{|R|}\frac{E_i' t_i}{2} \tag{3.11}$$

which contains a component due to the elastic strain in the layers and a component due to the bending of the wafer stack. The maximum strain in layer i can be calculated as

$$\varepsilon_{i,\max} = \frac{\sigma_{i,\max}}{E_i'} \tag{3.12}$$

As an example, we will consider the case of a three-layer stack formed by a 350μm thick InP wafer ($E_{InP} = 100GPa, \nu_{InP} = 0.36$) that is bonded to a 750μm silicon wafer ($E_{Si} = 130GPa, \nu_{Si} = 0.29$) using 1$\mu$m of DVS-BCB ($E_{DVS-BCB} = 3GPa, \nu_{DVS-BCB} = 0.36$). The "deposition" temperature of the bonded stack is 230C, as discussed above.

Using the model outlined above, we can calculate the bending of the wafer stack, the maximum stress level occurring in the InP wafer and the influence of thinning the InP substrate on the stress and strain level in the layer (assuming that no additional stress is caused by the thinning procedure). The results are plotted in figure 3.46 and figure 3.47. In this simulation, the temperature dependence of the thermal expansion coefficient of InP and silicon was taken into account.

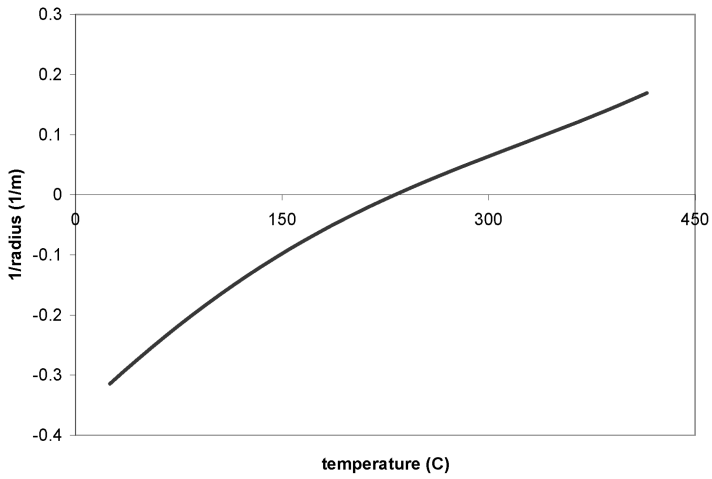


Figure 3.46: Simulation of the evolution of wafer curvature with temperature

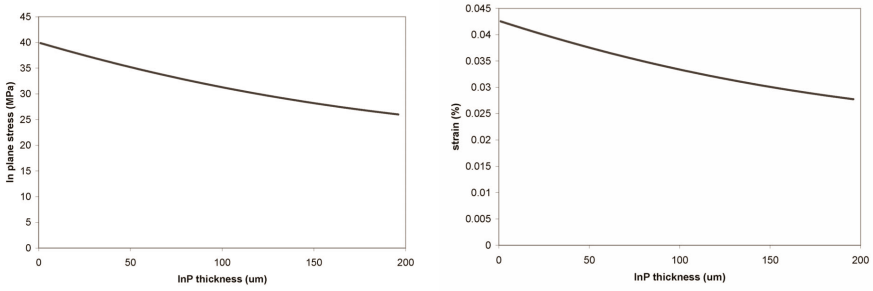


Figure 3.47: Influence of InP thickness on normal in-plane stress levels

At room temperature the InP substrate (and after substrate thinning the InP film) is under tensile stress. Stress levels at room temperature up to 40MPa are obtained, which correspond to a strain of 0.04 percent. This is sufficiently low from an optical point of view as the influence of the stress on the band shifting is acceptable. Comparing the simulation results with the stress levels needed to induce dislocations in the layer structure (figure 3.44(b)), elevating the temperature after bonding to temperatures higher than 400C could create dislocations in the InP layer, which should be avoided.

Replacing the silicon substrate by a silicon-on-insulator substrate doesn't considerably affect these results, as the major contribution to the induced stress is the difference in thermal expansion coefficient between the InP film and the silicon substrate.

In [127], the interfacial shear stress and stress that is normal to the interface is calculated (which is responsible for peeling and blistering of the films) and the calculations for stress parallel to the interface is modified. An exponential variation in the stress distribution across the films is suggested. The normal stress (that is parallel to the interface) is given by

$$\sigma_i(x) = \sigma_i(0)(1 - \exp(-k(L - x))) \tag{3.13}$$

in which L is the radius of the multi-layer stack and $\sigma_i(0)$ is the stress level in layer i, as calculated by equation 3.11. k is a constant that depends on the materials used in the stack and the thickness of the layers. Typically the stress drops to zero in an area that is very close to the edge of the stack (within $0.001L$ from the edge).

The shear stress that exists at the interface between the layers in the stack is then given by

$$\tau_i(x) = -\sigma_i(0)t_i k \exp(-k(L - x)) \tag{3.14}$$

and the peeling stress that is normal to the interfaces is given by

$$p_i(x) = -\frac{1}{2}(kt_i)^2 \sigma_i(0) \exp(-k(L - x)) \tag{3.15}$$

These stress distributions are shown in figure 3.48. It is clear that, while the normal stress drops to zero at the wafer edge, the shear and peeling stress are concentrated near this edge.

Although providing an easy to use estimation, both for stresses in layers and for interfacial stresses between layers, the peeling stress distribution violates global equilibrium [128] and the stress equilibrium in

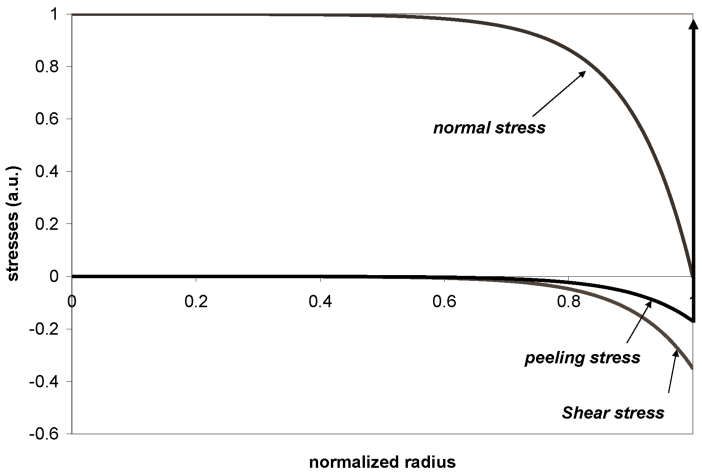


Figure 3.48: Stress behavior near the edge of a bonded layer: normal stress, peeling stress and shear stress function

the direction normal to the layers is not satisfied unless an additional concentrated force is introduced at the edge of the bonded layer.

From figure 3.47 it is clear that the layer thickness has only a limited influence on the normal stress levels in that layer. However, shear and peeling stresses increase with film thickness. As these stresses initiate the debonding of a wafer pair, the thickness of the wafers has an important influence on the temperature excursion that is allowed after bonding. This was confirmed by experiment in [129], where the fracture and/or separation temperature of a directly bonded GaAs/silicon wafer pair was measured for different GaAs/silicon thickness ratios. Decreasing the ratio (and the absolute thickness of the wafers), increased the fracture temperature from 160C to over 350C.

Also in [129], a finite element model was used to confirm the exponential increase of the shear stress near the edge of a bonded wafer pair. Moreover, it was shown that the shape of the edge of the bonded structures can change the maximum stress levels. It was also acknowledged that the actual size of the wafer modelled was not critical as long as it was many wafer stack thicknesses in diameter. This confirms the fact that the radius L of the multi-layer stack doesn't occur in the maximum stress level equations.

As the previously discussed analytical model was only approximative in nature and restricted to a rotation symmetric multi-layer stack

in which all layers have the same radius L, in this work a finite element model analysis was performed using COMSOL, a robust finite element analysis toolbox, on the stress levels occurring in InP square dies bonded to a larger silicon substrate. As the three-dimensional structure including a thin bonding layer would require an extensive computational power due to the fine meshing that is required in the thin bonding layer, no intermediate bonding layer was assumed (thereby emulating the case of a direct InP to silicon bond). The structure is meshed using tetrahedral elements. Second order elements were used implying a parabolic displacement function on the edges of the tetrahedral elements. Each node i of the mesh can be displaced by (u_i,v_i,w_i) in the (x,y,z) direction respectively. These displacement functions are related to the strain in the material by

$$\begin{aligned}
\varepsilon_x &= \frac{\partial u}{\partial x} \\
\varepsilon_y &= \frac{\partial v}{\partial y} \\
\varepsilon_z &= \frac{\partial w}{\partial z} \\
\varepsilon_{xy} &= \frac{1}{2}\left(\frac{\partial u}{\partial y} + \frac{\partial v}{\partial x}\right) \\
\varepsilon_{yz} &= \frac{1}{2}\left(\frac{\partial v}{\partial z} + \frac{\partial w}{\partial y}\right) \\
\varepsilon_{xz} &= \frac{1}{2}\left(\frac{\partial u}{\partial z} + \frac{\partial w}{\partial x}\right)
\end{aligned} \tag{3.16}$$

in which ε_i denote the normal strain components and ε_{ij} are the shear strain components. The definition of these strain components is graphically depicted in figure 3.49. In the case of the normal strain components, the deformation is in the same direction as the original length, while in the case of shear strain the deformation is perpendicular to it. The shear strain is defined as the average strain under a shear load.

These strain components can be ordered in a strain vector ε, which is related to the stress vector σ by

$$\varepsilon = \mathbf{A}\sigma \tag{3.17}$$

with

$$\mathbf{A} = \begin{bmatrix}
\frac{1}{E} & \frac{-\nu}{E} & \frac{-\nu}{E} & 0 & 0 & 0 \\
\frac{-\nu}{E} & \frac{1}{E} & \frac{-\nu}{E} & 0 & 0 & 0 \\
\frac{-\nu}{E} & \frac{-\nu}{E} & \frac{1}{E} & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{G} & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{G} & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{G}
\end{bmatrix} \tag{3.18}$$

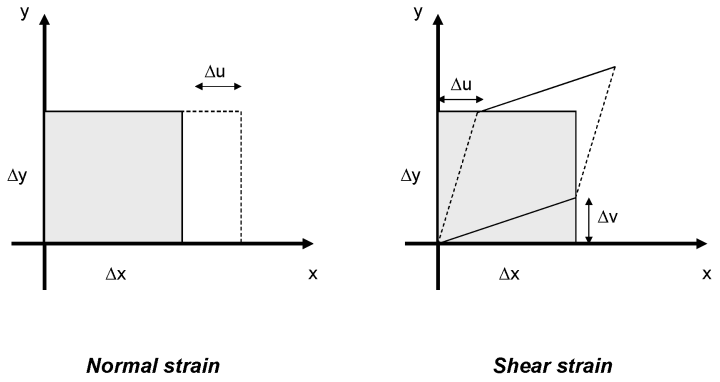


Figure 3.49: Definition of normal and shear strain

in which E is the Young's modulus of the material, ν is the Poisson ratio and G is the shear modulus of the material. From elasticity theory one can deduce that

$$G = \frac{E}{2(1+\nu)} \tag{3.19}$$

Inverting equation 3.17 leads to

$$\begin{bmatrix} \sigma_x \\ \sigma_y \\ \sigma_z \\ \tau_{xy} \\ \tau_{yz} \\ \tau_{xz} \end{bmatrix} = \frac{2G}{(1-2\nu)} \begin{bmatrix} 1-\nu & \nu & \nu & 0 & 0 & 0 \\ \nu & 1-\nu & \nu & 0 & 0 & 0 \\ \nu & \nu & 1-\nu & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1-2\nu}{2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1-2\nu}{2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1-2\nu}{2} \end{bmatrix} \begin{bmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \\ \varepsilon_{xy} \\ \varepsilon_{yz} \\ \varepsilon_{xz} \end{bmatrix} \tag{3.20}$$

The force equilibrium requires that

$$\begin{aligned} \frac{\partial \sigma_x}{\partial x} + \frac{\partial \tau_{xy}}{\partial y} + \frac{\partial \tau_{xz}}{\partial z} + f_x = 0 \\ \frac{\partial \sigma_y}{\partial y} + \frac{\partial \tau_{xy}}{\partial x} + \frac{\partial \tau_{yz}}{\partial z} + f_y = 0 \\ \frac{\partial \sigma_z}{\partial z} + \frac{\partial \tau_{yz}}{\partial y} + \frac{\partial \tau_{xz}}{\partial x} + f_z = 0 \end{aligned} \tag{3.21}$$

with (f_x,f_y,f_z) the volume body forces in (x,y,z) direction.

The equations discussed above describe the stress and strain occurring in a material subjected to an external load. In the case of a thermal expansion mismatch problem (as is here the case), no body forces are

present and a thermal expansion strain term has to be added to the normal strain equation, leading to

$$\begin{aligned} \varepsilon_x &= \frac{\partial u}{\partial x} + \alpha(T - T_{dep}) \\ \varepsilon_y &= \frac{\partial v}{\partial y} + \alpha(T - T_{dep}) \\ \varepsilon_z &= \frac{\partial w}{\partial z} + \alpha(T - T_{dep}) \end{aligned} \tag{3.22}$$

in which T is the temperature at which the stress levels are measured and T_{dep}, is the "deposition" temperature or bonding temperature.

Substituting equation 3.20 in 3.21 and using equation 3.22, results in a set of equilibrium equations in the displacements (u,v,w), which are solved using the finite element analysis tool COMSOL. Strain continuity at the interfaces between two materials is assured, as both materials share nodes from the mesh at the interface.

In the numerical calculations, a square InP die with thickness t_{InP} and side w_{InP} was bonded to a square silicon substrate with a thickness of 750μm and a side of 4cm. The bonding temperature was assumed to be 230C and the stress levels at room temperature were calculated. The influence of the size of the InP die, both in thickness and side width, on the normal stress, peeling stress and shear stress, was evaluated. The normal stress was evaluated in the bulk of the InP die, while the peeling and shear stress were evaluated at the interface between InP and silicon. Simulations were performed for an InP die of 1cm and 2cm wide while the thickness varied from 75μm to 15μm. The relevant stress components in the bonded InP die are shown in figure 3.50, 3.51 and 3.52.

Several conclusions can be drawn from these simulations. First, a rather good correspondence between the analytical model and the finite element analysis is obtained. Only in the case of the peeling stress, the singularity at the edge of the die is replaced by a more smooth transition. Considering the influence of the size of the die, one can conclude that the die size has only little influence on the normal stress, shear stress and peeling stress in the structure. This is consistent with the analytical expressions in which the maximum stress levels are not determined by the size of the stack L. The thickness of the InP die does play a significant role however [130]. The shear stress and peeling stress, which can cause shattering or debonding of a bonded die, increase with increasing die thickness and the stress function is distributed over a larger area with increasing die thickness. The normal stress levels increase with decreasing InP thickness however, which is

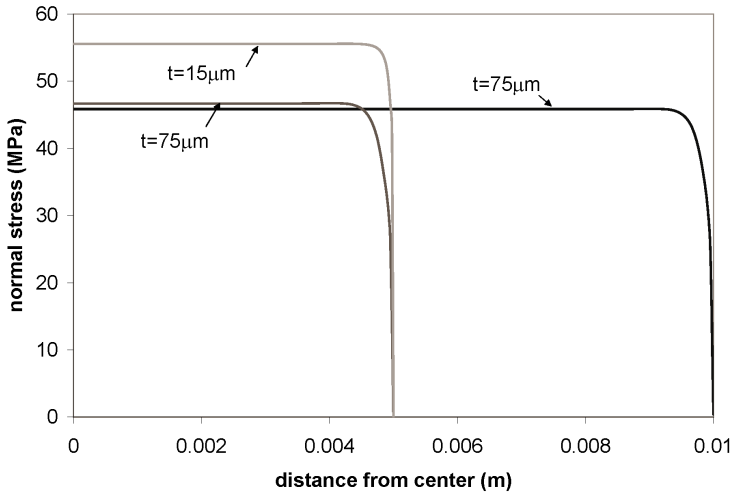


Figure 3.50: Simulated normal in-plane stress function in a bonded InP die (for varying die thickness and chip size)

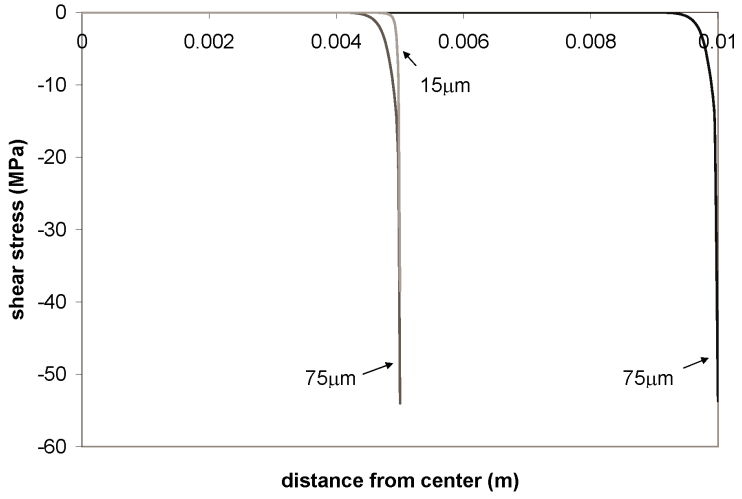


Figure 3.51: Simulated shear stress function at the bonding interface between a bonded InP die and a silicon substrate (for varying die thickness and chip size)

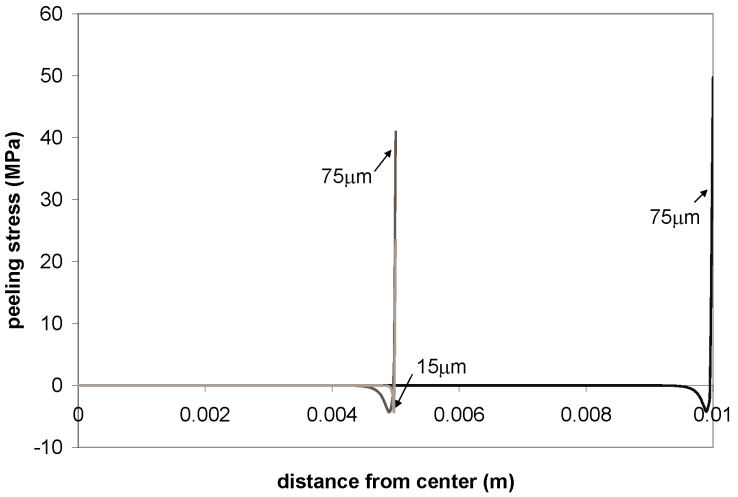


Figure 3.52: Simulated peeling stress function at the bonding interface between a bonded InP die and a silicon substrate (for varying die thickness and chip size)

related to the relaxation of the stress in the silicon substrate as the InP die is thinned. This is shown in figure 3.53, in which a cross-section of the normal in-plane stress in the bonded stack is plotted for an InP thickness varying from 375μm over 75μm to 15μm.

As the peeling stress is compressive at room temperature (not considering the singularity at the wafer edge), no peeling failure is to be expected. This can however be the case when the temperature is elevated above the bonding temperature, where the peeling stress becomes tensile. Since in practice the processing temperature is only elevated above the bonding temperature after substrate removal, chance for peeling failure is small. A more important point of concern is failure due to the shear stress, as the thick bonded InP die is subjected to shear forces during the grinding operation. Chipping of the edges of the bonded die during grinding (as shown in figure 3.20) is related to this shear stress failure. Therefore, in section 3.8.5 the bonding process was optimized to obtain a high shear strength.

The deformation of the wafer stack and the sign of the normal stress and peeling stress are shown in figure 3.54 for an InP to silicon bonded layer stack at room temperature and at a temperature above the bonding temperature.

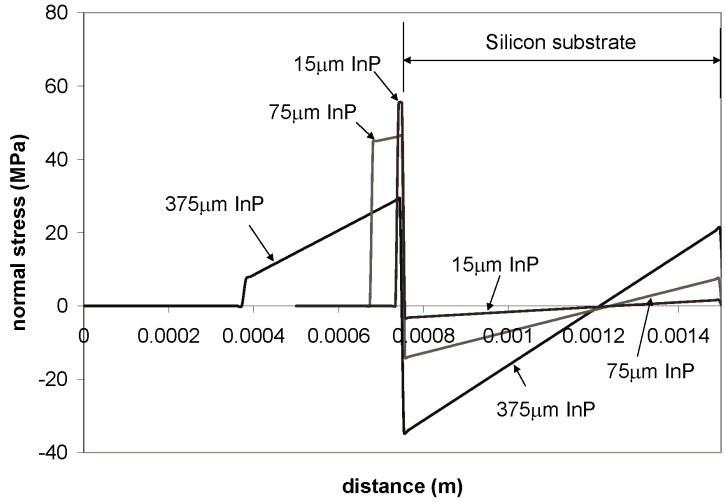


Figure 3.53: Stress relaxation in the silicon substrate through thinning of the InP die

Figure 3.54: Deformation of the bonded wafer stack upon cooling and heating

3.9.3 Stress measurements

Wafer curvature measurements

For the two-layer problem of a thin film deposited on (or bonded to) a substrate, the Stoney equation for the stress in the thin film [131]

$$\sigma = \frac{E_s' t_s^2}{6Rt_f} \tag{3.23}$$

can be derived, indicating that the stress in the thin film is linearly dependent on the wafer curvature $\frac{1}{R}$. Therefore, measuring the wafer curvature and inserting the layer thicknesses and material parameters in equation 3.23, allows to calculate the stress level in the thin film. For a multi-layer structure it is no longer possible to explicitly write the stress in a layer as a function of the wafer curvature without having information on the thermal expansion coefficients of the layers in the stack.

The material parameters in the model can be fitted however to the measured wafer curvature and from this fitting, the stress in the individual layers can be calculated using the model.

Wafer curvature measurements on a bonded InP/silicon wafer pair (using 1μm DVS-BCB) were performed in this work using a dual laser beam wafer curvature measurement setup within the department of Solid State Physics. The measurement setup is shown in figure 3.55. Two parallel laser beams are generated and hit the curved wafer surface of the InP die. The reflected laser beams are no longer parallel and the distance between the two laser beams is measured at a certain distance from the wafer surface. This allows a measurement of the wafer curvature.

By placing the bonded structure on a heater, the wafer curvature as a function of temperature can be recorded. The measurement results are shown in figure 3.56.

Several conclusions can be drawn from this measurement. First, a good correspondence between model (figure 3.46) and measurement is obtained. This justifies the use of the model to determine the stress levels in a bonded layer structure. Secondly, the wafer stack is stress free at 230C, indicated by the fact that wafer curvature is zero at that temperature. This corresponds to the temperature at which the DVS-BCB fixes the InP and silicon substrate. A third conclusion that can be drawn, is that the DVS-BCB bonding survives heating to 420C (ramped at 5C/min): as the relation between wafer curvature and temperature

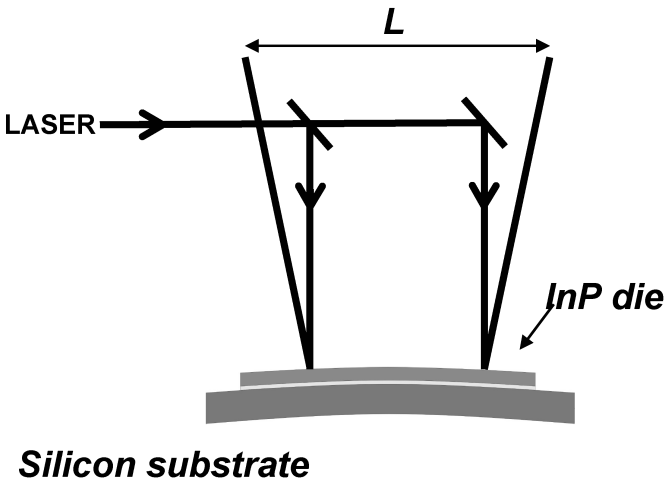


Figure 3.55: Measurement of wafer bending using a parallel laser beam setup

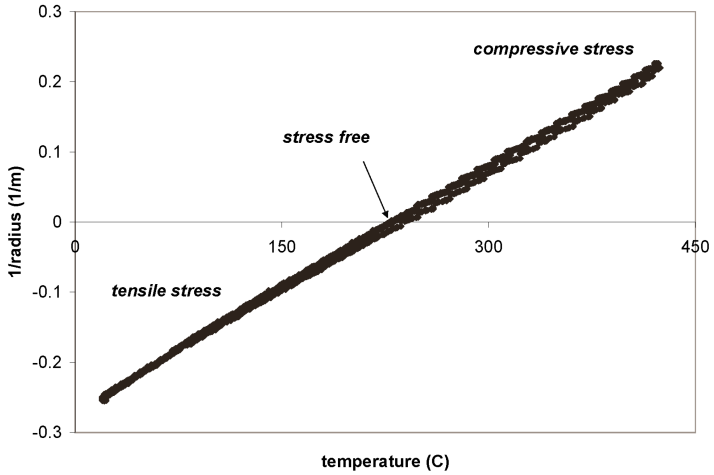


Figure 3.56: Measurement of the wafer curvature as a function of temperature

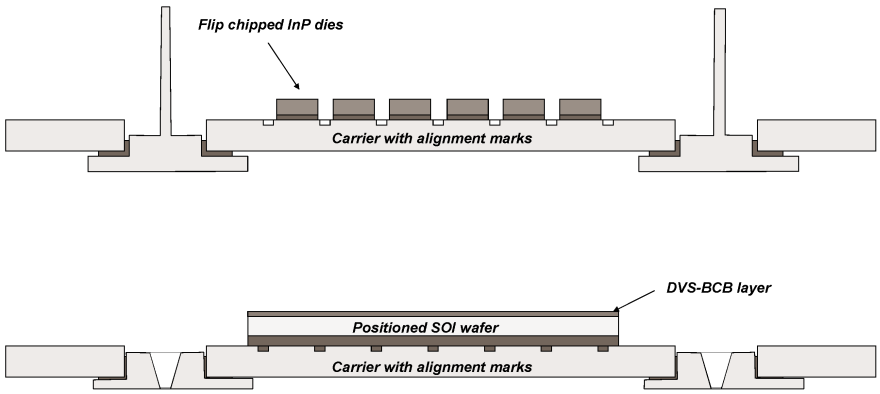


Figure 3.57: Multiple-die bonding mechanism - flip-chipping of InP dies onto carrier substrate

remains linear, no debonding or sliding at the bonding interface occurs, which would show up as kinks or hysteresis in the graph.

3.10 Multiple-die bonding

While the processes developed in this chapter were limited to bonding a single InP die on a host substrate, we will show in this section that the principle can be extended to bonding multiple dies on a host substrate. Two types of processes could be used to achieve this, which were however not developed in this work.

In a first approach, two carriers are used, one for carrying the InP dies to be bonded and one for carrying the SOI host wafer. The dies are positioned and attached to the carrier using a rapid flip-chip machine with limited alignment accuracy. Photoresist can be used to attach the dies. The SOI host wafer can be positioned as well on its carrier using photoresist. Both carrier wafers contain MT-like mechanical alignment structures to position both carriers with respect to each other (see figure 3.57).

After collective cleaning of the dies and the substrate wafer on their carriers, they are brought into the bonding chamber, as shown in figure 3.58. This bonding chamber is very similar to the one proposed in section 3.6, only differing in the springs used to allow a vertical movement of the alignment pins during bonding.

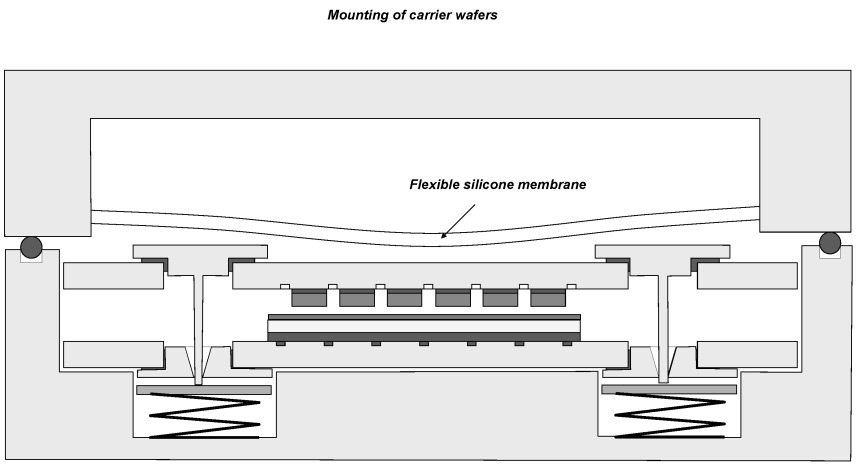


Figure 3.58: Multiple-die bonding mechanism - mounting of carrier wafers

After positioning of the carriers in the bonding chamber, the chamber is evacuated, resulting in a 1 bar pressure from the flexible silicone membrane, attaching the InP dies to the SOI host substrate in a vacuum environment as shown in figure 3.59.

After venting the bonding chamber, no more pressure is exerted on the stack and the InP dies remain attached to the DVS-BCB layer. The InP die carrier releases, as the photoresist used for attachment is thermoplastic and bonding is performed at 150C. After die attachment, pressurized curing with 300kPa pressure is needed to complete the process. This might require a specialized bonding tool containing a compliant layer that can compensate for a possible die thickness non-uniformity and that can allow a shift of the outer dies bonded to the wafer due to the difference in thermal expansion coefficient between the silicon host wafer and the pressure head. When the total InP die area is large, the bonding force that needs to be applied can be high.

In [132], an alternative approach, no longer requiring the carrier wafers is presented. In this work, a glue (poly-ethylene glycol, PEG-2000) is used to temporarily fix the aligned dies to the substrate, after which the wafer is brought into the bonding chamber. Increasing the temperature and evacuating the bonding chamber leads to a complete evaporation of the PEG-2000. Commercial wafer bonding equipment was used in this case. The bonding chamber is schematically shown (for the case of wafer-to-wafer bonding) in figure 3.61. Although this is

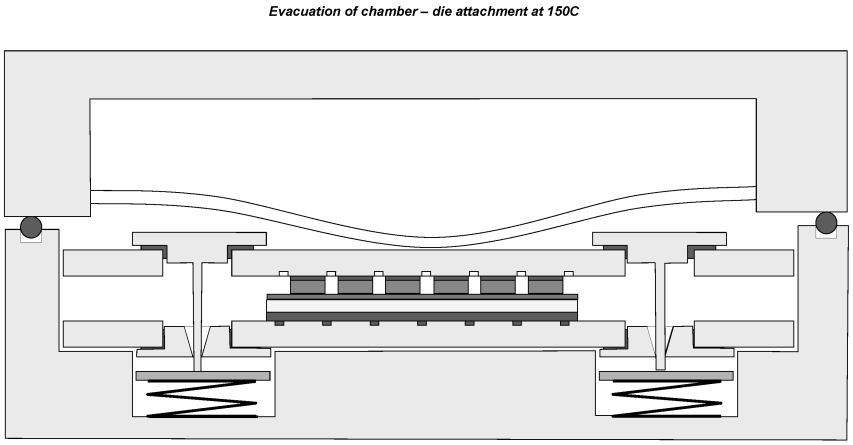


Figure 3.59: Multiple-die bonding mechanism - evacuation of bonding chamber

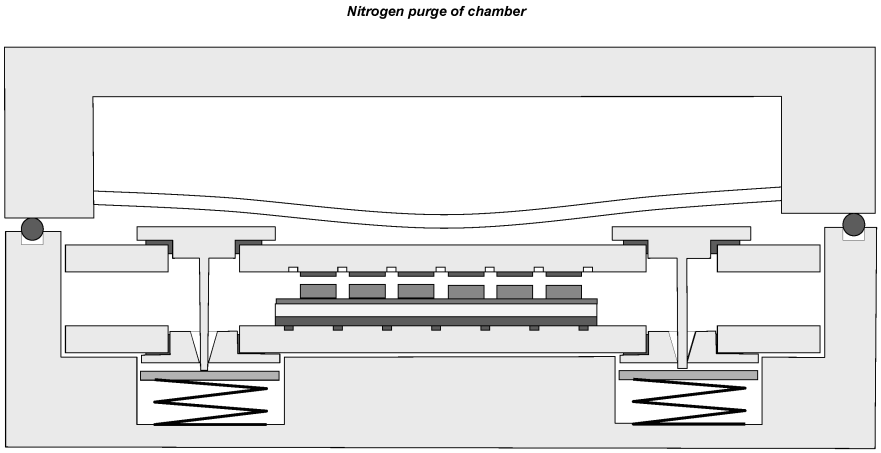


Figure 3.60: Multiple-die bonding mechanism - Nitrogen purge of bonding chamber

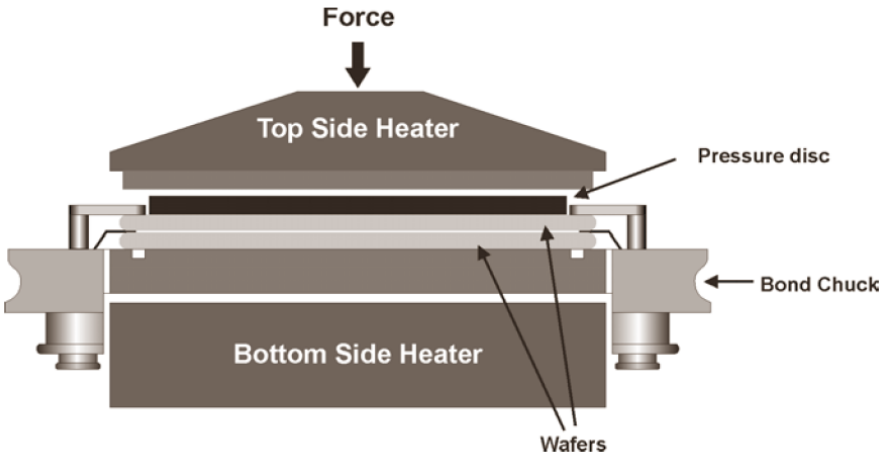


Figure 3.61: Layout of the bonding chamber of a commercial tool (from [133])

a viable approach, the interaction between the PEG-2000 and the DVS-BCB in our case needs to be studied (as in [132] a metal bonding process was used).

3.11 Conclusions

In this chapter we presented the development of a DVS-BCB die-to-wafer bonding process for InP/InGaAsP dies bonded to a processed silicon-on-insulator waveguide wafer. The bonding layer thickness can vary from 300nm to a few μm. Various bonding process characterization methods were developed. A model describing the stress induced in the bonded structures is presented, showing that the induced stress levels are sufficiently low, such that the optical properties of the bonded epitaxial layers remain unchanged. Finally, a multiple-die bonding scheme is proposed, which uses the same bonding technique as the single-die bonding process, developed in the context of this work.

The work presented in this chapter has been the subject of 3 publications in international journals (Appendix B.2-2,B.2-3 and B.2-7).

Chapter 4

Optical coupling schemes

Ain't no easy way
Black Rebel Motorcycle Club

Following a setting of the simulation environment, several types of structures for optical coupling between the active III-V semiconductor layer and the passive silicon-on-insulator waveguide layer will be presented and analyzed. Both coupling structures for in-plane operating devices and for surface-normal operating devices will be discussed. The various coupling schemes presented will be compared and two schemes will be selected for practical realization. Some types of the developed coupling schemes can also be used for coupling light from an optical fiber into a silicon-on-insulator waveguide. This will also be discussed.

4.1 Setting of the simulation environment

4.1.1 Selection of the operation wavelength

The choice of the operation wavelength of the active opto-electronic devices is determined by various factors, including the application, the material system of choice for the passive waveguides and possible interference with other devices such as CMOS transistors. As silicon-on-insulator is a good candidate as a passive waveguide system due to the high refractive index contrast, the operation wavelength has to lie above the band gap wavelength of silicon, being 1.1μm. Although shorter wavelengths could be chosen when using SiN_x waveguides (with a more modest index contrast), this should be avoided because,

when envisaging the integration with CMOS electronics, absorption of scattered light in the transistor layer could lead to a photovoltaic effect in the transistors, leading to a malfunction of the electronics. Considering applications in telecommunication, 1.3μm and 1.55μm are the wavelengths of interest. The choice between 1.3μm at 1.55μm is rather arbitrary and depending on the application, but can be motivated by the lower losses of silicon-on-insulator photonic wires at 1.55μm [134].

4.1.2 Active opto-electronic devices

Vertically operating devices

Vertical cavity surface emitting lasers are attractive due to their small size, the low threshold currents and the fact that the laser beam matches the mode of a single-mode optical fiber. They have emerged as one of the most important semiconductor light sources for numerous applications. This is true without exception for GaAs-based VCSELs with emission wavelengths below 1μm. The development of VCSELs for longer wavelength operation (such as 1.3μm and 1.55μm) suffers from fundamental intrinsic drawbacks of the material systems that are suited for these wavelengths. The low index contrast that can be achieved for defining the Bragg mirrors, the enhanced temperature sensitivity of the material gain in InP-based active regions and the poor thermal conductivity of ternary and quaternary alloys hamper the realization of high-performance lasers. Wafer bonding of an InGaAsP active region and GaAs/AlGaAs Bragg mirrors is an option, but expensive [135]. Only recently, advances have been made in the fabrication of long-wavelength vertical cavity semiconductor lasers [136]. Vertical cavity semiconductor optical amplifiers (VCSOA) [137] suffer from the same problems as the VCSELs and are therefore not the preferred way of heterogeneously integrating an optical amplifier. Moreover, the use of a cavity implies a small optical bandwidth of the device, which is not wanted. Therefore, even if VCSELs would be used as a light source, still an in-plane optical amplifier would be required, which would require developing an additional coupling scheme. Therefore, and due to the early stage of development of 1.55μm VCSELS, these devices will not be discussed in detail in this chapter.

Surface emitting LEDs typically have a low external efficiency due to the low extraction efficiency at the semiconductor/air interface. The spectral bandwidth over which light is emitted is large (which can be wanted or unwanted, depending on the application) and the directio-

nality of the beam is limited. Although resonant cavity LEDs [138] can provide a higher external efficiency and a more directional beam, these sources are also not considered in this work.

At the photodetector side, surface-illuminated devices are often used. Typically, there is a trade off between responsivity and transit time limited bandwidth for small area devices. In large area devices the RC time constant determines the maximum operation speed of the device. Therefore, in the next sections we will investigate the possibility of illuminating the surface of a bonded photodetector with light travelling in an SOI waveguide underneath.

In-plane operating devices

In-plane operating devices are well known in telecommunication as they are more compatible with the planar growth techniques. Different types of side emitting laser diodes exist: basic Fabry-Perot type laser diodes emit a multimode spectrum of laser peaks while a distributed feedback (DFB) and distributed Bragg reflector (DBR) laser diode typically emit at a single wavelength. The polarization control of the emitted light typically is achieved by using strained quantum wells (although already some polarization selection occurs due to the difference in confinement factor and reflection coefficients). Compared to a VCSEL, these types of devices typically have a larger active volume, leading to a higher threshold current and power dissipation.

The use of in-plane operating semiconductor optical amplifiers leads to a large optical bandwidth compared to the vertical-cavity-based device. Its layer structure and device structure are very similar to those of the in-plane operating laser diodes and therefore, when using this type of devices, a fabrication scheme can be envisioned that incorporates both side emitting laser diodes and semiconductor optical amplifiers, using the same layer structure and processing steps.

The use of waveguide-based photodetectors decouples the detection efficiency and the transit time limited bandwidth and are therefore interesting for high speed operation. Again, the layer structure and device layout are very similar to that of in-plane operating laser diodes and semiconductor optical amplifiers.

Selection of the type of devices studied

Due to the fact that the epitaxy for in-plane operating laser diodes is widely available and its fabrication is largely compatible with that of

in-plane optical amplifiers and waveguide-based photodetectors, these types of devices will be studied. On the photodetector side, both waveguide based detectors and surface-illuminated detectors will be used as mode-to-mode conversion is not required in a surface illumination coupling scheme, which can simplify the design of the coupling structure, as will be shown in section 4.5.

4.1.3 Passive waveguide systems

Advantages of high index contrast waveguide systems

As outlined in section 1.1.3, the advantages of using high index contrast waveguide systems are the sharp bends and small waveguide pitches that can be obtained, allowing a high density integration of optical functions. The main omni-directional high index contrast material systems are silicon-on-insulator ($\Delta n = 2$) and Si_3N_4/SiO_2 ($\Delta n = 0.5$). As a higher degree of integration can be obtained in the former material system, we will focus on coupling structures for the SOI waveguide system.

Silicon-on-insulator

The layer structure that is used for silicon-on-insulator waveguides in this work is shown in figure 4.1 and consists of a 220nm silicon core layer (n_{Si}=3.45) on top of a 1μm thick buried oxide layer (n_{SiO_2}=1.45) to prevent leakage of light to the underlying silicon substrate. Only photonic wires are considered, as rib type waveguides do not provide the same lateral high index contrast feature.

The effective index of the lowest order waveguide modes at a wavelength of 1.55μm is shown in figure 4.2 as a function of waveguide width, indicating that waveguides need to be narrower than 0.5μm to be single-mode. As higher order modes can be very lossy, slightly wider waveguides can also be used, showing effective monomodal behavior.

Design and analysis of coupling structures

Unless otherwise stated, a wavelength of 1.55μm will be used in the simulations. The simulations are limited to TE polarization as standard in-plane laser epitaxy emits TE polarized light and due to the fact

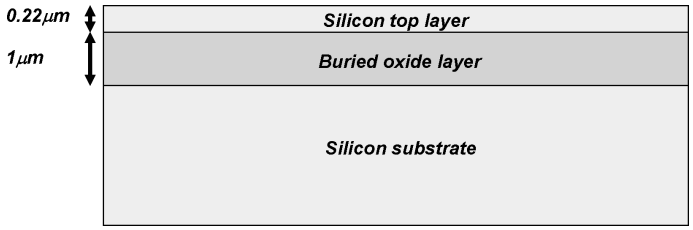


Figure 4.1: SOI layer structure used in simulations

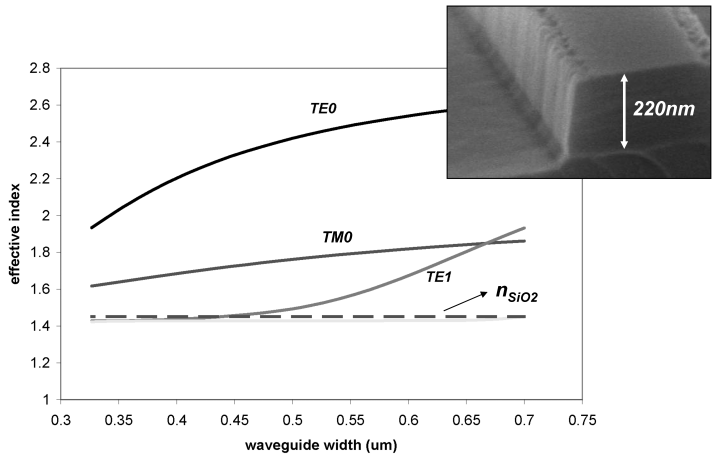


Figure 4.2: SOI waveguide effective index as a function of waveguide width (λ=1.55μm)

that high index contrast waveguide structures inherently are polarization dependent. Therefore, the polarization dependence of the coupling structures is not studied. In case an unknown polarization needs to be processed (as will be the case in telecom applications) a polarization diversity scheme as in [139] can be used.

4.2 Simulation software

4.2.1 Eigenmode expansion method

For the simulation of the coupling structures, an eigenmode expansion method is used. This method is based on the fact that the fields in a waveguide structure, that is invariant in the direction of light propagation, can be written as the sum of a set of eigenmodes, each with a different shape and phase velocity (effective index). At the interface between two sections, transmission and reflection matrices T and R need to be calculated expressing the coupling between both sections, as is shown in figure 4.3. In this way, a waveguide structure can be more efficiently analyzed than with brute force numerical techniques. For three-dimensional calculations, the commercially available software package FIMMWAVE was used, while for two-dimensional calculations requiring perfectly matched layers, which reduce the reflections at the simulation window boundaries, the in-house developed CAMFR tool was used [140].

4.2.2 Finite-difference-time-domain method (FDTD)

The finite-difference-time-domain (FDTD) method is a grid-based differential time-domain numerical modelling method, in which Maxwell's equations are discretized in space and time. The equations are solved in a leapfrog manner: the electric field is solved at a given instant in time and the magnetic field is solved at the next instant in time, and this process is repeated over and over again. FDTD is a versatile modelling technique in time domain. When a broadband pulse is used as the source, then the response of the system over a wide range of frequencies can be obtained with a single simulation. However, since FDTD requires that the entire computational domain is gridded, and the grid spatial discretization must be sufficiently fine to resolve both the shortest wavelength and the smallest geometrical feature, large computational domains can be necessary, resulting in long simulation times. For

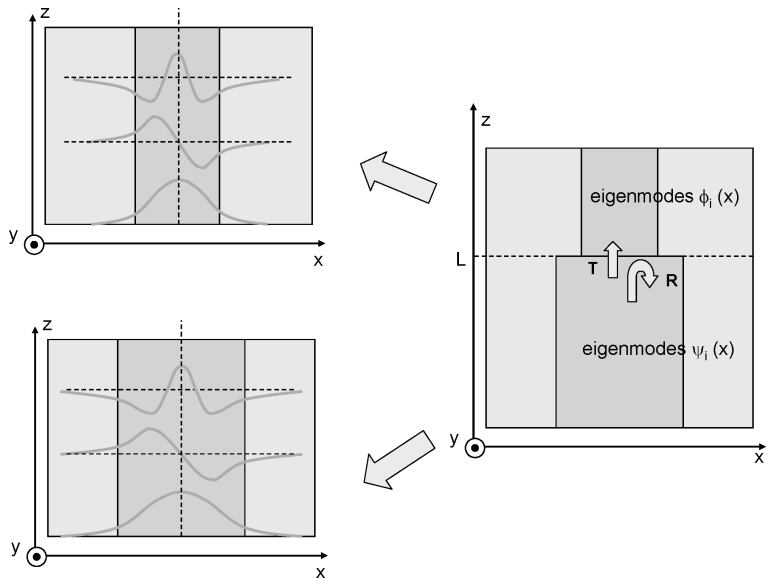


Figure 4.3: Eigenmode expansion method

two-dimensional and three-dimensional calculations, the commercially available OMNISIM package was used.

4.3 In-plane operating devices

In the first part of this section, we will investigate the coupling schemes to couple light to a passive high vertical index contrast InP membrane layer integrated on top of the SOI waveguide layer (directional coupling, tapered coupling, grating-assisted coupling). In a second part, we will argue that ultra-thin active waveguide structures using electrical carrier injection are difficult to obtain and therefore the design of a mode transformer to a low vertical index contrast structure will be proposed. In a third section, other types of mode transformers will be presented, no longer based on the passive InP membrane.

4.3.1 Directional coupling

The concept of a directional coupling scheme is based on the complete and periodic power transfer that occurs between two closely spaced waveguides, which are phase matched, i.e. the fundamental modes of both waveguides have the same effective index.

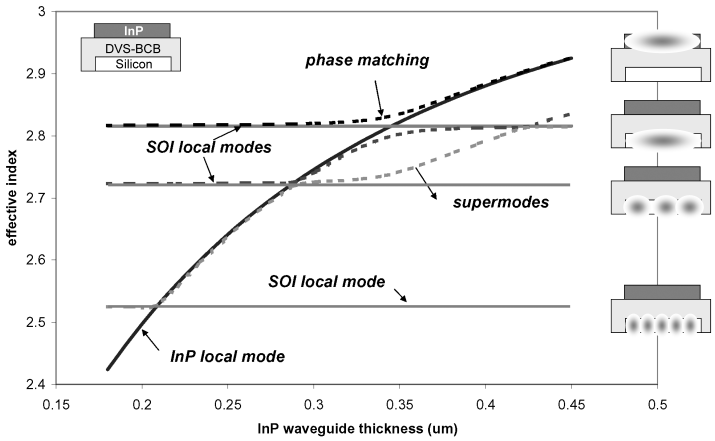


Figure 4.4: Phase matching condition for a vertical directional coupler structure - a field plot of the local mode profiles is also shown

Strictly speaking, the individual waveguide modes do no longer exist in the coupled structure: supermodes are formed that resemble the individual waveguide modes while far away from phase matching, but obtain a particular form when phase matching occurs. The effective index of the local modes and supermodes as a function of InP waveguide thickness is plotted in figure 4.4 for the case of a 300nm DVS-BCB layer in between both waveguide layers. A 3μm wide SOI waveguide and InP membrane waveguide are assumed.

A field plot corresponding to the phase matching condition (achieved for an InP waveguide thickness of 340nm) is plotted in figure 4.5, which shows that a complete power transfer occurs after 24μm.

Although a compact and efficient coupling scheme, the fabrication tolerances are very strict. In figure 4.6, the influence of a deviation of the bonding layer thickness and InP waveguide thickness is shown (design parameters: DVS-BCB thickness of 300nm and an InP waveguide thickness of 340nm). A $\pm$ 10 percent deviation from the design parameters was assumed. While relatively tolerant to bonding layer thickness variations, there is a strong dependence on InP layer thickness variation (which in a practical situation can be up to 10 percent). Therefore, the directional coupling scheme was not considered as a viable coupling scheme.

While not appealing for coupling to passive waveguides, the directional coupling scheme can be used for coupling to a waveguide-based

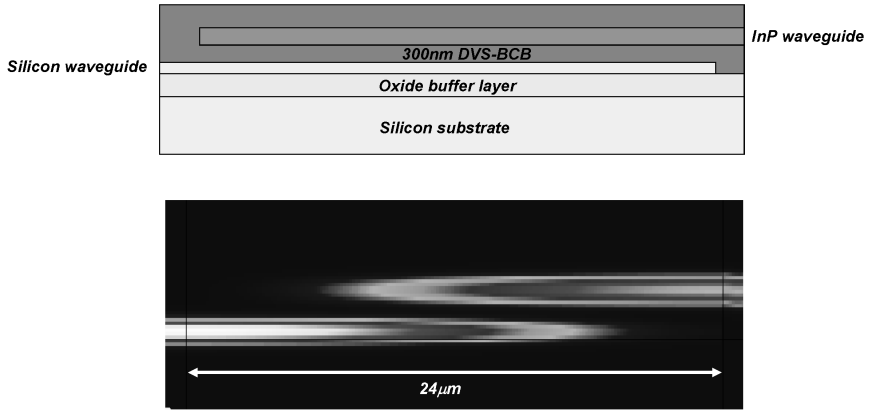


Figure 4.5: Design and field plot of a directional coupler structure

metal-semiconductor-metal (MSM) photodetector, as will be shown in section 7.2. As the waveguide is absorbing in this case, the influence of the epitaxial layer thickness variation is far less severe, as the device length can be increased to accommodate fabrication errors.

4.3.2 Tapered coupling

In order to circumvent the reduction in efficiency by fabrication errors, a tapered coupling scheme can be used as shown in figure 4.8. This coupling scheme is based on the concept of adiabatic tapering: when the dimensions of a waveguide structure vary sufficiently slow along the propagation direction, no power exchange occurs between the modes of the structure. Again, in this case the local modes of the individual waveguides no longer exist and the supermodes of the structure need to be used. The effective index of the supermodes and local modes of the waveguide structure as a function of the SOI waveguide width is plotted in figure 4.7. A 2.5μm wide InP membrane waveguide, which is 280nm thick, is assumed.

When choosing the starting width and the end width of the SOI waveguide taper sufficiently far away from phase matching, the fundamental supermode will resemble the local modes of the individual waveguides. When the tapering is sufficiently slow (so called adiabatic transformation as explained in appendix A), complete power transfer occurs between both waveguide layers. A field plot of the coupling

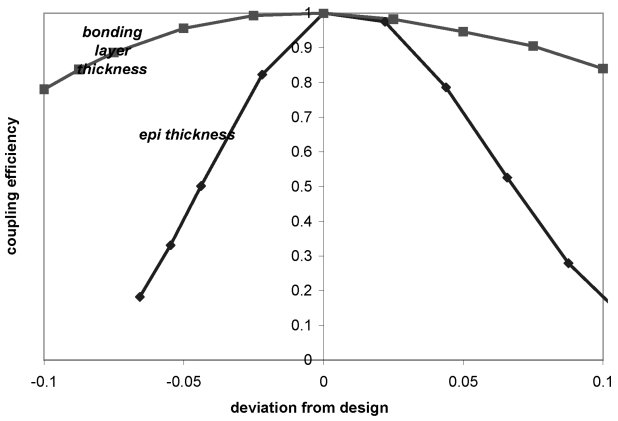


Figure 4.6: Fabrication tolerance of the directional coupler structure - influence of a variation in the bonding layer thickness and InP membrane thickness

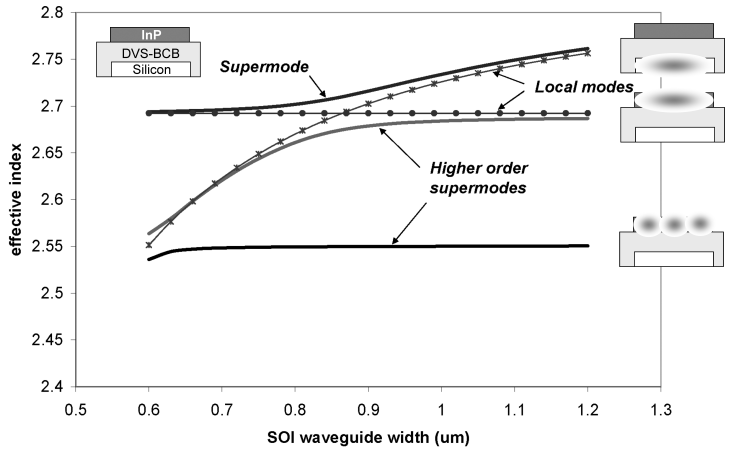


Figure 4.7: Supermodes versus local modes for the adiabatic taper coupling structure - a field plot of the local mode profiles is also shown

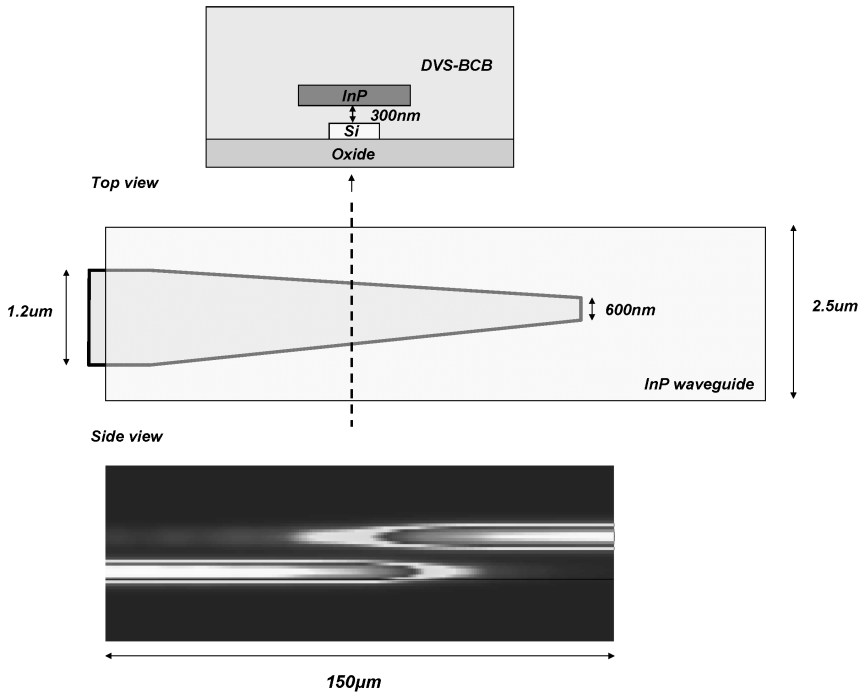


Figure 4.8: Design and field plot of tapered coupler structure

structure is shown in figure 4.8. A linear silicon-on-insulator taper was used.

The influence of the thickness of the InP membrane (which was the most critical dimension in the directional coupler design) and the DVS-BCB bonding layer thickness on the tapered coupler efficiency is shown in figure 4.9. From this picture it is clear that by choosing a sufficiently slowly varying taper, these fabrication errors can be compensated for and the device becomes relatively insensitive to fabrication errors, at the expense of device length.

In principal the first higher order supermode could also be used for coupling. In this case, there is however a chance of parasitic coupling with higher order modes of the InP membrane waveguide as can be seen in figure 4.7 close to the taper tip width of 0.6μm, where the SOI waveguide mode starts to couple with the second higher order local mode of the InP membrane waveguide.

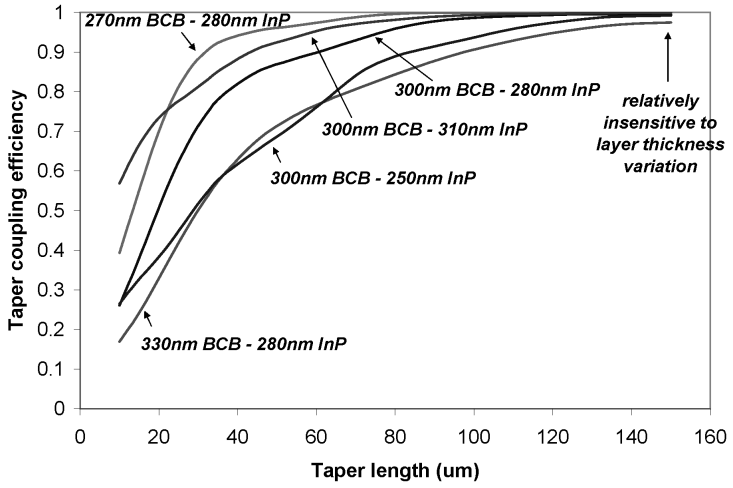


Figure 4.9: Influence of DVS-BCB thickness and InP membrane waveguide thickness variation on the coupling efficiency of a tapered coupler

4.3.3 Grating-assisted coupling

One-dimensional periodic structures: waveguide gratings

One-dimensional periodic structures defined in a waveguide structure allow a power exchange between particular modes of the structure. This power exchange is described by the projected Bragg condition. The Bragg condition starts from the definition of a vector **K**, which lies along the direction of periodicity of the grating and is defined by

$$K = \frac{2\pi}{\Lambda} \tag{4.1}$$

in which Λ is the period of the grating.

If we plot a **k**-vector diagram with the wavevectors of the guided modes and the continuum of radiation modes (depicted as half a circle in the upper and lower space in figure 4.10), the coupling caused by the grating between the incident light (in this case the fundamental waveguide mode of the silicon-on-insulator waveguide) and the other modes of the system can be calculated by evaluating the values of k_x, with

$$k_x = -\beta_{\mathrm{mod}} + mK \quad with \quad m = ..., -2, -1, 0, 1, 2, ... \tag{4.2}$$

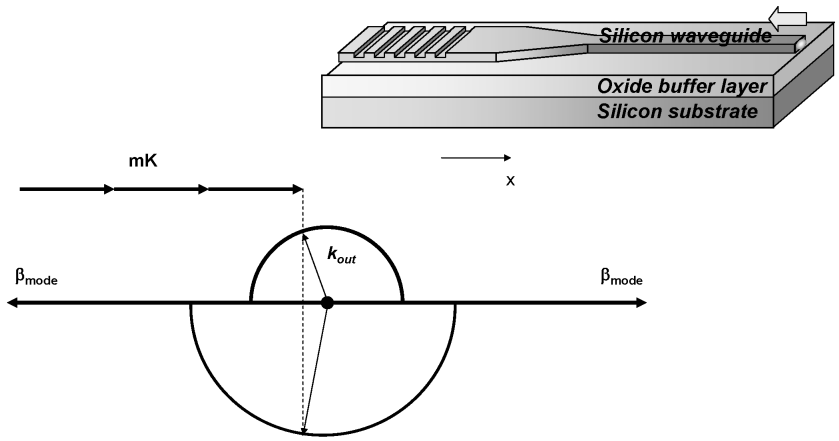


Figure 4.10: Bragg condition for one-dimensional periodic structures

for which there exists a mode of the system, with a wavevector having a k_x component, which matches with equation 4.2. These are the modes to which power can be coupled. The strength of the coupling is determined by the index contrast of the grating and the strength of the m-th Fourier component in the Fourier expansion of the periodic grating dielectric function (a large component means a strong coupling and vice versa).

Coupling to radiation modes

By tuning the period of the waveguide grating, coupling of the incident light with plane wave modes can occur, which travel along a direction defined by the grating period, as is clear from the geometric construction in figure 4.10. If one can fabricate a pair of matched grating couplers, one in the silicon-on-insulator waveguide and one in the InP membrane waveguide, light can be coupled between both waveguides using these radiation modes. The design of the grating coupler periods can be chosen such that light in both waveguides travels in the same direction or in opposite direction, as is shown in figure 4.13. The wavevector diagram for both gratings for the case of coupling in the opposite direction is plotted in figure 4.11.

This type of coupling scheme allows a large separation between both waveguide layers, which can simplify the bonding process. The

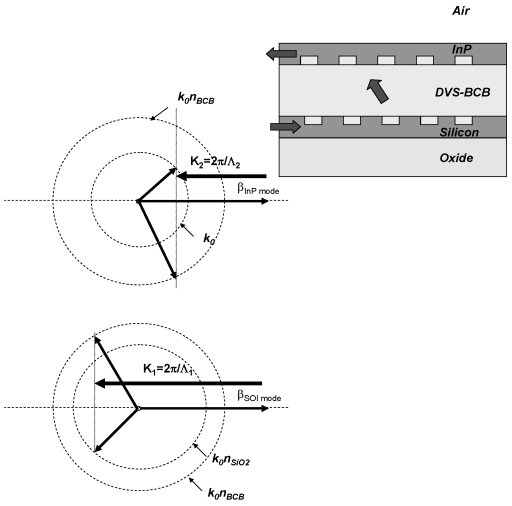


Figure 4.11: Wavevector diagram for matched coupling to radiation modes

coupling efficiency is determined by the directionality D of the grating (being the ratio of the fraction of light that is coupled towards the matching grating to the total diffracted power), the matching of the coupling constants κ_1 and κ_2 of both gratings and the matching of the diffraction angle and can, for the case of coupling in opposite direction, be written as

$$\eta = D_1 D_2 \left| \int_0^L \sqrt{\kappa_1 \kappa_2} \exp(\frac{-\kappa_1 x}{2}) \exp(\frac{-\kappa_2 x}{2}) \exp(-j2k_0 n_{BCB} \sin(\alpha_0) \sin(\varepsilon) x) dx \right|^2 \tag{4.3}$$

with α_0 the nominal angle of light diffraction for both gratings and $\frac{\varepsilon}{2}$ the difference in effective diffraction angle. For the case of coupling in the same direction the coupling efficiency is lower, as there is a mismatch in the diffracted field profile from both gratings. This structure will therefore not be treated here.

Assuming identical coupling constants and a nominal diffraction angle of about 90 degrees (not exactly 90 degrees to avoid a large second order reflection of the grating), we can calculate the influence of a diffraction angle mismatch on the obtainable coupling efficiency. This is plotted in figure 4.12.

To assess the fabrication tolerance of the optical coupling scheme, one can calculate the influence of an error in the thickness of the waveguides and an error in the grating etch depth, on the diffraction angle

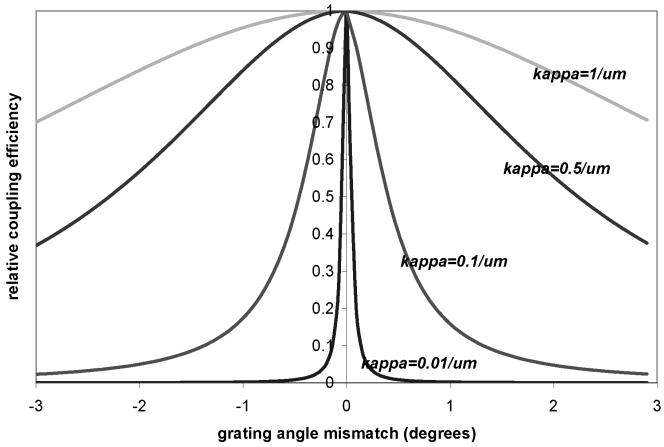


Figure 4.12: Influence of the diffraction angle mismatch on the coupling efficiency for different grating coupling constants

α. This was done for a nominally 220nm thick SOI waveguide with a grating period of 630nm (duty cycle 50 percent) and a nominal etch depth e of 70nm, resulting in a coupling constant of $0.22\mu\text{m}^{-1}$.

$$\begin{cases} \frac{\partial\alpha}{\partial t_{SOI}} = \frac{2.9^\circ}{10nm} \\ \frac{\partial\alpha}{\partial e} = -\frac{1.7^\circ}{10nm} \end{cases} \tag{4.4}$$

From this analysis it is clear that this type of coupling structure has tight fabrication tolerances, as typically the grating coupling constant is below $0.5\mu\text{m}^{-1}$. Moreover, a high directionality of both gratings is needed to obtain a large coupling efficiency.

Other types of grating couplers

Besides coupling to radiation modes, other types of grating couplers can be envisaged. Contra-directional (or co-directional) coupling between the guided modes of the SOI waveguide and InP membrane can be achieved, as is shown in figure 4.13.

The Bragg condition for the gratings is plotted in figure 4.14. Due to the high vertical index contrast, this type of devices however requires thin bonding layers and leads to long structures with a small optical bandwidth, which is not wanted for practical applications.

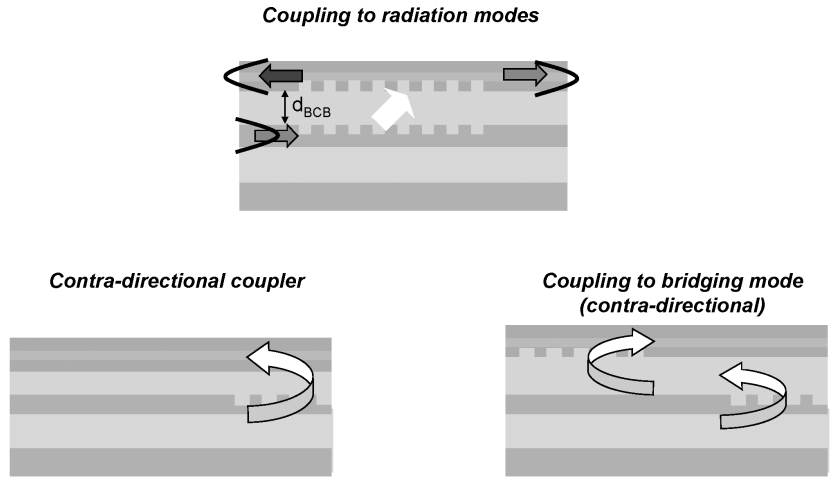


Figure 4.13: Grating-assisted coupling schemes

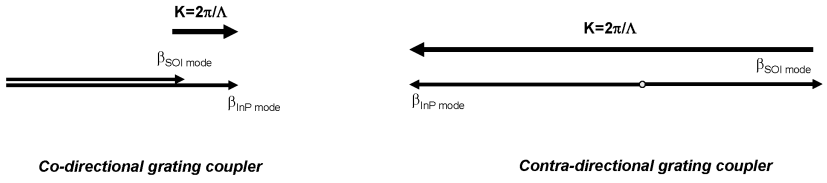


Figure 4.14: Bragg condition for a grating-assisted directional coupler

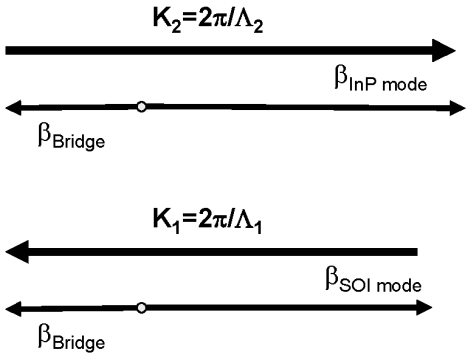


Figure 4.15: Bragg condition for contra-directional coupling to a bridging mode

Coupling to bridging modes

A larger waveguide spacing compared to the contra- or co-directional coupler can be achieved by coupling to a bridging mode [141], as shown in figure 4.13, which is an optical mode that is predominantly concentrated in the DVS-BCB bonding layer. An example of such a mode is plotted in figure 4.16. The Bragg condition for the case of contra-directional coupling is depicted in figure 4.15. However, due to the high vertical index contrast, again long structures are needed and low optical bandwidth is obtained.

4.3.4 Ultra-thin active waveguides

Rationale

In previous coupling designs, light was coupled to an ultra-thin III-V waveguide. Question remains wether this waveguide can be made active. This requires changing the epitaxial layer structure of the membrane layer and injection of carriers in the active layer. Both optical pumping and electrical pumping can be used for carrier injection.

Optical pumping

Carriers can be injected in the III-V waveguide by illuminating the area with light having a photon energy larger than the band gap of the active layer. This light can either be injected through the SOI waveguide (or through a polymer waveguide on top) or by surface illumination, as is

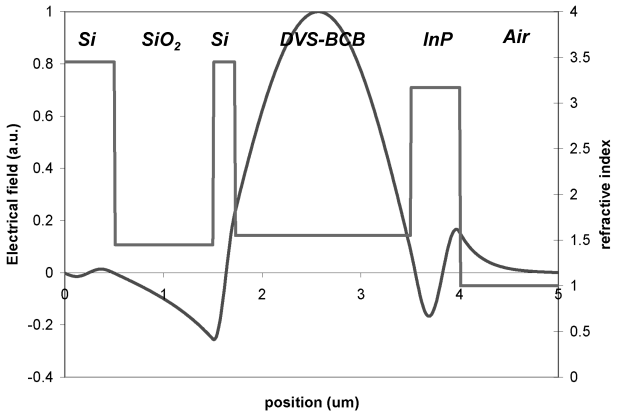


Figure 4.16: Electric field of a TE bridge mode and the associated refractive index profile

shown in figure 4.17. The question remains if optical injection (using an off-chip light source) is viable for practical applications, which depends on the type of application and the number of active structures that need to be pumped.

Electrical injection

The electrical injection of carriers in the active layer structure requires the definition of a pin-layer structure. In planar waveguide technology this is a vertical pin-structure and requires p-type and n-type ohmic contacts. Different electrical injection schemes are presented in figure 4.18.

Standard top and side contacting of the active InP/InGaAsP membrane leads to large metal absorption losses due to the absorption in the p++ InGaAs contact layer and p-type TiAu contact. These absorption losses can be reduced by incorporating a tunnel junction [58] so only n-type contacts would be needed, but losses are still unacceptably high, as shown in figure 4.19, where the losses of the TE fundamental slab waveguide mode of a DVS-BCB bonded InP membrane waveguide with a gold top contact (for the case of an n-type top contact with incorporated tunnel junction) and a standard InGaAs(20nm) - Ti(30nm)-Au(150nm) p-type top contact are shown (the losses due to doping of the structures is neglected). From this simulation several conclusions can be drawn. The loss is dominated by the InGaAs contacting layer

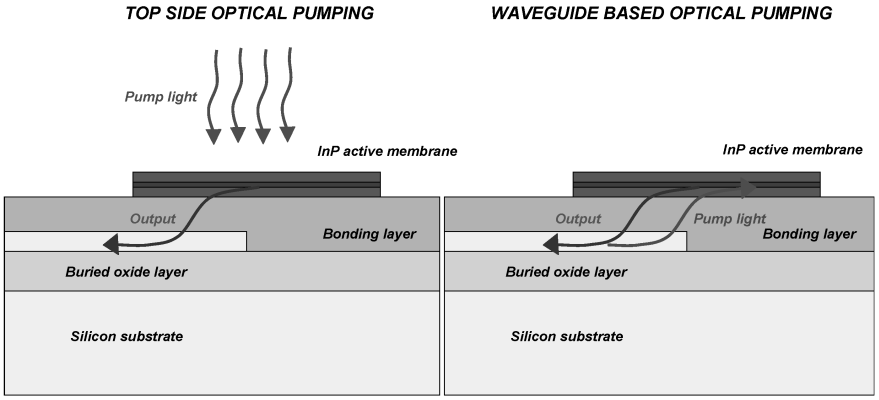


Figure 4.17: Optical pumping of bonded active devices: top side optical pumping and waveguide-based optical pumping

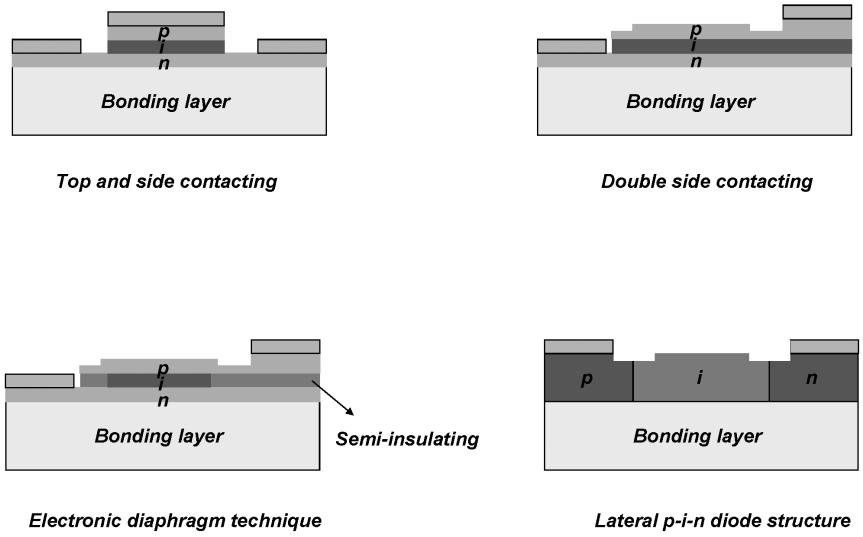


Figure 4.18: Electrical injection schemes: top and side contacting scheme, double side contacting scheme, electronic diaphragm technique and lateral pin-diode structure

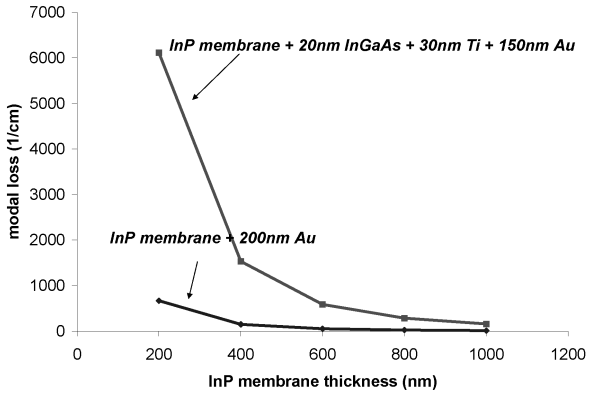


Figure 4.19: Optical losses in a metal-clad high vertical index contrast slab

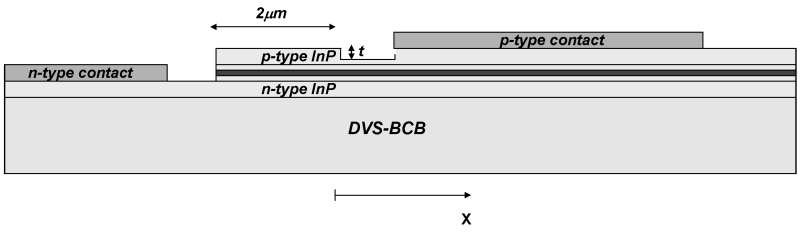


Figure 4.20: Structure of the double side contacting scheme

and titanium adhesion layer needed to achieve a good electrical contact. The modal loss is in the order of 4000/cm for a 300nm InP membrane (a typical thickness needed for phase matching with an underlying silicon waveguide), which is unacceptably high. Losses are reduced by using a tunnel junction approach, but are still very high.

These losses can be avoided by shifting the p-type top contact as shown in figure 4.20. In figure 4.21, the loss of the fundamental mode as a function of the etch depth t of the p-type top cladding layer, is shown. A 100nm InGaAsP core layer, consisting of two 25nm thick InGaAsP separate confinement layers (band gap wavelength 1.25μm) and a 50nm InGaAsP active layer (band gap wavelength 1.55μm), sandwiched between a 100nm InP top cladding layer and a 100nm InP bottom cladding layer is assumed. The p-type contact consists of a 20nm thick InGaAs contact layer, a 30nm thick titanium adhesion layer and a 150nm thick gold contact. While deep etching reduces the losses due

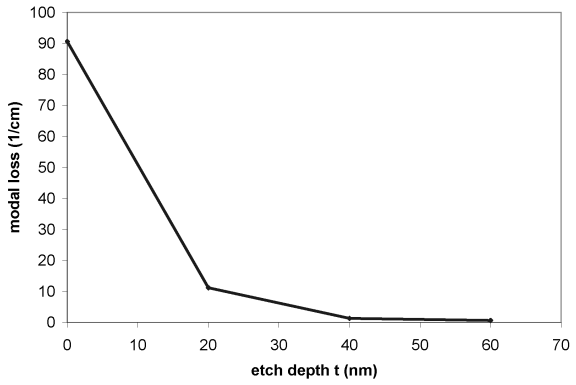


Figure 4.21: Optical losses in double side contacting scheme

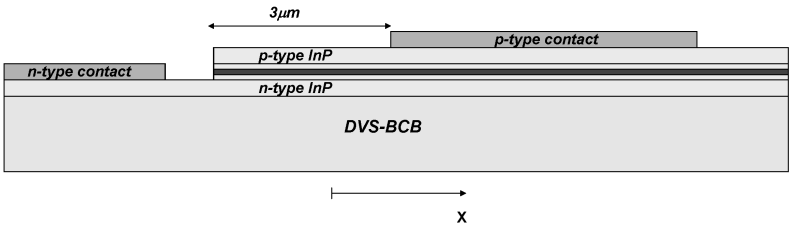


Figure 4.22: Electrical injection scheme to reduce modal losses due to contacting

to stronger lateral optical confinement, the etch depth has to be kept small to avoid low carrier injection efficiency underneath the ridge waveguide.

The injection efficiency in the active layer underneath the waveguide rib was calculated using the finite element simulation tool DESSIS [142], solving the governing electron and hole continuity equations. The layer structure is identical to the one described above. The electrical contacts are placed as shown in figure 4.22. 1μm separation between the n-type contact and the waveguide edge was chosen. The etch depth t is assumed to be zero, in order not to further reduce the injection efficiency. A contact resistivity of $5 \times 10^{-5}\Omega cm^2$ is assumed, both for n-type and p-type contacts. A surface recombination velocity at the InGaAsP/air interface of $5 \times 10^5 cm/s$ is used.

The carrier concentration in the active layer is plotted in figure 4.23, for different combinations of acceptor and donor doping concentra-

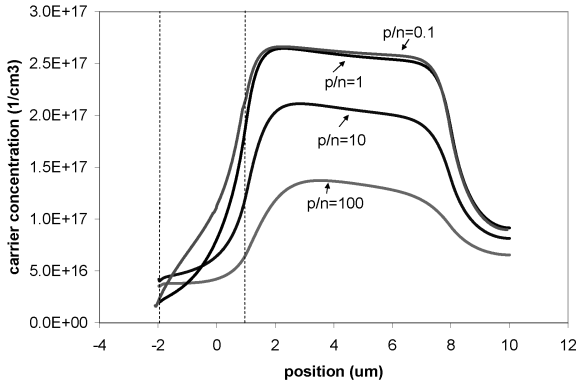


Figure 4.23: Carrier concentration distribution in the double side contacting scheme for various ratios of the p and n-type doping - the optical mode is located in between the two vertical dashed lines

tions in the p-type and n-type InP cladding layers respectively. The injection efficiency is defined as the ratio of the integral of the carrier concentration function underneath the ridge waveguide and the integral of the total carrier concentration function. A typical injection efficiency of 10 percent is obtained. As most of the carriers are concentrated below the p-type contact, the gain experienced by the optical mode, which is located besides the electrical contact, is limited.

This can be circumvented using an electronic diaphragm (see figure 4.18), by regrowing a semi-insulating InP layer outside the waveguide region. This requires a pre-bonding regrowth step (as post-bonding regrowth would require too high temperatures for an adhesive bond), which means that an aligned bonding process would need to be developed to position the processed InP/InGaAsP epi-structure onto the processed SOI substrate.

This pre-bonding regrowth can be avoided by local proton implantation for effective electrical isolation of the InP/InGaAsP active layer [143]. Effectively controlling the implantation depth to the thin active region in an active InP/InGaAsP membrane, while maintaining highly conductive cladding layers, is difficult however.

Another option would be to define a lateral pin-junction by dopant implantation (see figure 4.18). However, this type of electrical injection scheme suffers from the same drawbacks as the electronic diaphragm technique, as high temperature annealing is required to activate the implantation and this has to be done prior to bonding.

From this discussion we can conclude that the fabrication of an ultra-thin electrically injected active membrane is difficult. Therefore, we will focus in the next section on a mode transformer structure to adiabatically transform the high vertical index contrast waveguide mode to a low vertical index contrast waveguide mode, for which electrical injection is readily achievable.

4.3.5 Mode transformation: high vertical index contrast to low vertical index contrast

Rationale

As discussed in the previous section, electrically injected ultra-thin active waveguides are difficult to achieve. Therefore, a mode transformation structure can be designed to couple light from a high index contrast passive III-V waveguide to a low vertical index contrast thick active III-V waveguide. This simplifies electrical injection using a standard top and side contacting scheme.

Design aspects

A lateral taper structure was designed for performing this mode transformation. The layout of the coupling structure is shown in figure 4.24. Important parameters of the design are the required taper tip width (to achieve a high coupling efficiency between the taper waveguide mode and the InP membrane waveguide mode), the length and the optimal shape of the taper structure.

The influence of the taper tip width on the coupling efficiency of the mode transformer is shown in figure 4.25, for two different InP membrane thicknesses. From these simulation results, we can conclude that taper tip widths of 300nm are required for efficient coupling.

The optimal taper design was derived based on the criterion of Love as explained in appendix A and is plotted in figure 4.26. This optimal taper shape can be approximated by a piecewise linear structure as schematically shown in figure 4.24. Three-dimensional eigenmode expansion simulations show that adiabatic conversion is obtained for a taper length of 100μm.

The fabrication of the taper tips (and especially the large aspect ratio) can be a cause of concern for these type of mode transformers. From a lithography point of view standard contact lithography will not be sufficient for defining the taper tip due to its limited resolution. The use

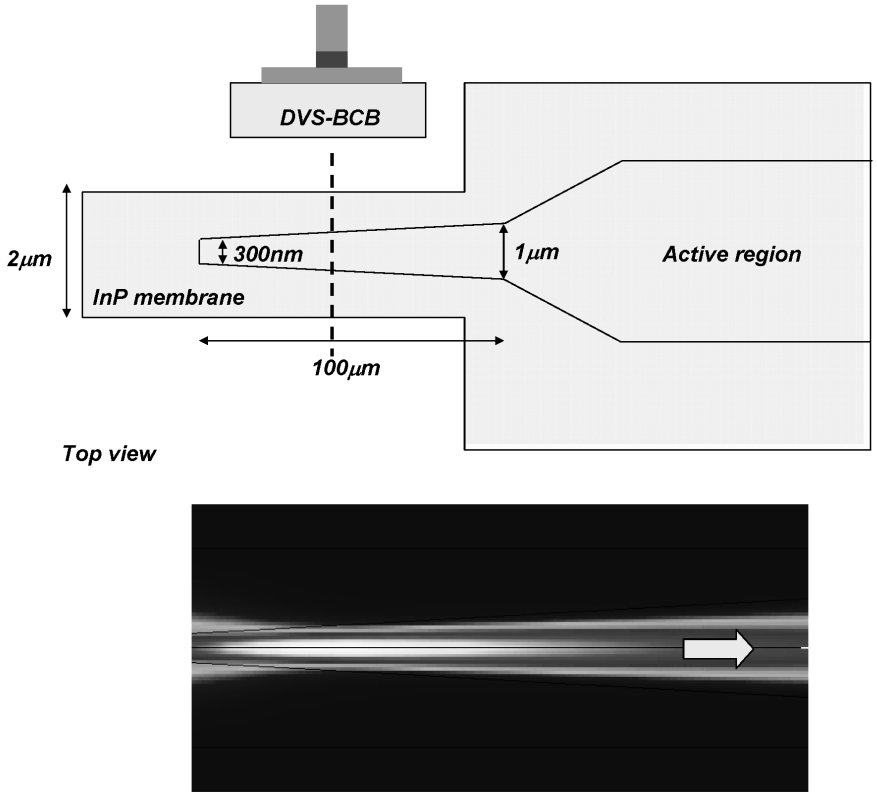


Figure 4.24: Design and field plot of mode transformer structure

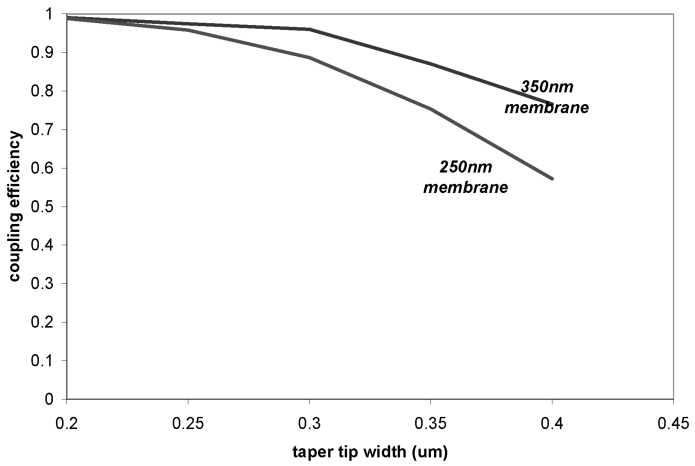


Figure 4.25: Influence of taper tip width on the coupling efficiency of the mode transformer

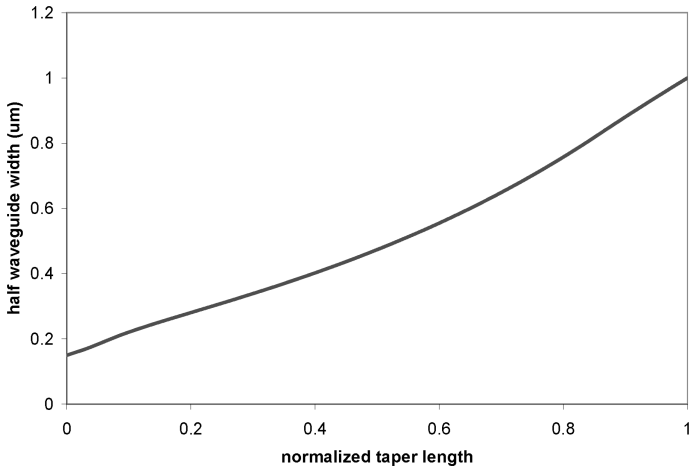


Figure 4.26: Optimal shape of mode transformer as calculated by the adiabaticity criterion of Love

of 248nm deep UV lithography or the use of the knife edge technique [144] can circumvent this problem. Due to these fabrication issues and the fact that, in order to define a laser cavity, additional processing is needed to define a reflector, another type of coupling structure will be analyzed in the following section, based on a polymer waveguide layer.

4.3.6 Coupling structures using a polymer waveguide layer

Rationale

The effective index of the SOI slab waveguide mode (n=2.82) is lower than the material refractive index of InP (n=3.17). The consequence is that thin III-V membranes layers are needed to couple light between both material systems, which are difficult to pump electrically and mode transformers are required to gradually transform the III-V membrane to a thick active membrane, as was discussed in the previous sections.

Another approach is to abruptly change the effective index in the thick III-V membrane layer while maintaining high coupling efficiency, which additionally results in a (un)wanted reflection due to the change in refractive index. This can be done by butt-coupling a thick active membrane with a polymer waveguide. Now the effective index of the polymer waveguide mode is lower than that of the SOI slab mode and coupling can be achieved by changing the dimensions of the SOI waveguide.

Based on the previous discussions, adiabatic mode transformation shows the best performance and fabrication tolerance. Therefore, we will design a coupling structure based on butt-coupling of a thick active membrane to a polymer waveguide and use an adiabatic taper approach to transform the polymer waveguide mode to the SOI waveguide mode, as shown in figure 4.28 and figure 4.32.

Design of the coupling structure

The design of the coupling structure consists of optimizing the butt-coupling at the interface between the III-V active waveguide and polymer waveguide and the design of the adiabatic taper.

The butt-coupling efficiency from the bonded III-V waveguide to the polymer waveguide structure was assessed. The InP/InGaAsP layer stack consists of a 600nm n-type InP bottom cladding, four InGaAsP quantum wells with a band gap wavelength of 1.55μm in between two separate confinement layers of 150nm (bandgap wavelength 1.25μm)

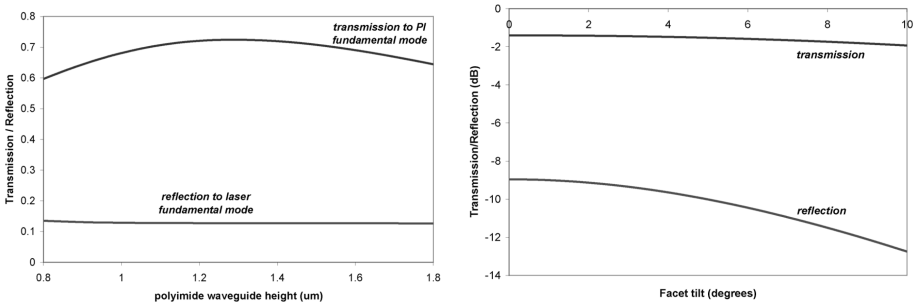


Figure 4.27: Butt-coupling efficiency at the III-V/polymer interface as a function of polymer waveguide height and facet angle

and a 2μm p-type InP and 150nm p++ InGaAs contact layer. The polyimide (n=1.69) waveguide core height was designed for an optimal coupling between the fundamental III-V waveguide mode and the polymer waveguide mode. The coupling efficiency from III-V to polymer waveguide and reflection of the III-V waveguide mode is plotted in figure 4.27. A DVS-BCB cladding layer for the polymer waveguide is assumed. Waveguides were assumed to be 3μm wide. Calculations were based on a three-dimensional fully vectorial eigenmode expansion method. A coupling efficiency of -1.4dB (72 percent) is obtained at an optimum polyimide waveguide height of 1.3 μm. About -0.6dB (12 percent) is due to the reflection at the polymer/III-V interface.

The influence of the quality of the facet etching process (namely the influence of a residual tilt of the etched facet) on the coupling efficiency to polymer waveguide and power reflection of the III-V waveguide mode was also assessed and is shown in figure 4.27. From this simulation, it is clear that the facet tilt has to be kept below 4 degrees from vertical to maintain high transmission and reflection.

Two types of coupling schemes were designed, one based on a standard DVS-BCB bonding approach and one based on an ultra-thin DVS-BCB approach.

The design based on the ultra-thin DVS-BCB bonding is schematically depicted in figure 4.28. As the butt-coupling efficiency optimization resulted in an optimal polyimide core height of 1.3μm, this core height will be assumed in the analysis of the adiabatic taper structure.

While no tapering occurs in the polymer waveguide structure, the SOI waveguide structure tapers down to a narrow tip to achieve good coupling efficiency at the taper tip/polymer waveguide interface [145].

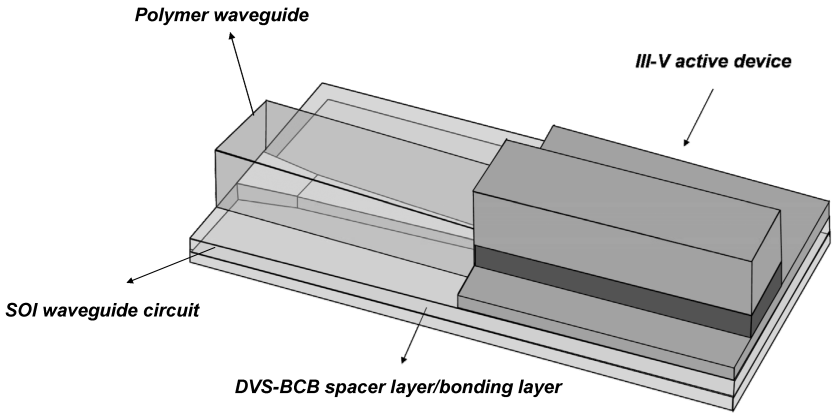


Figure 4.28: Adiabatic-taper-based coupling scheme using a polymer waveguide and an ultra-thin bonding layer

The influence of the taper tip width on the coupling efficiency is plotted in figure 4.29. A DVS-BCB bonding layer thickness of 300nm is assumed. From this simulation it is clear that, in order to achieve high coupling efficiency, a taper tip width below 200nm is needed.

The optimal taper shape was derived based on the adiabaticity criterion of Love as explained in appendix A and is shown in figure 4.30. A taper tip width of 180nm was assumed, which is about the limit of what can be defined using standard 248nm deep UV lithography (see section 5.4.4). This optimal taper shape can be approximated by a piecewise linear taper. A taper length of 200μm is needed to adiabatically transform the polymer waveguide mode to the silicon-on-insulator waveguide mode. A field plot of the optimized coupling structure is plotted in figure 4.31.

As this inverse adiabatic taper scheme relies on ultra-thin DVS-BCB bonding, an alternative coupling scheme based on standard DVS-BCB bonding was designed. As standard DVS-BCB bonding would imply a too large separation between polyimide waveguide and SOI taper structure, the waveguide modes would be completely decoupled and the previously presented adiabatic taper approach would fail.

Therefore, we present here a double adiabatic taper structure in which the DVS-BCB bonding layer is also used as a waveguide layer as is shown in figure 4.32. After butt-coupling of the III-V active component to a polymer waveguide, this polymer waveguide mode is adi-

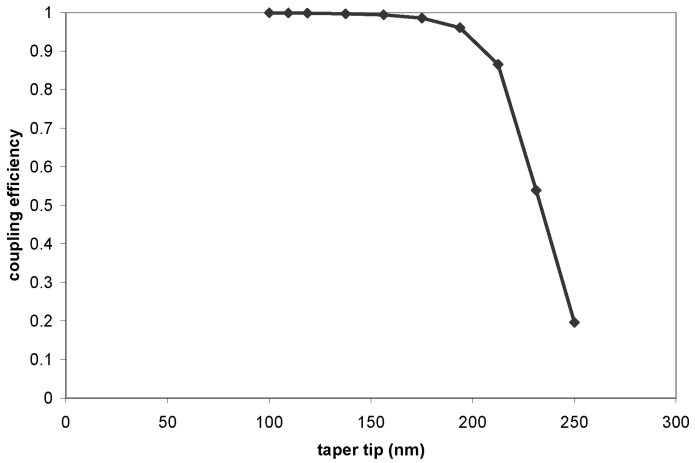


Figure 4.29: Influence of the SOI taper tip width on coupling efficiency (a polymer waveguide of 3μm wide is assumed)

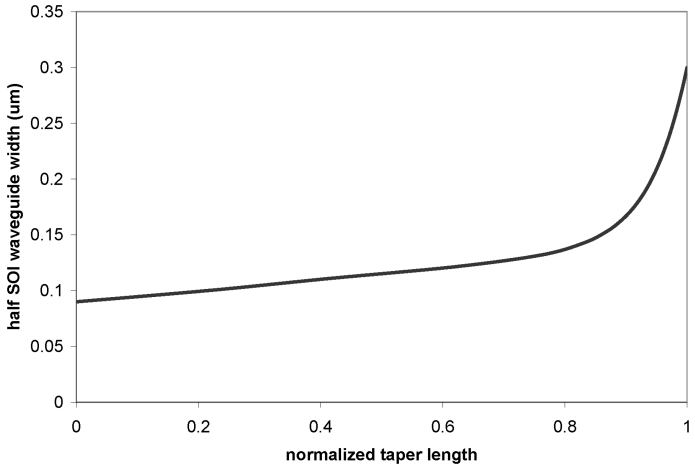


Figure 4.30: Optimal SOI inverted taper shape

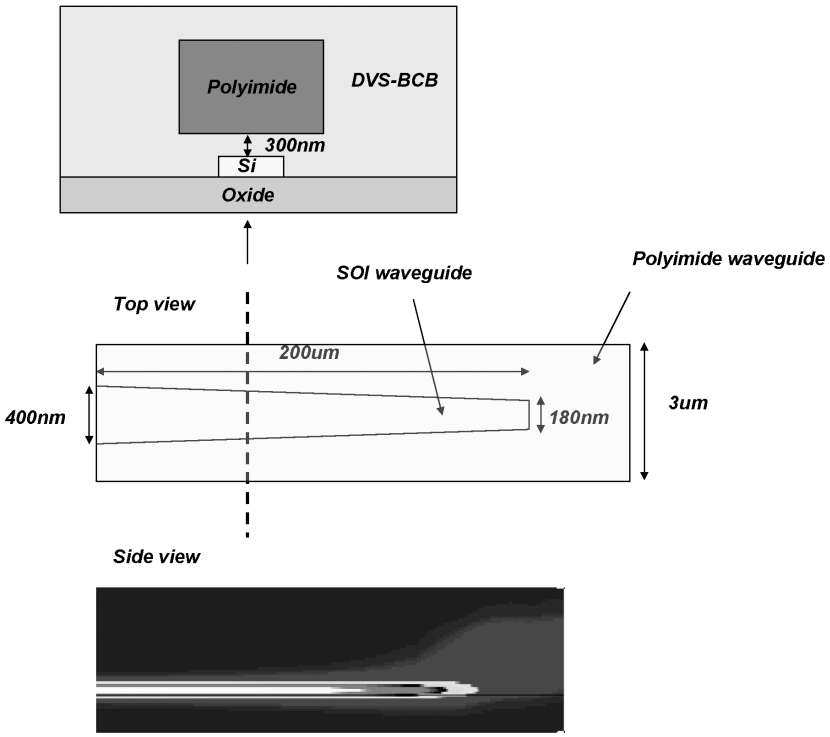


Figure 4.31: Design and field plot of SOI taper coupling structure

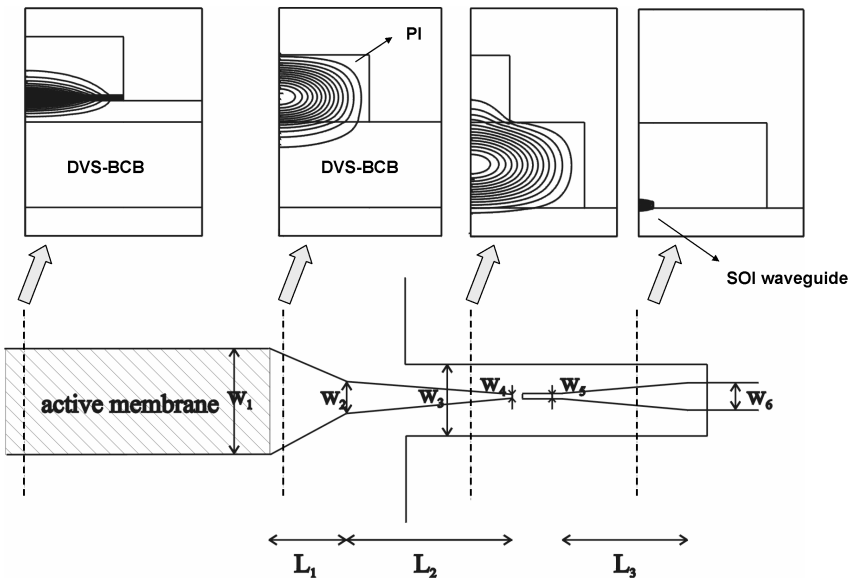


Figure 4.32: Adiabatic taper coupling scheme for thick bonding layers

abatically transformed to the DVS-BCB waveguide mode, after which an inverted SOI taper is used to adiabatically transform the DVS-BCB waveguide mode to the fundamental SOI waveguide mode.

We analyzed this taper structure in [146]. From a fabrication point of view, this double taper structure is less appealing, as more processing steps are needed for fabrication and the required SOI taper tip width is reduced to 50nm due to the strong coupling between the DVS-BCB waveguide and the silicon-on-insulator waveguide. Although this can be circumvented by adding an SiO_2 spacer layer between the SOI waveguide and the polymer waveguide (again adding processing), the total length of the device (typically 400-500μm) is an additional hurdle to integrate this coupling scheme.

4.3.7 Coupling to radiation modes using beveled facets

Rationale

Previously, grating coupler structures were presented to couple guided light to radiation modes. Another way to couple light to radiation modes is to use a beveled facet [147, 148]. To avoid substantial free

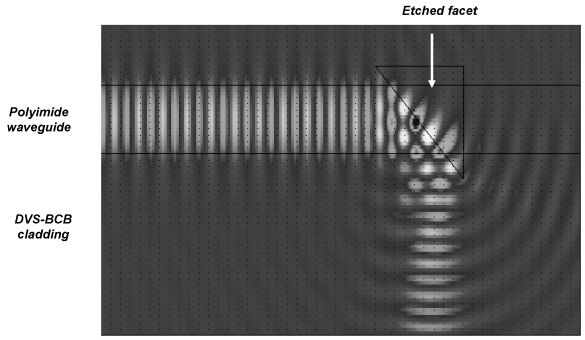


Figure 4.33: Field plot of a 45 degree angled facet in a polymer waveguide

space diffraction (which makes the coupling problem more difficult) the waveguide mode needs sufficiently large lateral and transversal dimensions. Beveled facets can therefore only be used on thick active membranes or on the polymer waveguide structures used in the previous section. This coupling is very efficient in the total internal reflection regime. A field plot of this type of structure is shown in figure 4.33.

In the SOI waveguide layer we can still use a grating coupler to deflect the light. The schematic coupling structure layout is shown in figure 4.34. Due to the particular nature of the coupling structures, the grating coupler required for coupling, needs to be designed for the opposite polarization as the laser diode. For the fabrication of a laser diode, the choice of fabricating the beveled facet in the InP/InGaAsP or in a polymer waveguide is determined by the type of laser diode that is fabricated: in a DFB laser diode, the beveled facet no longer has to supply reflection into the laser cavity, thereby relaxing the fabrication tolerances of the beveled facet. In this case the beveled facet can be fabricated in the InP/InGaAsP layer. For a Fabry-Perot type laser diode this beveled facet has to provide reflection when fabricated in the InP/InGaAsP layer and the 45 degree angle of the facet is therefore more critical. In that case, a beveled facet in a butt-coupled polymer waveguide is preferable (while the reflection into the laser cavity is provided by the polymer/III-V interface).

In these basic configurations shown in figure 4.34 the laser diodes are positioned perpendicular to the SOI waveguide. This results in a low coupling efficiency using a standard grating coupler structure due to the second order reflection of the grating. As discussed above, non-perpendicular incidence on the grating supplies higher grating coupler

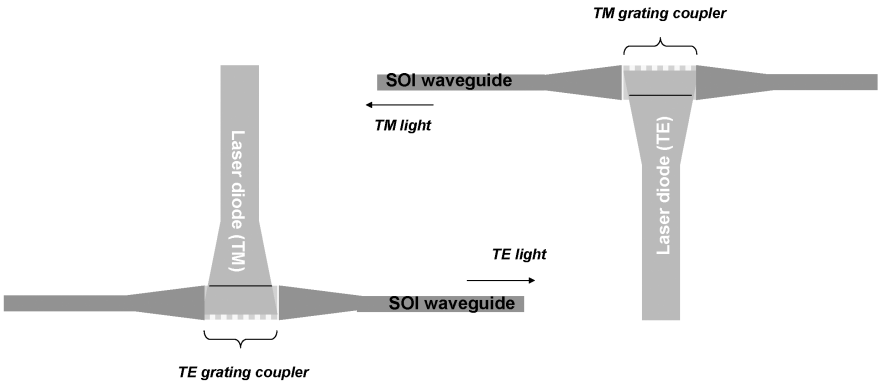


Figure 4.34: Coupling structure layouts based on 45 degree angled facets

efficiency, by avoiding this strong second order reflection. This can be accomplished by rotating the laser diode by an angle α, as shown in figure 4.35, while keeping the parameters and orientation of the beveled facets identical (i.e. etched under an angle of 45 degrees).

The corresponding angle of incidence θ on the SOI grating with respect to the surface normal of the SOI plane, is then given by

$$\sin(\theta) = \frac{n_a}{n_b} \sin(\alpha) \tag{4.5}$$

taking into account the refraction at the interface between bonded laser diode (refractive index n_a) and the bonding medium (refractive index n_b). The coupling structure is schematically represented in figure 4.35.

Tilting the laser diodes reduces the reflection into the laser diodes and can therefore only be used for DFB-type laser diodes (or by forming a reflector structure in the SOI layer). As will be shown in section 4.6.5, it is possible to design the SOI grating structure to achieve high waveguide coupling efficiency for perpendicular incidence by making the grating structure asymmetric. This could avoid the use of the angled waveguides.

Although efficient coupling can be expected over a relatively large wavelength range, this type of coupling structure was not developed in this work. This is mainly related to the question wether the fabrication of beveled facets is a sufficiently developed technique, suitable for mass fabrication.

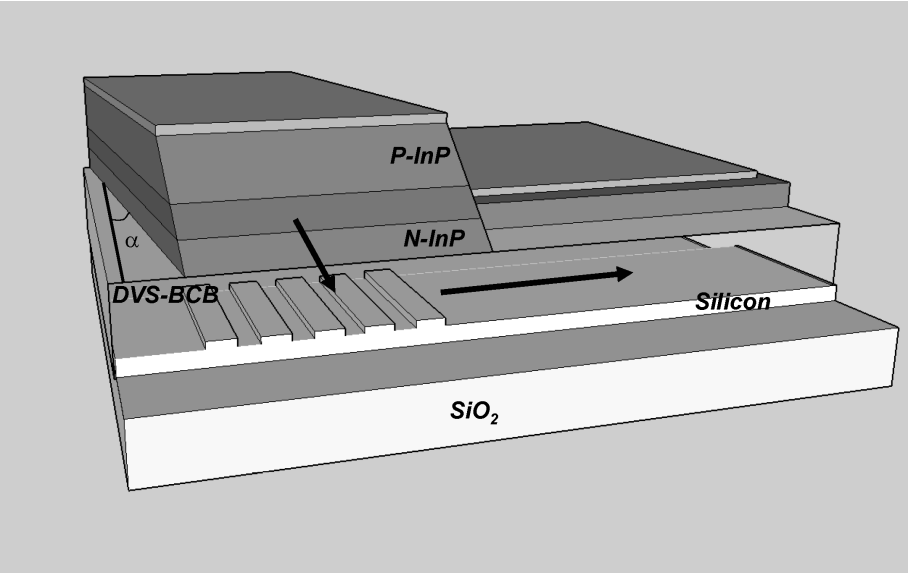


Figure 4.35: Layout of the 45 degree facet coupling structure

4.3.8 Evanescent coupling

An approach based on evanescent coupling from a laser cavity to an SOI waveguide is investigated in the framework of the PhD thesis of J. Van Campenhout. When the laser cavity has a sufficiently high quality factor, lasing can still be obtained in the cavity when loading the cavity by evanescently coupling light to an underlying SOI waveguide. Two laser cavity designs (a DBR microlaser and a microdisk laser) are shown in figure 4.36. Although these are interesting coupling schemes for laser diodes, the extension to using these structures as a coupling scheme for optical amplifiers and modulators is not trivial as there is a large wavelength selectivity of the coupling mechanism due to the presence of the cavity. When used as a photodetector, the quality factor of the cavity is reduced due to the absorption in the cavity and a less pronounced wavelength selectivity can be expected.

4.3.9 Hybrid silicon-InP/InGaAsP modes

In [149, 150], a continuous wave optically pumped hybrid AlGaInAs-silicon evanescent laser was reported, while in [151] electrical-injection-based lasing was demonstrated. In this work, a III-V active layer struc-

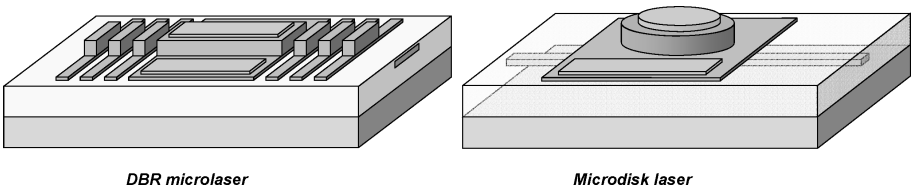


Figure 4.36: Microlaser configurations

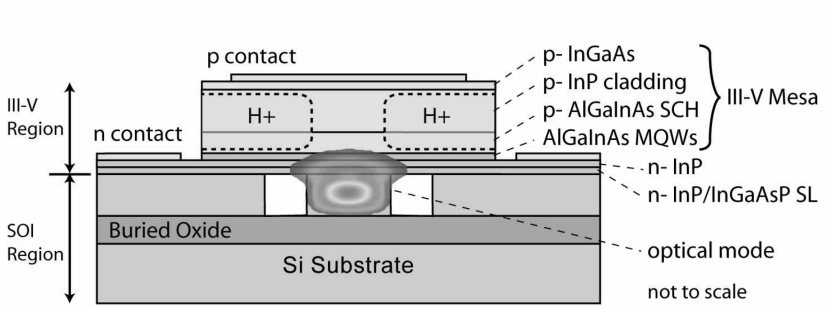


Figure 4.37: Device structure for achieving a hybrid silicon-InP/AlGaInAs laser (from [149])

ture was transferred by molecular bonding to a large core silicon rib waveguide structure as shown in figure 4.37. As the tail of the SOI waveguide mode overlaps with the quantum wells in III-V layer stack, this optical mode experiences gain.

Although this is an elegant method to obtain laser diodes integrated on and coupled to an SOI rib waveguide circuit, the extension of the concept to photonic wire technology is not straightforward. This is shown in figure 4.38, where the confinement factor Γ of the fundamental waveguide mode in the silicon core layer (which will in the end determine the coupling efficiency to a standard silicon waveguide) is plotted as a function of the height of the silicon waveguide layer. A 1μm thick InP/InGaAsP active layer consisting of 5 InGaAsP quantum wells (10nm wide,n=3.55) surrounded by 10nm wide barrier layers (n=3.39), sandwiched between InP cladding layers (n=3.17) is assumed and the silicon waveguide is defined by etching completely through the silicon waveguide layer (a 3μm wide silicon waveguide is assumed). The quantum well active region is located 100nm from the bottom of the InP/InGaAsP layer stack.

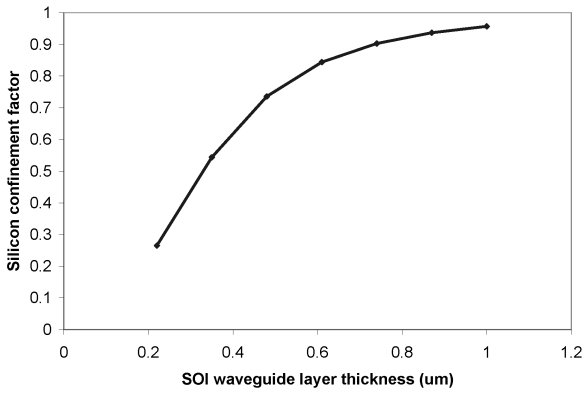


Figure 4.38: Influence of the SOI waveguide thickness on the confinement factor in the silicon waveguide

From this simulation is it clear that the confinement factor in the silicon waveguide layer decreases with decreasing SOI waveguide height. This is due to the fact that the strongly asymmetric oxide/silicon/InP waveguide stack is approaching cut-off. A silicon confinement factor of 26.5 percent is obtained for a 220nm thick SOI waveguide layer. This device structure would imply a significant decrease in external efficiency when the transition is made from InP/InGaAsP loaded waveguide to a standard SOI waveguide outside the laser cavity, or a significant increase in laser threshold current when the transition is made inside the laser cavity.

There are various ways to deal with this problem. In a first approach, the thickness of the InP/InGaAsP layer stack can be reduced as shown in figure 4.39, where the influence of the thickness of the top InP cladding layer is shown. Only minor improvement in confinement factor can be obtained. Moreover, thinning the InP/InGaAsP membrane further makes electrical injection difficult, as discussed in section 4.3.4.

In a second approach, a waveguide can be defined in the InP/InGaAsP layer stack, such that the width of the InP/InGaAsP waveguide can be exploited as an additional parameter to increase the confinement in the silicon waveguide layer. Additionally, this opens the way to electrical pumping of the active layer stack by etching through the active layer to reach the bottom InP cladding layer. The influence of the InP/InGaAsP waveguide width on the confinement factor in the SOI waveguide is shown in figure 4.40.

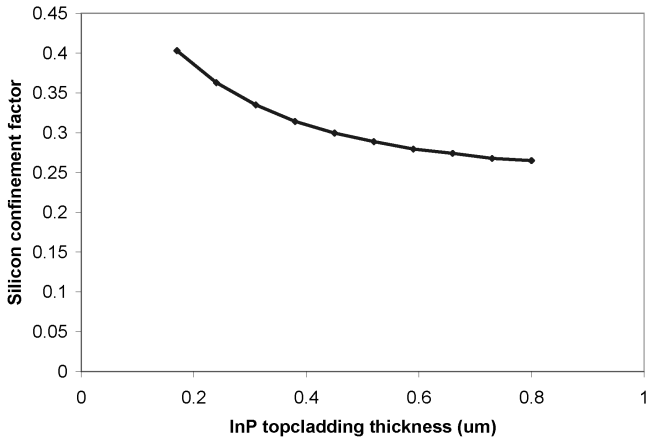


Figure 4.39: Influence of the InP/InGaAsP layer thickness on the confinement factor in the silicon waveguide layer

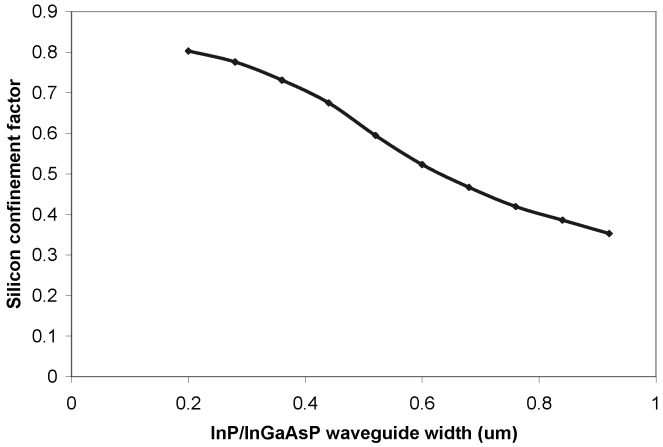


Figure 4.40: Influence of the InP/InGaAsP waveguide width on the confinement factor in the silicon waveguide layer

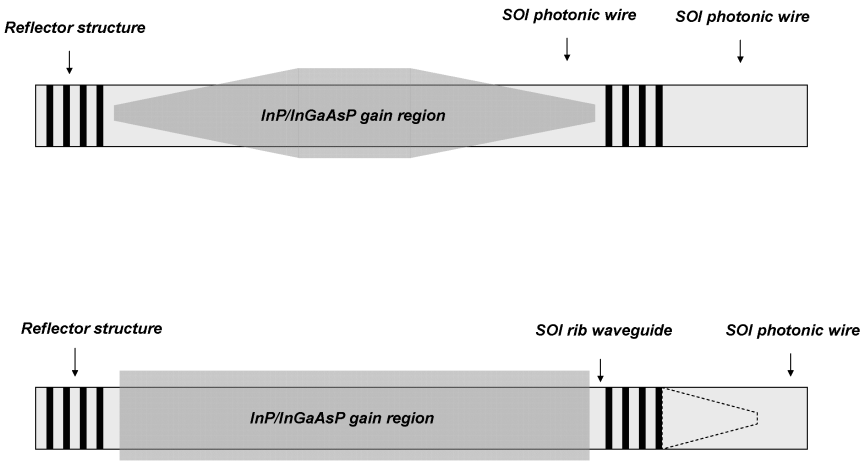


Figure 4.41: Different approaches to circumvent the problem of low optical confinement in a 220nm SOI waveguide layer

This width can vary throughout the laser structure to obtain a high confinement factor in the silicon layer when coupling to a standard SOI waveguide and a low confinement factor in the silicon layer (and hence a high confinement factor in the quantum well active region) where gain is needed. Making the transition adiabatic avoids additional losses. Relatively narrow taper tips are required for high coupling efficiency however, which are difficult to obtain.

In a third approach, the thickness of the silicon waveguide layer can be locally increased to achieve high confinement in the silicon waveguide layer and an adiabatic transformation to the photonic wire mode can be incorporated. Both ”adiabatic” approaches are schematically drawn in figure 4.41. The taper regions can be placed both inside the laser cavity (as is shown in the tapered InP waveguide approach) or outside the laser cavity (as is shown in the case of the local increase of SOI waveguide thickness). Although DBR type laser diodes are presented, the fabrication of a DFB type laser diode with the grating structure defined in the silicon rib waveguide layer, is equally attractive for the latter approach, as will be shown later in this section.

Note that the coupling scheme based on the tapering of the InP waveguide width is essentially identical to the one described in section 4.3.5.

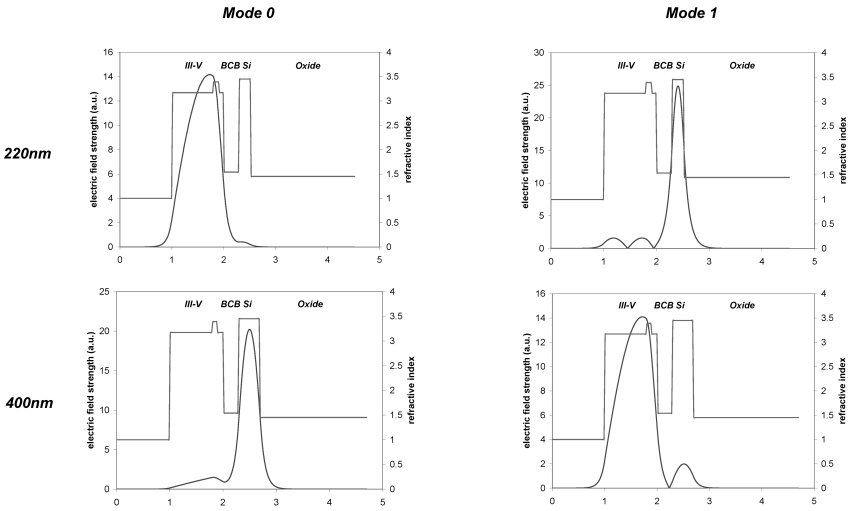


Figure 4.42: Hybrid waveguide modes in the case of a low index intermediate layer

So far, the discussion was restricted to a molecular bonding approach, in which a low index layer of negligible thickness (5nm is stated in [149]) is present between the silicon waveguide layer and the III-V layer stack. Therefore, we will discuss the influence of a low index bonding layer in between the silicon waveguide layer and the III-V layer stack, as is the case for adhesive bonding.

The presence of a low index intermediate layer has important implications on the properties of the optical modes. A double waveguide structure originates in which thickening the low index intermediate layer further decouples both waveguide modes. Increasing the intermediate low index layer thickness can both decrease or increase the confinement factor of the fundamental waveguide mode in the silicon waveguide, depending on the thickness of the silicon waveguide layer. To illustrate this, a cross-section of these waveguide modes is plotted in figure 4.42, for the case of a 220nm silicon waveguide layer thickness and a 400nm silicon waveguide layer thickness respectively. Both type of modes (silicon confined or III-V confined) can be used to achieve lasing in the structure.

The modes with high confinement in the InP/InGaAsP layers (mode 1 for the 400nm SOI waveguide layer thickness and mode 0 for the 220nm SOI waveguide layer thickness) were considered in the previous

sections to achieve lasing. Coupling between these waveguide modes and SOI waveguide was discussed. Note that, as the mode is nearly completely confined in the InP/InGaAsP layer stack, the presence of the silicon waveguide layer underneath is of little importance.

When the modes with high confinement in the silicon waveguide layer are considered for lasing, the influence of the intermediate low index layer thickness on the confinement factor in the quantum well active region has to be considered, together with the losses experienced by the optical mode. This will determine the material gain g_{th} that is needed to achieve lasing for these optical modes as

$$g_{th} = \frac{\alpha_i + \alpha_m + \alpha_b}{\Gamma} \tag{4.6}$$

in which α_i is the loss experienced by the optical mode due to doping and metallization of the InP/InGaAsP layer structure for electrical injection. α_m is the distributed loss due to the (usefull) extraction of photons from the cavity and α_b is the loss due to scattering at rough waveguide side walls.

The quality factor Q of a cavity is defined as the ratio of the resonance wavelength and the full width at half maximum of a transmission peak of the cavity and is (for a Fabry-Perot cavity) given by

$$Q = \frac{\lambda}{\Delta\lambda_{3dB}} = \frac{2\pi n L \exp(-\frac{(\alpha_m+\alpha_i+\alpha_b)L}{2})}{\lambda(1-\exp(-(\alpha_m+\alpha_i+\alpha_b)L))} \tag{4.7}$$

with $\frac{\lambda}{n}$ the material wavelength and L the length of the cavity. From equation 4.7 and 4.6 we can calculate the required modal gain Γg_{th} to achieve lasing as a function of the cavity quality factor. This is graphically shown in figure 4.43.

In figure 4.44, the influence of the thickness of a low index DVS-BCB bonding layer on the confinement factor in the multiple quantum well region and in the SOI waveguide core is plotted. A 1μm thick layer stack consisting of 5 InGaAsP quantum wells (10nm wide,n=3.55) surrounded by 10nm wide barrier layers (n=3.39) and InP cladding layers was assumed and three sets of curves were plotted, for 220nm, 400nm and 700nm SOI waveguide thickness respectively. As in the 400nm and 700nm layer thickness case, the mode is evanescent in the InP/InGaAsP layer stack (see figure 4.42), the optimal confinement factor is achieved when placing the multi quantum well structure as close to the SOI waveguide as possible. A minimal 100nm InP cladding layer was inserted between the bonding layer and the multi quantum well stack, to allow

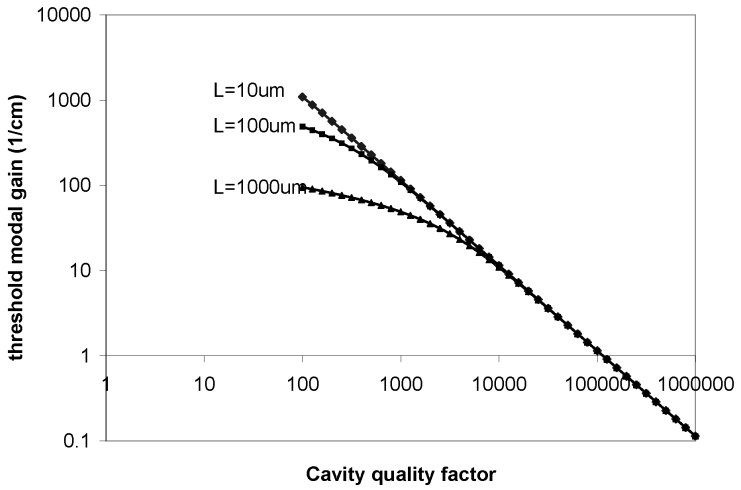


Figure 4.43: Required modal gain to achieve lasing as a function of cavity quality factor

electrical injection. In the case of the 220nm layer stack, the confinement factor in the quantum well layer is a strong function of the position of this quantum well stack, due to the oscillating field behavior in the InP/InGaAsP layer stack. The thickness of the n-type cladding layer was therefore optimized to obtain maximum confinement in the quantum well region while maintaining a total InP/InGaAsP layer thickness of 1μm.

From this simulation, several conclusions can be drawn. In order to obtain an acceptable confinement factor in the SOI waveguide of 80 percent, a minimal bonding layer thickness of 150nm is needed in the 220nm SOI and 400nm SOI case. The confinement factor in the quantum wells is about 1 percent in these cases. Assuming a maximum achievable threshold material gain of $10^4 cm^{-1}$, this leads to a maximum achievable modal gain of $100 cm^{-1}$ and therefore a minimal cavity Q-factor of 1000 for sub-mm length devices. In the 700nm SOI case, the confinement in the SOI waveguide is sufficient even without a bonding layer and a maximum quantum well confinement of 2 percent is achieved. As the minimum bonding layer thickness developed in this work was about 300nm, this results in a confinement factor in the order of 10^{-3} both for the 220nm and 400nm thick SOI case. Under the same assumption of a maximum material gain of $10^4 cm^{-1}$, the minimum required cavity quality factor is about 10^4. Note that these quality factors

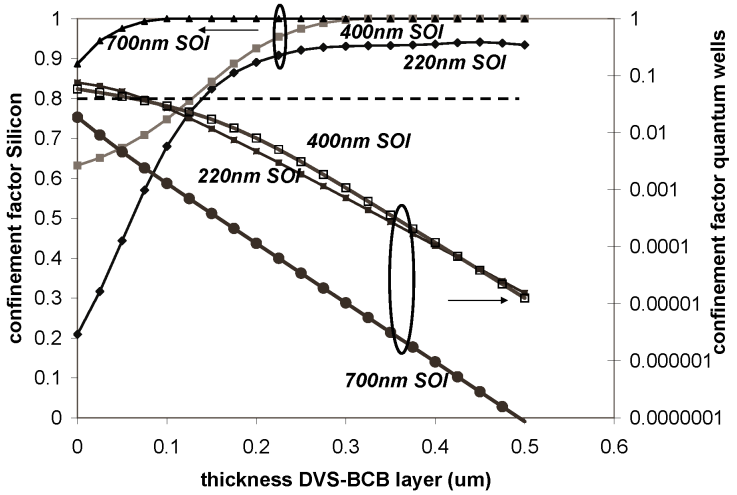


Figure 4.44: Influence of the low index DVS-BCB layer thickness on the confinement in the SOI waveguide and in the multiple quantum well region

include the influence of loss due to doping and metallization of the III-V stack.

In figure 4.45, the influence of a low index DVS-BCB intermediate bonding layer on the threshold gain contribution $g_{th,i} = \frac{\alpha_i}{\Gamma}$ due to the metallization and doping of the InP/InGaAsP layer stack, is plotted both for a 220nm thick SOI waveguide layer, a 400nm SOI waveguide layer and a 700nm SOI waveguide layer respectively. A 1μm thick InP/InGaAsP layer is assumed. The position of the quantum well region is again optimized to obtain the highest confinement in this quantum well region. A n-type doping of $10^{18}cm^{-3}$ and a p-type doping of $5 \times 10^{17}cm^{-3}$ is assumed. The metallization consists of a 20nm InGaAs contact layer, a 30nm titanium adhesion layer and a 150nm gold contact.

From this simulation, it is clear that the losses due to the metallization and doping of the InP/InGaAsP layer stack nearly fully consume the achievable material gain from the quantum wells in the case of a 220nm thick silicon waveguide layer. The major contribution factor to this loss is the presence of the titanium adhesion layer. In order to achieve lasing in these 220nm SOI layer structures, non-standard p-type injection schemes need to be developed, as varying the thickness of the InP/InGaAsP layer structure doesn't have a large influence on this threshold gain contribution. For example, removing the titanium

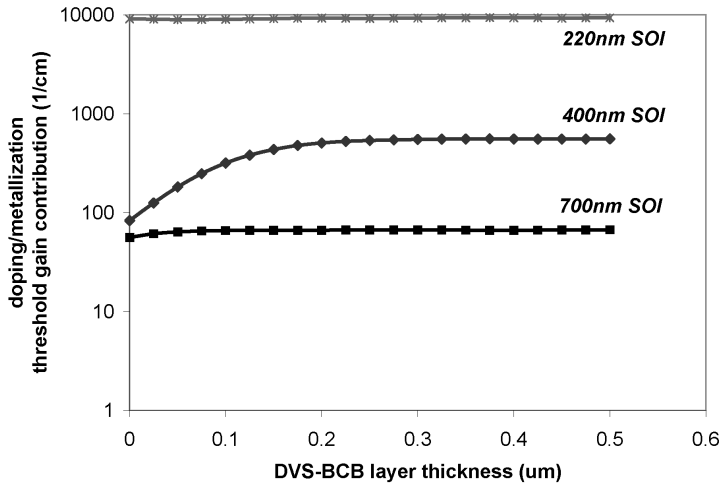


Figure 4.45: Influence of the DVS-BCB bonding layer thickness on $\frac{\alpha_i}{\Gamma}$

layer from the top contact reduces the threshold gain contribution by a factor of 7, although additional losses can be expected caused by the Au/InGaAs/InP material intermixing, due to the alloying of the contacts, which was neglected in figure 4.45. The use of shiny gold contacts [152], could alleviate this intermixing. In [153] the use of a DBR stack in between the gain region and the metallization was proposed to shield the optical mode from the metal contacts. A tunnel junction could be incorporated as well. The electronic diaphragm technique or the double side contact technique described in section 4.3.4 cannot be applied in this case as the lasing mode is a second order mode that would radiate into the InP/InGaAsP slab waveguide when no strong lateral index contrast is applied by etching through the waveguide core layer.

In order to achieve lasing in this SOI confined mode, sufficient threshold gain discrepancy between this SOI confined waveguide mode and the other waveguide modes needs to be achieved. Especially the mode concentrated in InP/InGaAsP layer stack needs to be considered as this mode shows higher quantum well confinement. This discrepancy can be partially achieved by the higher loss of the InP/InGaAsP mode (which is enhanced by not using separate confinement layers in the active layer stack), although an important contribution possibly has to be made by the difference in cavity modal reflection coefficients. Neglecting the losses due to scattering α_b, we can calculate the maximum

SOI thickness	Bonding layer thickness	L=10μm	L=100μm	L=1000μm
220nm	300nm	-0.05dB	-0.49dB	-4.9dB
400nm	300nm	-0.037dB	-0.37dB	-3.7dB
700nm	300nm	>0dB	>0dB	>0dB
220nm	150nm	-0.7dB	-7dB	-70dB
400nm	150nm	-0.68dB	-6.8dB	-68dB
700nm	150nm	-0.015dB	-0.15dB	-1.5dB
700nm	0nm	-0.8dB	-8dB	-80dB

Table 4.1: Minimum required SOI confined reflection coefficients for a maximum material gain of 10000/cm

SOI thickness	Bonding layer thickness	L=10μm	L=100μm	L=1000μm
220nm	300nm	-0.02dB	-0.2dB	-2dB
400nm	300nm	-0.017dB	-0.17dB	-1.7dB
700nm	300nm	>0dB	>0dB	>0dB
220nm	150nm	-0.3dB	-3dB	-30dB
400nm	150nm	-0.33dB	-3.3dB	-33dB
700nm	150nm	-0.007dB	-0.07dB	-0.7dB
700nm	0nm	-0.4dB	-4dB	-40dB

Table 4.2: Minimum required SOI confined reflection coefficients for a maximum material gain of 5000/cm

allowed reflection coefficient of the InP confined waveguide mode, in order to achieve lasing in the SOI confined mode as

$$R_{InP,\max} = R_{SOI}^{\frac{\Gamma_{InP}}{\Gamma_{SOI}}} \exp(-\Delta g_{th,i} L \Gamma_{InP}) \tag{4.8}$$

by equalizing the threshold material gain for the InP confined mode and the SOI confined mode.

In equation 4.8, R_{InP},Γ_{InP} and R_{SOI},Γ_{SOI} are the reflection coefficient and quantum well confinement factor for the InP and SOI confined mode respectively. L is the cavity length, while $\Delta g_{th,i} = g_{th,i,SOI} - g_{th,i,InP}$ is the difference in metallization/doping threshold gain contribution between both waveguide modes.

The minimum required R_{SOI} to achieve lasing is determined by the maximum achievable material gain g_{max} and is given by

$$R_{SOI,\min} = \exp(-(\Gamma g_{\max} - \alpha_i - \alpha_b)L) \tag{4.9}$$

In table 4.1 and table 4.2 the numerical results of equation 4.9 is tabulated for a maximum obtainable material gain of 10000/cm and 5000/cm respectively. A waveguide scattering loss $\alpha_b = 0.25cm^{-1}$ was assumed. The titanium layer was removed to reduce the losses experienced by the SOI confined waveguide mode.

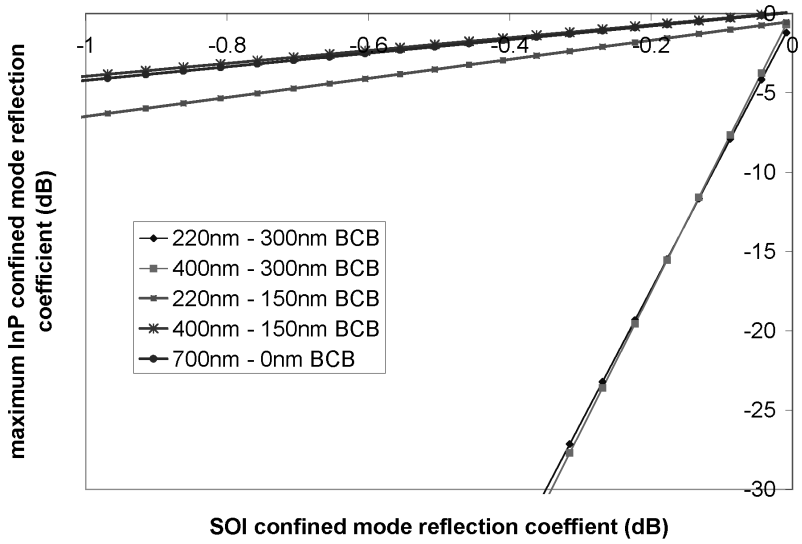


Figure 4.46: Maximum InP confined mode reflection coefficient for a 10μm long laser cavity

Equation 4.8 is plotted in figure 4.46, 4.47 and 4.48 for a laser cavity length of 10μm, 100μm and 1000μm respectively.

For a silicon layer thickness of 220nm and a bonding layer thickness of 300nm, the minimal reflection coefficient of the SOI confined waveguide mode must be very high for L=10μm and L=100μm, while for L=1000μm only a moderate reflection coefficient is needed. In this case the reflection of the InP confined mode has to be kept very low (below -30dB) in order to avoid lasing in this mode. This requirement is relaxed for thinner bonding layers (150nm), where for L=100μm, the required R_{SOI} is low and the maximum allowed R_{InP} is acceptable. This requirement is further relaxed when a 400nm thick silicon waveguide layer is used, in which case even a standard p-type contact would be viable.

From this discussion we can conclude that the use of InP/InGaAsP-silicon hybrid modes is a viable solution for achieving a current injected laser diode integrated on and coupled to an SOI waveguide, especially on thicker SOI layer stacks. In the case of a 220nm SOI layer stack, special electrical contacting schemes need to be designed, thinner bonding layers are required to achieve lasing, a high reflection coefficient for the SOI confined waveguide mode is needed and/or care has to be taken to

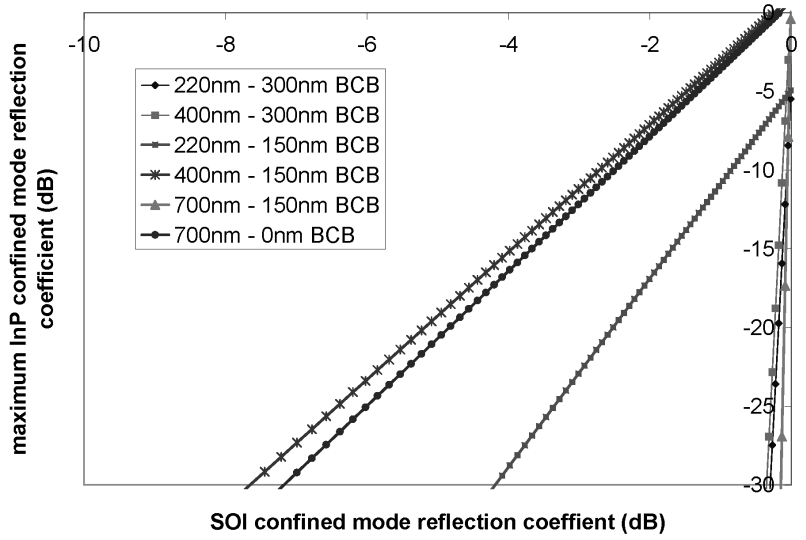


Figure 4.47: Maximum InP confined mode reflection coefficient for a 100μm long laser cavity

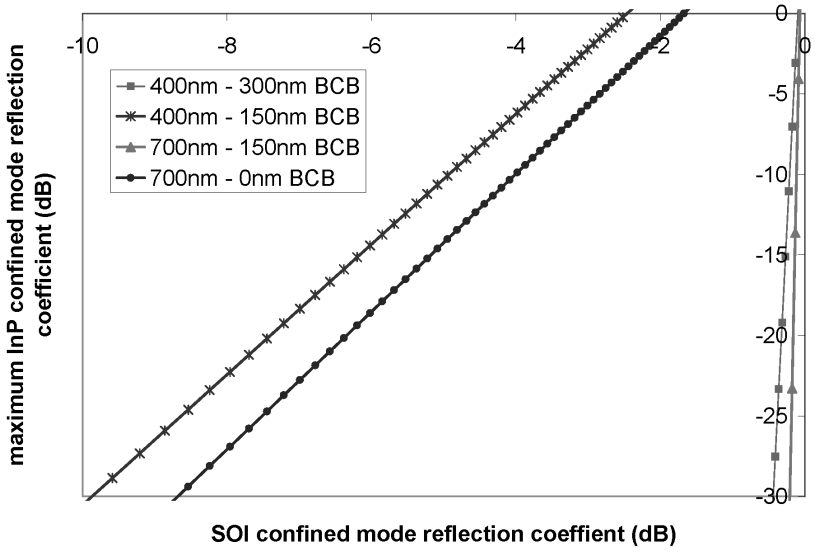


Figure 4.48: Maximum InP confined mode reflection coefficient for a 1000μm long laser cavity

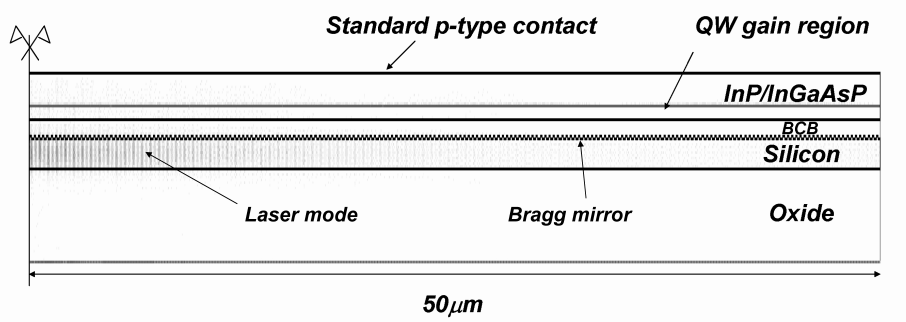


Figure 4.49: Field plot of a hybrid DFB laser diode

sufficiently reduce the reflection coefficient of the InP confined mode to avoid lasing in this mode. Especially the further reduction of the bonding layer to 150nm on a higher topography (400nm instead of 220nm) is outside the scope of this work.

A simulation example of this type of laser diode is shown in figure 4.49. The laser structure consists of a 400nm silicon waveguide core in which a first order Bragg reflector was etched (etch depth 40nm). A 0.5μm thick InP/InGaAsP active layer with standard doping levels and a standard p-type contact is bonded on top of the silicon waveguide structure using a 150nm bonding layer. The gain region consists of 5 quantum wells which supply a threshold material gain of about 3000/cm for a 100μm long device.

4.4 Comparison of optical coupling schemes

As is clear from the previous discussion, the coupling schemes presented for coupling to in-plane operating devices differed in various ways, each having their own advantages and disadvantages. An overview of the coupling methods is presented in table 4.3. From this overview, we selected the polymer-waveguide-based coupling scheme using ultra-thin DVS-BCB bonding, as a good compromise between optical performance (efficiency, bandwidth and device footprint) and ease of fabrication (fabrication tolerance, type of DVS-BCB bonding and number of processing steps) is obtained. This type of coupling mechanism will be explored further in the following chapters on bonded laser diodes and bonded waveguide-based photodetectors. Especially, the

Coupling scheme	efficiency	bandwidth	tolerance	footprint	DVS-BCB thickness	Number of steps
Directional	high	medium	medium	medium	ultra-thin	medium
Tapered coupler	high	high	high	medium	ultra-thin	medium
GADC	high	low	low	medium	ultra-thin	medium
Bridging modes	high	low	low	medium	thick	medium
Radiation modes	medium	medium	low	low	thick	medium
Polymer taper (thin)	high	high	high	medium	ultra-thin	high
polymer taper (thick)	medium	high	high	high	thick	high
45 degree facet	medium	medium	low	low	thick	high
evanescent	medium	low	low	low	ultra-thin	low

Table 4.3: Comparison of different optical coupling schemes

adiabatic nature of this approach is appealing, as always a trade off can be made between actual device length and fabrication tolerance.

4.5 Vertically operating devices

While in the previous section various optical coupling schemes were analyzed for coupling to in-plane operating devices, in this section the use of a diffractive grating structure will be studied for surface illumination of a bonded photodetector. Only recently, advances have been made in the fabrication of long-wavelength vertical cavity semiconductor lasers [136]. These will therefore not be discussed in detail, although a grating-based coupling scheme for VCSEL devices will be proposed in section 4.6.5.

4.5.1 Surface illumination of a photodetector using a diffractive grating

As a starting point for the design of a coupling scheme for efficient surface illumination of a bonded InP/InGaAsP photodetector, a grating coupler structure optimized for coupling light to a single-mode optical fiber was used [154]. This grating coupler is defined by etching a one-dimensional periodic structure in the 220nm thick silicon core layer with an etch depth of 50nm, a grating period of 610nm and a duty cycle of 50 percent. In order not to complicate the overall fabrication process, this grating structure was not modified for this specific purpose of illuminating a photodetector. The coupling scheme is schematically depicted in figure 4.50.

A 2μm thick InGaAs absorption layer was chosen as a compromise between efficiency and transit time limited bandwidth of the device. In order to obtain efficient detection, the influence of the thickness of the buried oxide layer and the DVS-BCB bonding layer was assessed as a

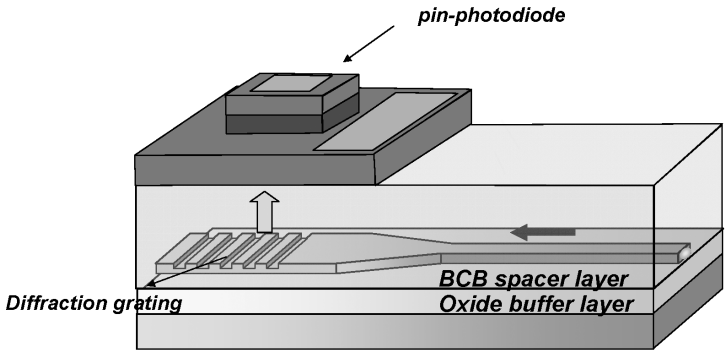


Figure 4.50: Coupling scheme for surface illumination of a bonded photodetector

cavity is formed caused by the reflection at the DVS-BCB/InP interface and the SiO_2/silicon substrate interface. The exact location of the SOI grating inside the cavity determines its directionality (being the ratio of the power coupled upwards to the total diffracted power) and its coupling strength (determining the length of the grating). Simulation results showing the influence of the DVS-BCB bonding layer thickness and SiO_2 buffer layer thickness on the fraction of absorbed power for a 50 μm long detector are shown in figure 4.51. Optimal device operation is achieved for a DVS-BCB bonding layer thickness of 3 μm and an SiO_2 buffer layer of 1.4 μm thick.

A field plot of the proposed structure is shown in figure 4.52, indicating the reflections at the DVS-BCB/InP interface and SiO_2/silicon interface.

The wavelength dependence of the absorbed and reflected power fraction back into the SOI waveguide is shown in figure 4.53. The dispersion of the refractive index of the materials was taken into account in the simulation. Around a wavelength of 1650nm a sharp peak in the reflected power can be observed, which is due to the second order reflection of the grating. By placing this reflection peak near the absorption edge of InGaAs, the complete C (1525nm-1565nm) and L (1570nm-1610nm) optical telecommunication band can be covered.

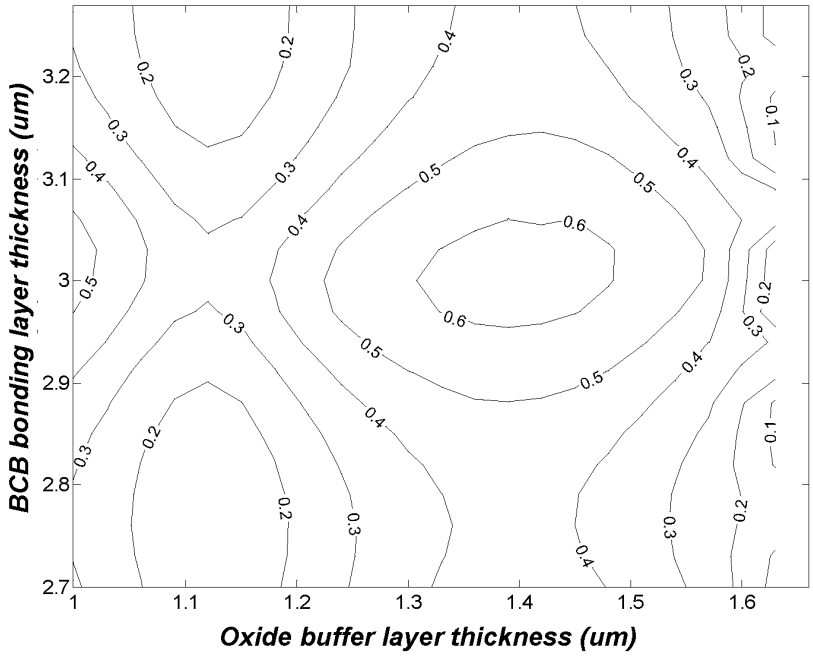


Figure 4.51: Optimization of the buried oxide layer thickness and the DVS-BCB bonding layer thickness (λ=1.55μm, TE polarization)

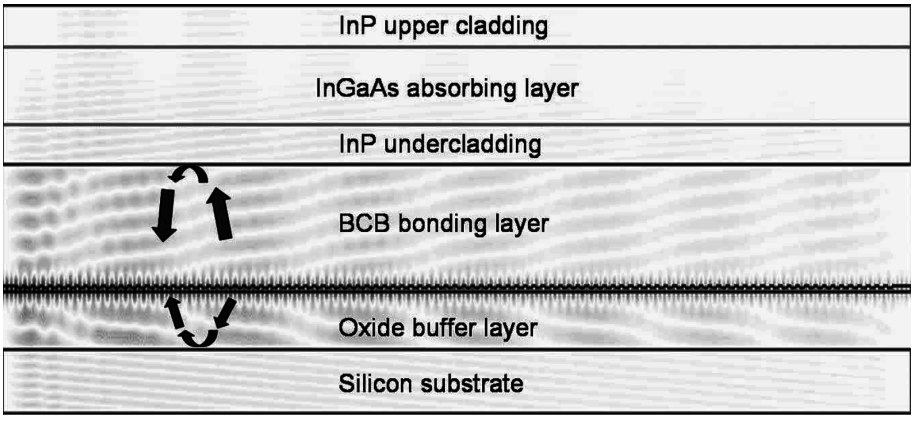


Figure 4.52: Simulation of an optimized photodetector/grating structure (λ=1.7μm, TE polarization)

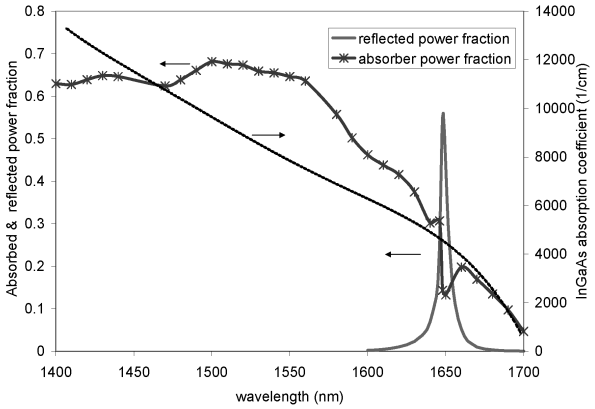


Figure 4.53: Simulated spectral response of an optimized InGaAs photodetector - the power reflection back into the SOI waveguide is also plotted

4.5.2 Improvement of the coupling efficiency

The coupling efficiency of the scheme based on a grating coupler can be increased by improving the directionality of the grating. This can be done in two ways: a first method is to include a mirror underneath the grating structure, which redirects the downwards diffracted light. This can be both a DBR type mirror formed by Si/SiO_2 layer pairs or a gold bottom mirror (obtained by an additional wafer bonding step as will be explained in section 8.6). In a second approach, an additional silicon layer is added to the SOI layer structure prior to grating etching, which improves the directionality of the grating. The different approaches are shown in figure 4.54.

Mirror-clad grating coupler design

As there are no commercial SOI wafers available containing the DBR type bottom mirror as shown in figure 4.54, we will focus on the use of a gold bottom mirror for efficiency enhancement. This type of structure can be obtained by a double bonding step (one bonding step to obtain the gold bottom mirror and one bonding step to integrate the InP/InGaAsP layer stack), as will be explained in section 8.6. Again, the spacing between the grating and the InP/InGaAsP layer stack and the spacing between the grating and the gold mirror needs to be optimized. In this case, the directionality is no longer influenced by these parameters (due to the presence of the gold mirror), but the coupling

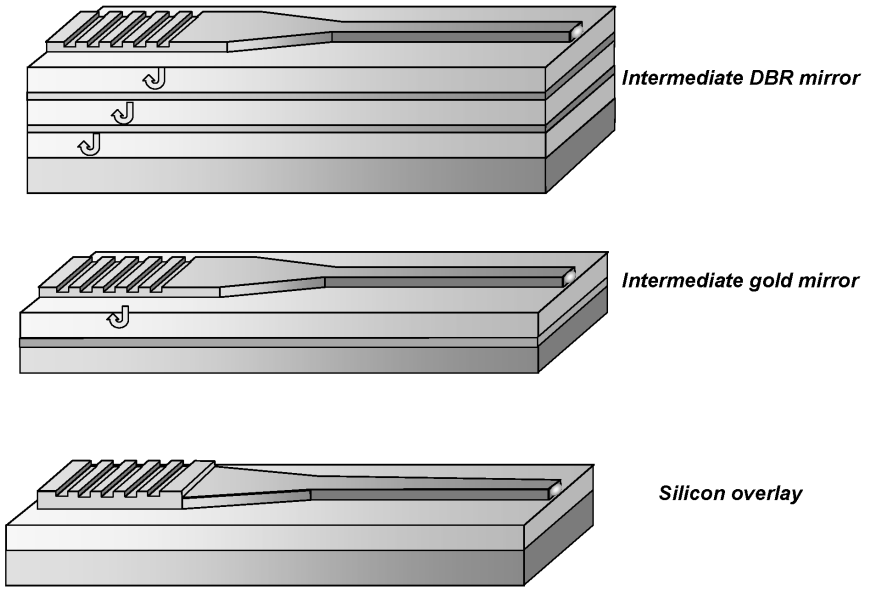


Figure 4.54: Configurations to increase the directionality of grating coupler structures

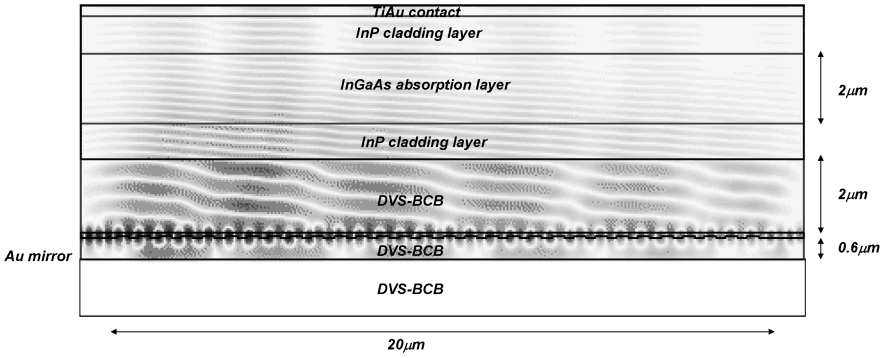


Figure 4.55: Optimized structure for efficient coupling to a photodetector using a gold bottom mirror - note that the grating teeth are directed downwards, due to the additional bonding step to create the gold bottom mirror

strength of the grating still is however. Therefore, in order to achieve a compact device (large coupling strength) with little second order reflection back into the SOI waveguide, these parameters need to be optimized. A field plot at a wavelength of 1.55μm of an optimized structure is shown in figure 4.55. A photodetector length of 20μm is needed to detect most of the light diffracted by the grating. The grating structure is identical to the one in the previous section and the optimized spacings are indicated in figure 4.55.

Overlay-based grating coupler design

Although the gold bottom mirror design allows to define a grating coupler with a directionality close to 1, a double bonding step is needed for fabrication of the device. Therefore, an alternative coupling scheme was designed that only requires one bonding step and for which there is only a slight penalty in grating coupler directionality. This coupling scheme is based on the additional deposition of a silicon layer prior to grating etching and based on changes in the grating etch depth and period. As will be shown in section 4.6.5, this leads to an important improvement in grating directionality compared to the standard grating coupler scheme.

A field plot of an optimized coupling structure for a wavelength of 1.55μm is shown in figure 4.56. An addition silicon layer of 150nm thickness is deposited. The grating etch depth is 220nm, while the grating period is 610nm. A grating duty cycle of 50 percent is assumed. 87

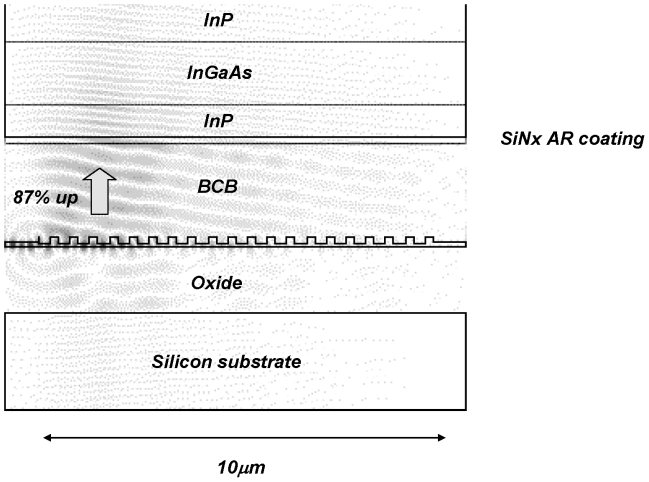


Figure 4.56: Optimized structure for efficient coupling to a photodetector using a silicon overlay

percent of the optical power is diffracted upwards over a 10μm grating length. An anti-reflection coating is applied on the InP/InGaAsP epitaxial layer stack to avoid the formation of a cavity, which could introduce a reduction of the coupling strength and grating directionality. As the high directionality of the optimized grating structure is intrinsic to the grating (and not related to a constructive interference effect caused by the reflection at the oxide/silicon interface) and as an anti-reflection coating on the detector layer stack is applied, the thickness of the DVS-BCB layer and oxide buffer layer is not critical.

4.6 Coupling to optical fiber

4.6.1 Rationale

The coupling schemes discussed in the previous sections were developed for coupling light exiting a bonded active device to a silicon-on-insulator waveguide circuit and vice versa. Another important subject of research in photonics is how to couple light from an optical fiber into a photonic integrated circuit with high efficiency and large optical bandwidth. In this section we will show that some of the coupling

schemes developed in the previous sections can also be used for this purpose.

4.6.2 Literature review

In literature, several methods for coupling an optical fiber to a high index contrast waveguide system are described. In these high index contrast systems, butt-coupling of the optical fiber to the integrated waveguides leads to large coupling losses, due to the severe mismatch in fiber mode size and integrated waveguide mode size. The most important coupling mechanisms to circumvent this problem are shown in figure 4.57.

The use of a grating coupler mechanism was proposed in literature to achieve high coupling efficiency. Both one-dimensional [154] and two-dimensional [139] grating couplers were presented, with variations in the particular designs (the use of slanted gratings [155] or curved vertically etched gratings [156]). Two-dimensional grating couplers can be used in a polarization diversity approach. Besides grating couplers based on coupling to radiation modes, also grating-assisted directional coupler schemes were proposed [157], although only limited optical bandwidth can be obtained in this way.

Another important class of coupling structures are the adiabatic taper structures. Both three-dimensional adiabatic taper structures [158] and inverted taper structures based on a low refractive index waveguide overlay [145, 159] were proposed. While three-dimensional adiabatic taper structures are difficult to process and control, the use of standard inverted taper couplers requires e-beam definition of the sub 100nm taper tip, which is not achievable using standard CMOS 248nm deep UV lithography.

A new type of coupling structure presented in literature is based on a graded index (GRIN) coupler for efficient coupling into an SOI waveguide [160].

4.6.3 Comparison and selection of coupling schemes

A comparison of the coupling schemes based on the information found in literature is outlined in table 4.4, in which the coupling efficiency, device footprint, polarization dependent loss (PDL), size of the smallest features, ease of fabrication and optical bandwidth are compared.

From this comparison we can conclude that the inverted taper coupler approach results in large bandwidth devices with high coupling

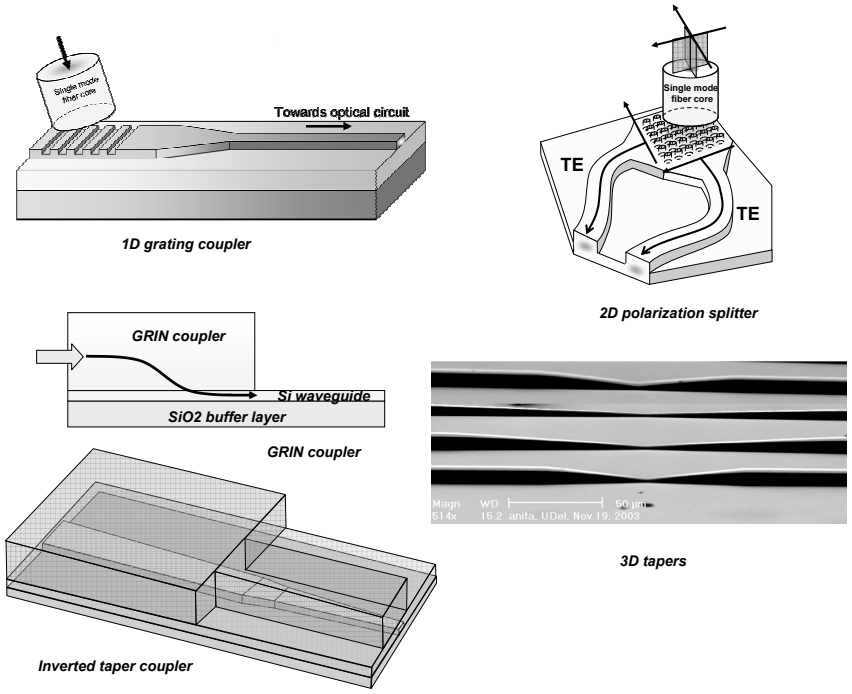


Figure 4.57: Overview of different fiber coupling structures

Type of coupling	loss	length	PDL	features	fabrication	bandwidth
butt-coupling	20dB	0μm	<0.5dB	>1μm	easy	>100nm
grating (1D) [161]	5-7dB	15μm	>20dB	300nm	medium	60nm
grating (2D) [139]	7dB	15μm	<1dB	300nm	medium	60nm
inverse taper [145, 159]	0.5dB	300μm	<1dB	100nm	medium	>100nm
GRIN coupler [160]	n.k.	15μm	0.5dB	>1μm	hard	n.k.
3D taper [158]	1.5dB	600μm	<1dB	>1μm	hard	>100nm

Table 4.4: Comparison of different fiber coupling schemes presented in literature

efficiency at the expense of a larger device length and critical feature sizes, while the grating coupler approach shows very compact devices with medium optical bandwidth and medium coupling efficiency. As these are also the type of coupling schemes that were analyzed in the previous sections on the coupling to bonded active devices, it is interesting to investigate wether the same type of devices (i.e. fabricated using the same processing steps) can be used for coupling to an optical fiber. We will show that, based on the analysis of the coupling schemes for bonded devices, significant improvements were made to existing fiber coupling structures described in literature.

4.6.4 Inverted taper couplers

While the inverted taper coupler structures presented in literature [145, 162] obtained high coupling efficiency towards a lensed or high numerical aperture fiber, critical feature sizes of 100nm or lower needed to be defined (i.e. the taper tip width). These features cannot be defined using standard CMOS 248nm deep UV lithography, which was one of the main reasons for the interest in the SOI material system, namely the use of standard CMOS technology for mass fabrication. This narrow taper tip feature is required due to the fact that in the proposed design, the polymer waveguide mode and the SOI waveguide mode are strongly coupled (as is the case in the adiabatic taper coupling scheme for standard DVS-BCB bonding of section 4.3.6). Therefore, we proposed to introduce a low refractive index DVS-BCB spacer layer between the SOI waveguide layer and the polymer waveguide layer, to partially decouple both waveguide modes as shown in figure 4.58.

The influence of the introduction of the DVS-BCB spacer layer on the coupling efficiency at the taper tip interface is plotted in figure 4.59 for a polyimide (n=1.69) waveguide core height of 3μm (also a waveguide width of 3μm was assumed for efficient coupling to a lensed fiber). It is clear that the taper tip width required for efficient coupling shifts from 100nm width into the deep UV definable region, by introducing this spacer layer.

While this introduction of a spacer layer has a positive influence on the feature sizes to be defined, it has an averse influence on the device length. This is plotted in figure 4.60, in which the minimum adiabatic taper angle is plotted versus DVS-BCB spacer layer thickness. An obvious way of increasing this adiabatic taper angle is to reduce the polymer waveguide core height, as this again increases the coupling

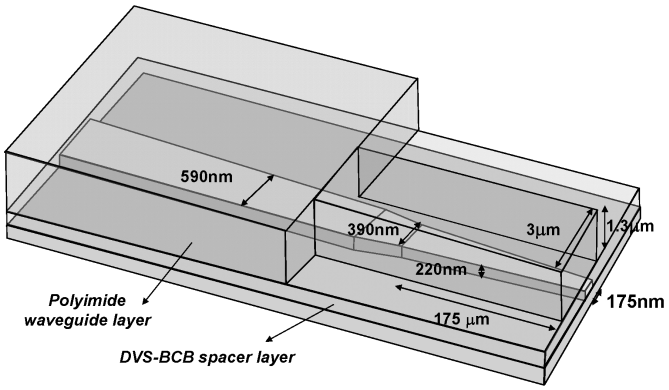


Figure 4.58: Inverted taper structure with a DVS-BCB spacer layer

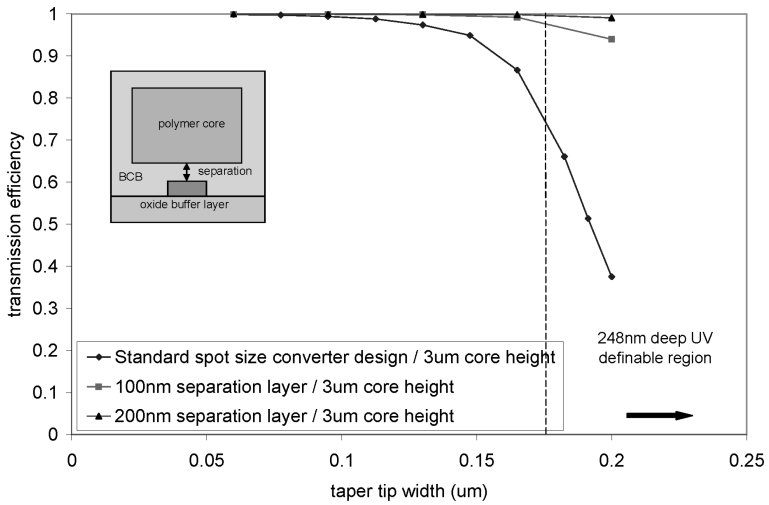


Figure 4.59: Design of an inverted taper structure: influence of taper tip width

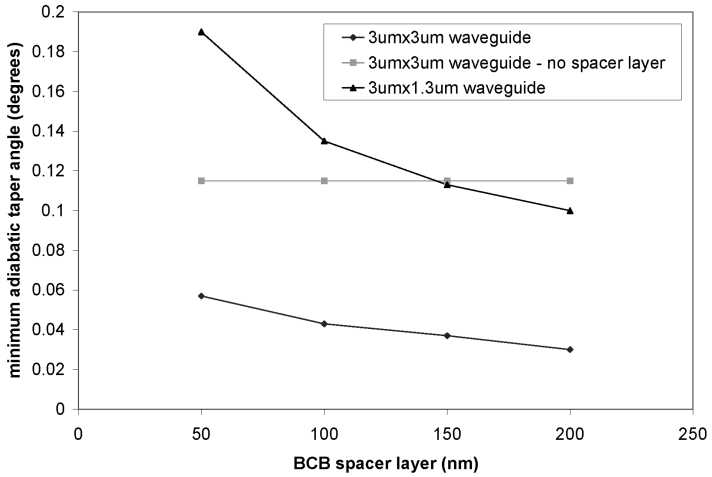


Figure 4.60: Design of an inverted taper structure: minimum adiabatic taper angle

between the waveguide modes, this at the expense of a reduced coupling efficiency to lensed fiber, due to the mode mismatch between the polymer waveguide mode and the lensed fiber spot size, as is shown in figure 4.61 and 4.60. While this decrease in polymer waveguide height has an important influence on the device length, the required taper tip definition stays inside the deep UV definable region, to come to an optimized fiber-to-waveguide coupling scheme, definable using 248nm deep UV lithography, as shown in figure 4.58.

4.6.5 Grating-based fiber couplers

The use of a grating coupler has the advantage of resulting in a very compact coupling structure and not requiring a polished facet for coupling, paving the way to wafer-scale testing of integrated optical components. The coupling efficiencies of fabricated devices presented in literature is limited however (typically 20 to 30 percent fiber coupling efficiency is experimentally obtained), which can be sufficient for testing but is not sufficient in practical applications. Therefore, we will present two ways (identical to the mechanisms described in the section on coupling to a surface-illuminated photodetector) to improve this coupling efficiency. One mechanism is based on the incorporation of a gold bot-

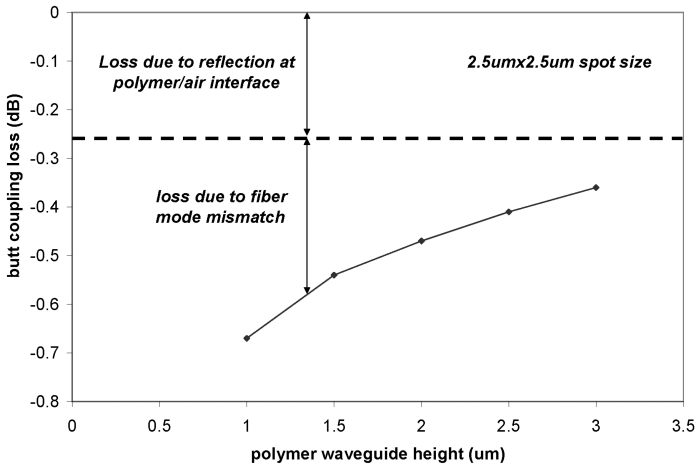


Figure 4.61: Design of an inverted taper structure: fiber insertion loss

tom mirror to redirect the downwards diffracted light, while the second approach is based on a silicon overlay.

Mirror-clad fiber-to-waveguide grating coupler

While the introduction of a gold bottom mirror provides perfect directionality for the grating, the position of the mirror also changes the coupling strength of the grating coupler. As there is an optimal coupling strength for the grating coupler to couple light into a single-mode fiber [163], the spacing between the gold mirror and the grating coupler needs to be optimized. The result of this optimization is shown in figure 4.62, from which it is clear that a coupling efficiency to optical fiber of 72 percent can be obtained when a DVS-BCB buffer layer thickness between the grating and gold mirror of 850nm is used. A grating period of 610nm, an etch depth of 50nm and a duty cycle of 50 percent was used in the simulations. A 20 period grating coupler was assumed. The fiber is tilted 10 degrees off vertical to avoid a strong second order reflection. While simulations are performed for one-dimensional grating structures, the same concepts can be extended to a two-dimensional grating structure for polarization diversity.

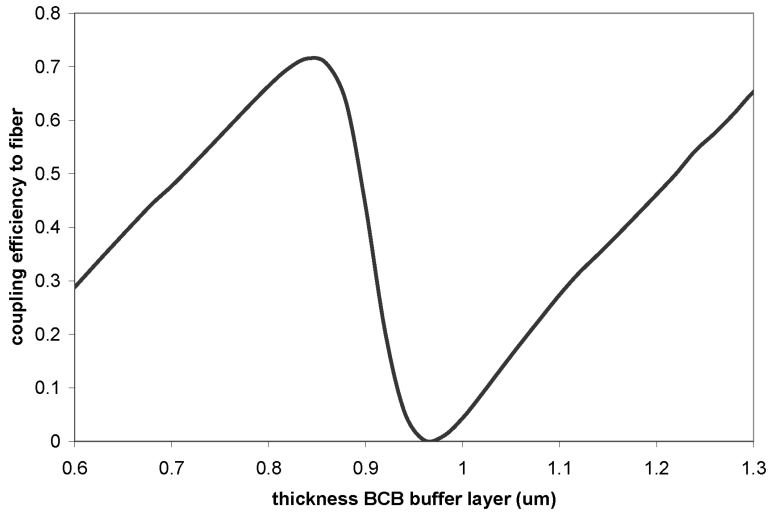


Figure 4.62: Design of DVS-BCB buffer layer thickness for a gold bottom mirror approach, determining the optimal spacing between the grating coupler and the gold bottom mirror

Fiber-to-waveguide grating couplers with silicon overlay

One can argue wether the introduction of a gold mirror underneath the grating coupler is a truly CMOS compatible fabrication step. This gold layer can however be replaced by CMOS compatible metals, like copper. In either case, the introduction of a metallic bottom mirror complicates the fabrication process, as a bonding step is required to fabricate the bottom mirror (see section 8.6). Here we propose a different coupling scheme based on the deposition of a silicon layer prior to etching of the grating coupler. The proposed structure is depicted in figure 4.63. The fiber is slightly tilted off vertical to avoid a strong second order reflection.

The choice of the additional silicon layer thickness, the grating etch depth and grating period is driven by the simulation presented in figure 4.64, in which the directionality (defined as the fraction of the power that is coupled upwards over a 20 period grating) is plotted versus the etch depth for several combinations of the grating period and silicon overlay thickness. A uniform grating structure with a grating duty cycle of 50 percent was assumed. From this simulation it is clear that the optimum performance of such a uniform grating structure is obtained for a grating period of 610nm, with 150nm of silicon added and a grating etch depth of 220nm. Moreover, the directionality is much higher

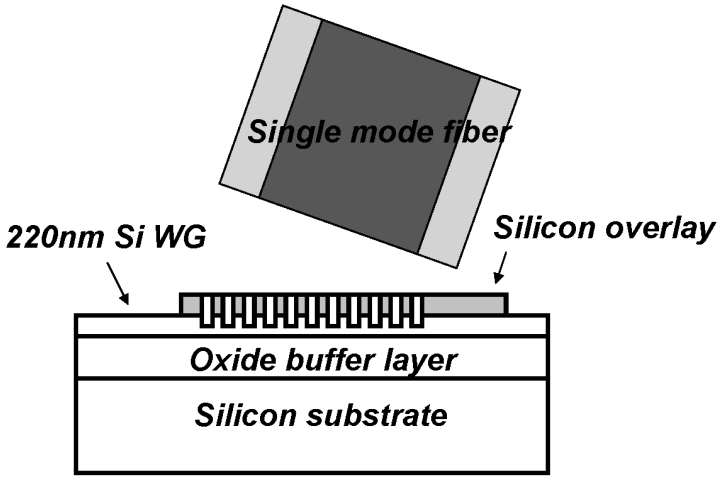


Figure 4.63: Layout of the structure proposed for efficient coupling to fiber - a silicon overlay is deposited prior to grating etching

than for a standard grating, for which typically 50 percent directionality is achieved [154].

The extra step of locally defining an additional silicon layer can introduce a misalignment of the grating mask with respect to the defined silicon layer mesa. This introduces a change in the width of the first and the last grating tooth. As nearly all light has diffracted out of the grating when reaching the last grating tooth, we will focus on the influence of the grating coupler efficiency on the first grating tooth width. This influence is plotted in figure 4.65 in which the coupling efficiency to a single-mode optical fiber is plotted versus the width of the first grating tooth. The optical fiber is tilted 10 degrees off vertical.

For a half period grating tooth width, a coupling efficiency to optical fiber of 67 percent is obtained while a plus/minus 150nm alignment tolerance is obtained, which is easily achievable using standard CMOS technology (typical alignment accuracy 50nm). As proposed in [163], we can also modify the design of the grating structure to obtain a non-uniform grating coupler with improved coupling efficiency to optical fiber. This design optimization was done using a genetic algorithm technique, in which a lower boundary grating tooth and grating slit width of 200nm was assumed, to maintain the option of fabrication

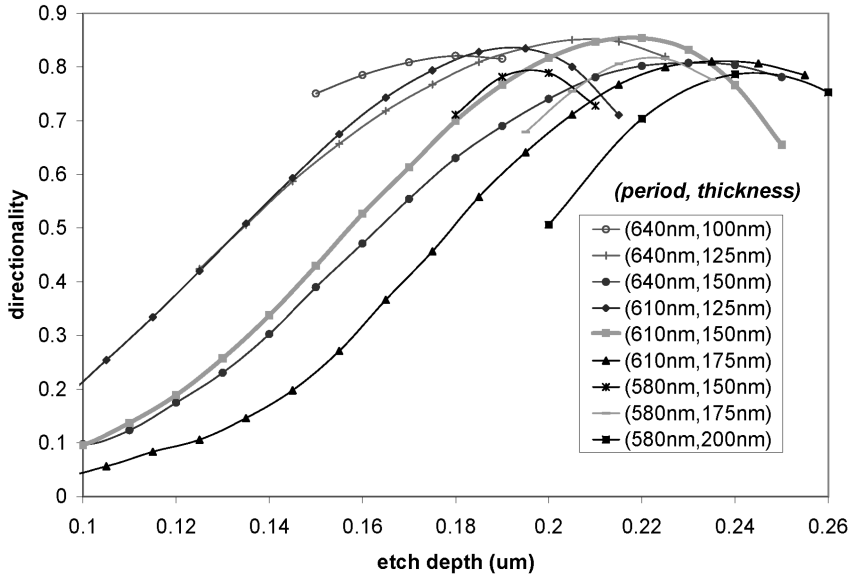


Figure 4.64: Influence of the grating parameters on the grating directionality (a grating duty cyle of 50 percent was assumed)

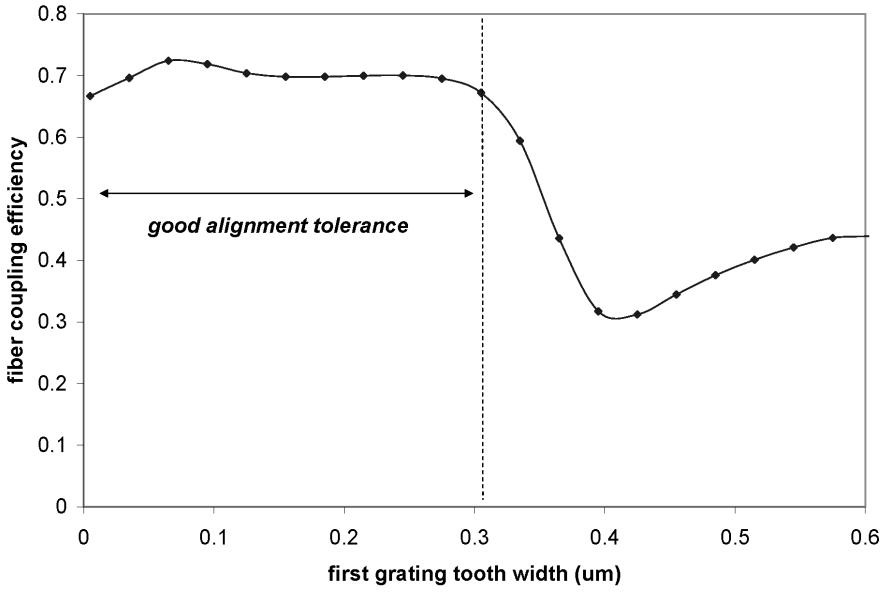


Figure 4.65: The coupling efficiency to a single-mode optical fiber versus the width of the first grating tooth (λ=1.55μm, TE polarization)

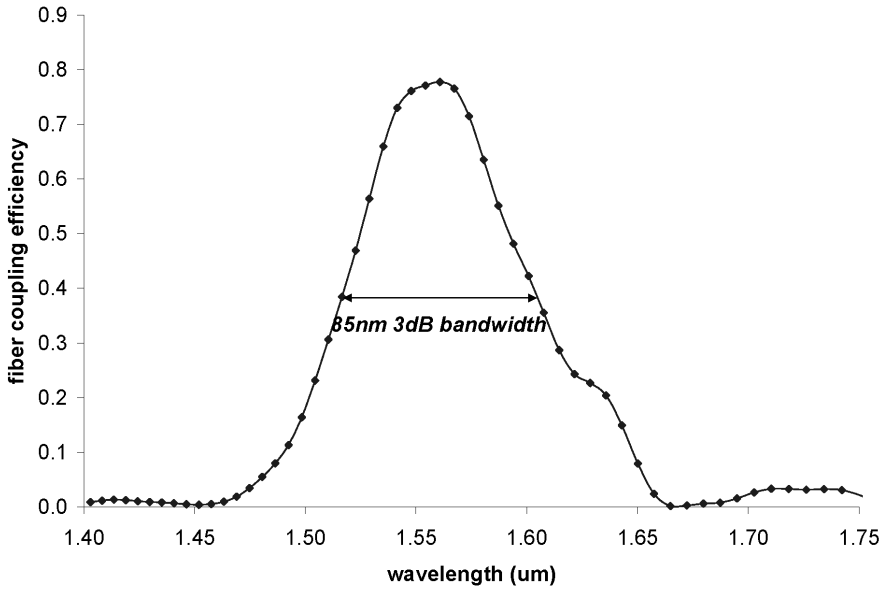


Figure 4.66: FDTD analysis of the optimized grating coupler structure

using 248nm deep UV lithography. Doing this, the coupling efficiency increased from 67 percent for the case of a uniform grating to 78 percent for an optimized grating shape.

An FDTD analysis was performed to simulate the optical bandwidth of the grating coupler structure. The wavelength dependence of the coupling efficiency is plotted in figure 4.66, showing an 85nm 3dB bandwidth, which is sufficient for most applications. A field plot of the optimized grating coupler structure is shown in figure 4.67.

Again the tolerance of the first grating tooth width was assessed resulting in about the same alignment tolerance requirements as in the case of a uniform grating. Variation of the silicon layer thickness and grating etch depth leads in first order only to a shift in the coupling efficiency spectrum, as shown in figure 4.68, while random variations of the optimal design parameters by ± 10 percent only decreases the device efficiency by 10 percent.

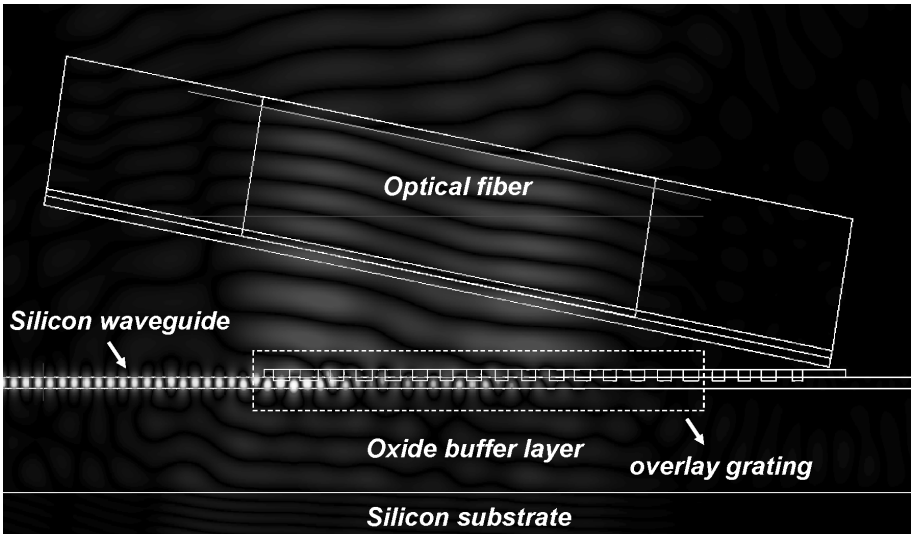


Figure 4.67: Field plot of the optimized grating coupler structure (excitation from the single-mode optical fiber)

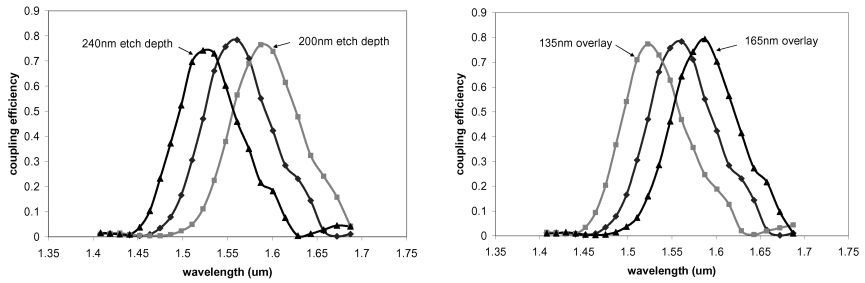


Figure 4.68: Tolerance analysis of the grating coupler structure: influence of the grating etch depth and silicon overlay thickness

Bloch mode analysis of the one-dimensional grating coupler structure

While in the previous section the directionality of the finite grating coupler structure was assessed, we will show in this section that there is a good correspondence between this type of analysis and an analysis based on the Bloch modes that exist in the infinitely extending periodic grating structure.

In order to optimize the grating coupler structure for efficient fiber coupling, the grating directionality (being the ratio of the fraction of optical power that is diffracted towards the optical fiber to the total diffracted power) needs to be maximized, while the grating coupling length needs to be optimized. Indeed, when the fundamental SOI waveguide mode is launched in the exciting waveguide, the upwards diffracted field profile can be written as

$$E_{diff} \propto \sqrt{\frac{D}{L_d}} \exp(-\frac{z}{2L_d}) \tag{4.10}$$

in which D is the directionality of the grating structure, L_d the grating coupling length and z the distance from the edge of the grating coupler structure. Assuming a Gaussian profile of the optical fiber mode

$$E_{fib} \propto \frac{1}{\sqrt{w}} \exp(-\frac{(z-\mu)^2}{w^2}) \tag{4.11}$$

the overlap integral between both field profiles can be maximized by optimizing the center position μ of the optical fiber and grating coupling length L_d for an optical fiber with a given width parameter w and a grating with directionality D. For a single-mode optical fiber with a width parameter w of 4.5μm, the overlap integral is maximally $0.81D$ for a grating coupling length L_d of 3.3μm. In order to optimize the grating coupler structure, the properties of the relevant leaky Bloch mode of the grating coupler structure were assessed, for various design parameters. A grating duty cycle of 50 percent was chosen, while the total waveguide layer thickness and the etch depth was varied. Both the directionality and the power attenuation length of the Bloch mode (which is identical to the grating coupling length) were calculated. The results are plotted in figure 4.69 for a total silicon waveguide thickness of 220nm, 290nm, 370nm and 440nm respectively. A grating period Λ of 610nm, a wavelength of 1.55μm and TE polarization are assumed, together with an infinite thickness of SiO_2 bottom cladding

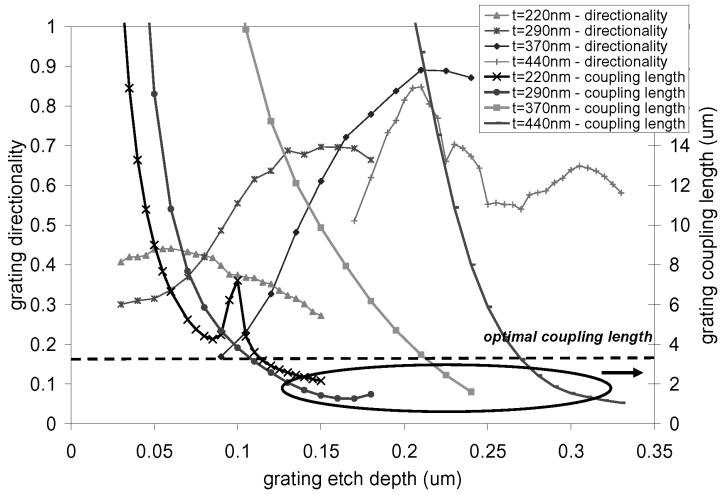


Figure 4.69: Directionality and attenuation length of the leaky Bloch mode supported by the grating structure as a function of grating etch depth

and air top cladding. From this figure, the improvement of the grating coupler directionality compared to the standard grating structure (corresponding to the t=220nm case) is impressive. An optimal performance is obtained for the 370nm silicon waveguide thickness case with an etch depth of 220nm, for which the optimal attenuation length coincides with the highest directionality of the grating structure. These grating parameters lead to a diffracted field that is tilted 10 degrees off vertical.

While the Bloch mode properties can be optimized for directionality and attenuation length, the excitation of this Bloch mode from a standard SOI waveguide also has to be maximized. As the diffracted field is sufficiently tilted off vertical, a large second order reflection can be avoided. In figure 4.70, the influence of the waveguide height of the exciting waveguide on the fiber coupling efficiency is plotted. A maximum coupling efficiency is obtained in the case of a 220nm SOI waveguide thickness exciting the optimized grating structure with total silicon layer thickness of 370nm and an etch depth of 220nm. A fiber-to-waveguide coupling efficiency of 67 percent is obtained.

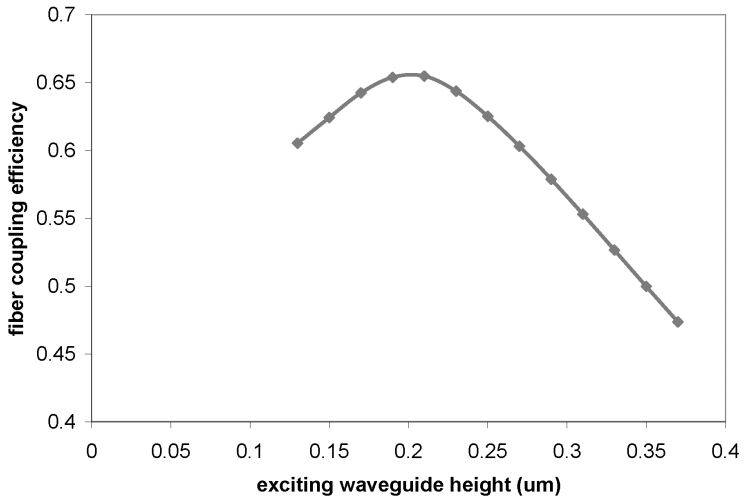


Figure 4.70: Fiber coupling efficiency as a function of the height of the exciting waveguide for the optimized grating coupler structure

Grating coupler for perfectly vertical positioned fiber

In the previous section, it was shown that a high coupling efficiency to optical fiber can be obtained using vertically etched slits, by optimizing the grating design. A uniform grating structure exhibiting a fiber coupling efficiency of 67 percent was designed, while using a non-uniform grating structure, 78 percent coupling efficiency can be obtained. The coupling efficiency was in this case dramatically improved by adding a silicon layer on top of the 220nm thick single-mode silicon waveguide layer prior to grating etching. However, these designs relied on slightly tilting the optical fiber with respect to the vertical axis (typically 10 degrees off vertical). This is required to avoid a large second order Bragg reflection back into the SOI waveguide in the case of perfectly vertical coupling, which dramatically reduces the fiber coupling efficiency. The requirement of the slight tilting of the optical fiber has important consequences for practical applications, which would require angled polishing of the fiber ferrule and mounting of the ferrule under an angle with respect to the substrate normal direction [16]. In order to avoid this costly complication in the packaging of the photonic integrated circuit, the possibility for perfectly vertical coupling in an efficient way is assessed here, by designing an asymmetric grating structure in order to avoid the large second order Bragg reflection. The grating structure can

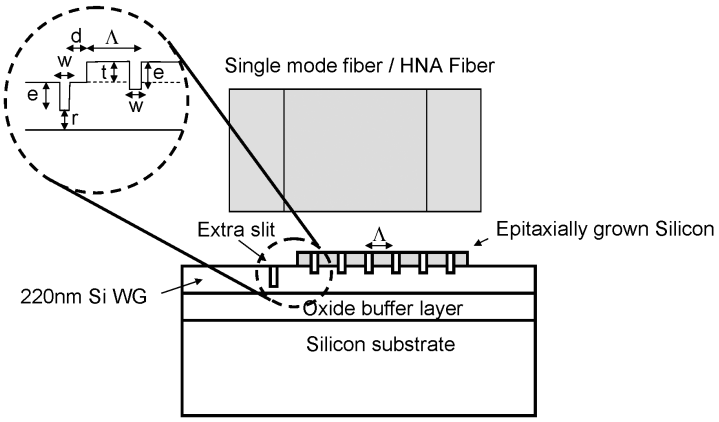


Figure 4.71: Layout of the fiber coupling structure for a perfectly vertically positioned optical fiber

be made asymmetric by tailoring the width and pitch of the individual grating slits. This is however not interesting from a fabrication point of view, as the practical realization of this type of structures is hampered by the different etch rate for slits with a different width. In this section, we will combine the previously mentioned approach of locally adding a silicon layer to improve the fiber coupling efficiency and incorporating an asymmetry in the grating coupler structure to avoid the large second order Bragg reflection, while maintaining a uniform grating structure in which all slits are identical in width and etch depth.

The structure we propose to allow efficient vertical fiber coupling is schematically depicted in figure 4.71. A 220nm silicon waveguide core layer on top of a 2μm buried SiO_2 layer is assumed. Locally, a silicon epitaxial layer of thickness t is grown in order to increase the directionality of the grating (being the ratio of the upwards diffracted optical power to the total diffracted power) as explained above. The asymmetry in the grating structure is created by etching one additional slit in the 220nm thick silicon waveguide layer instead of in the thicker epitaxial layer stack. This slit will function as a partially reflecting mirror to achieve destructive interference of the second order Bragg reflection from the uniform grating structure.

The behavior of the etched slit in the 220nm thick silicon waveguide layer as a partially reflecting mirror was assessed by calculating power reflection and scattered optical power as a function of the slit

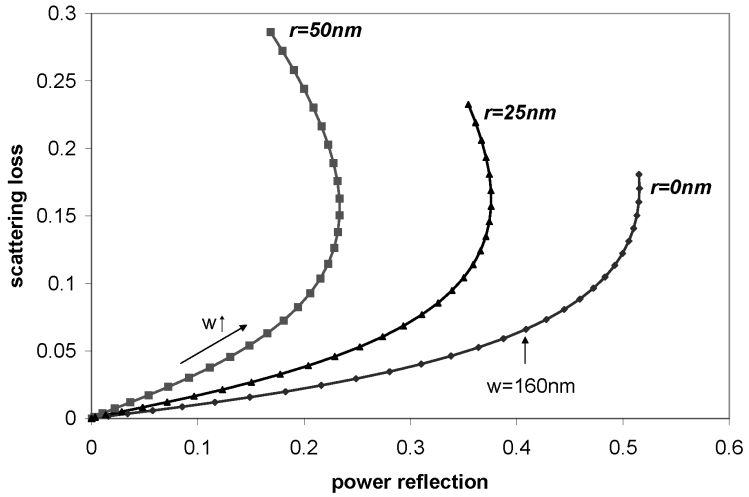


Figure 4.72: Scattering loss of a single slit in a 220nm SOI waveguide as a function of the power reflection for various slit widths and etch depths

etch depth, using the slit width w as a parameter. Results are shown in figure 4.72 for three different etch depths, corresponding to r=0 (etched through the silicon waveguide layer), r=25nm and r=50nm. From this simulation, it is clear that the completely etched through slit offers the largest reflection for a given acceptable scattering loss. Therefore, in the subsequent analysis, the slit is assumed to be etched completely through the 220nm silicon waveguide layer. This assumption also fixes the slit etch depth in the uniform grating structure to 220nm, for ease of fabrication as explained above. In order to keep the scattering losses low while maintaining a sufficient reflection, the minimum definable slit width using 248nm deep UV lithography of 160nm was chosen for the design. This then also fixes the slit width w of the diffractive grating structure in the thick silicon layer stack to 160nm.

In a second step of the optimization, the thickness of the epitaxially grown silicon layer t and the period of the grating structure Λ were optimized to achieve diffraction in the vertical direction at 1.55μm while maximizing the directionality of the grating at this wavelength. This can be done by evaluating the Bloch modes at the Γ-point (Bloch wavevector equal to zero) supported by the periodic grating structure and assessing the directionality of these leaky modes. Optimal directionality and vertical coupling at 1.55μm was obtained for a silicon epitaxial layer thickness t of 150nm and a grating period Λ of 560nm. The electric

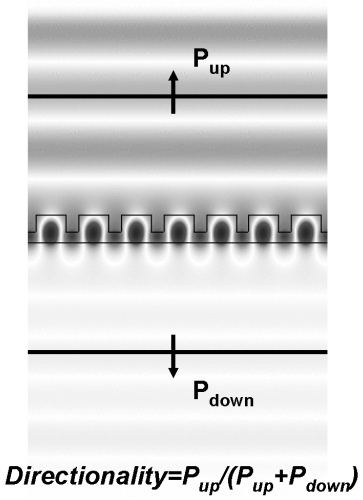


Figure 4.73: Bloch mode at the Γ-point with optimized directionality

field of this TE Bloch mode is plotted in figure 4.73. The directionality of the optimized grating structure is higher than 80 percent.

In order to appreciate the influence of the additional slit on the fiber coupling efficiency, the symmetric grating structure without the additional slit was simulated first. The fundamental TE mode at 1.55μm was launched in the SOI waveguide and the scattering by the grating structure was evaluated. In order to obtain the coupling efficiency to a single-mode optical fiber, the electric field E_{scat} at a certain distance above the grating structure was evaluated and the overlap integral of E_{scat} and a Gaussian beam, with its mode field diameter ($1/e^2$ intensity width) as a parameter, was evaluated. This was done for various center positions of the Gaussian beam profile, thereby obtaining the optimal position of the optical fiber, the optimal mode field diameter and the maximum achievable fiber coupling efficiency. For the uniform grating structure without the additional slit and the parameters mentioned above, a fiber coupling efficiency of 33 percent and 26 percent is obtained for a mode field diameter of 4μm and 9μm respectively. Reduced mode field diameters can be obtained by splicing a high numerical aperture fiber to a single-mode fiber with low optical loss at the splice [164]. This low coupling efficiency is, as mentioned above, due to the large second order Bragg reflection (55 percent in this case). In order to achieve destructive interference of this reflection in the pro-

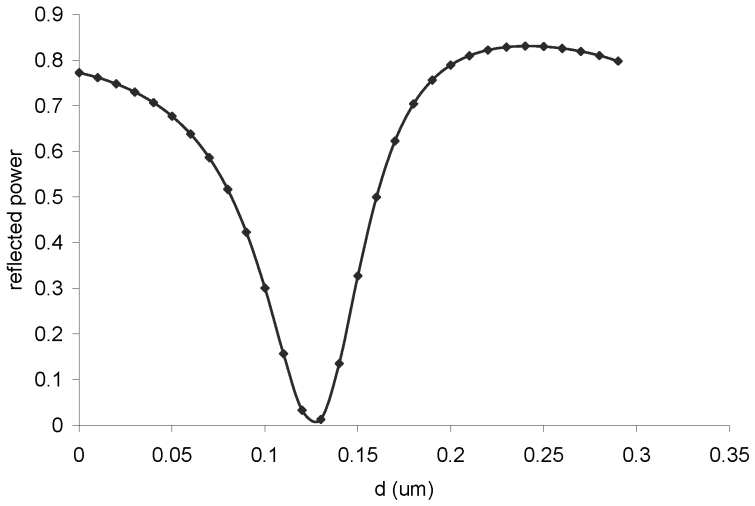


Figure 4.74: Influence of the distance d on the power reflection of the grating structure

posed design, the distance d between the additional slit and the edge of the thickened layer stack needs to be optimized. The power reflection as a function of the distance d, for the parameters mentioned above, is plotted in figure 4.74. This simulation shows that nearly perfect destructive interference can be obtained by choosing an optimal distance d of 0.13μm.

Using this optimal set of parameters, the coupling efficiency can be reassessed, showing that a fiber coupling efficiency of 65 percent and 50 percent can be obtained for a 4μm and 9μm diameter fiber respectively, with a 3dB bandwidth of approximately 55nm, while the 1dB bandwidth is about 35nm. This implies a 3dB improvement in coupling efficiency over the symmetric grating structure.

In order to further increase the fiber coupling efficiency, a non-uniform grating structure can be applied. As the width of the slits has to be kept identical throughout the grating structure for ease of fabrication, only the distance between subsequent slits can be varied. A genetic algorithm optimization was performed to maximize the coupling efficiency to optical fiber (both for a 9μm and for a 4μm mode field diameter). The fiber coupling efficiency increased from 65 percent (50 percent) for the uniform grating structure to 80 percent (60 percent) for the non-uniform grating structure in the case of a 4μm (9μm) mode field diameter. The fiber coupling efficiency spectrum for this non-uniform grating struc-

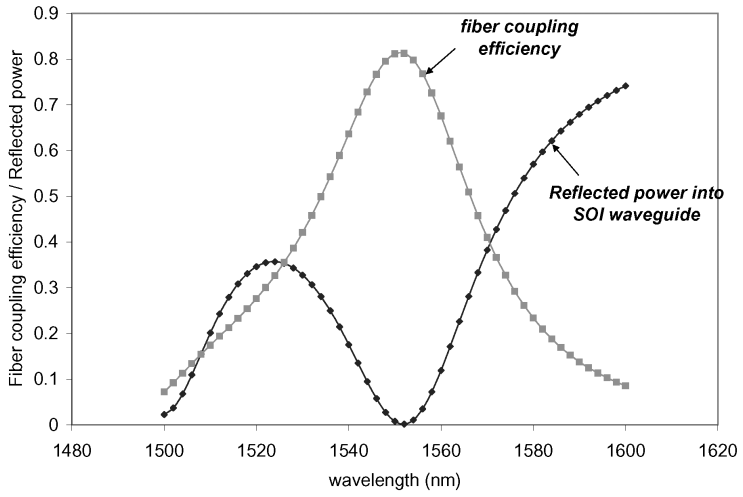


Figure 4.75: Non-uniform grating coupler: fiber coupling efficiency and reflection back into the SOI waveguide (for a 4μm mode field diameter optical fiber)

ture is plotted in figure 4.75, for the case of a 4μm mode field diameter. The power reflection back into the SOI waveguide, when the grating is excited from the left hand side waveguide, is also plotted.

A field plot of the optimized non-periodic structure, when illuminated by the 4μm diameter high numerical aperture fiber is shown in figure 4.76.

As can be seen from figure 4.75, the power reflection back into the SOI waveguide is minimal at 1.55μm, but rises quickly for a slight wavelength detuning. This limits the effective bandwidth of the grating coupler structure, as substantial reflection back into the SOI waveguide has to be avoided. In order to extend the effective bandwidth of the grating coupler structure, multiple additional slits in the 220nm SOI waveguide layer can be used to achieve a low power reflection over a broader wavelength range. Optimization of a non-uniform grating structure, with two slits etched in the standard 220nm silicon waveguide, was carried out using a genetic optimization algorithm as well. A high numerical aperture fiber with a mode field diameter of 4μm was assumed. The average fiber coupling efficiency at 1.54μm and 1.56μm was maximized, while minimizing the average power reflection at these wavelengths. The resulting fiber coupling efficiency spectrum and power reflection spectrum is plotted in figure 4.77.

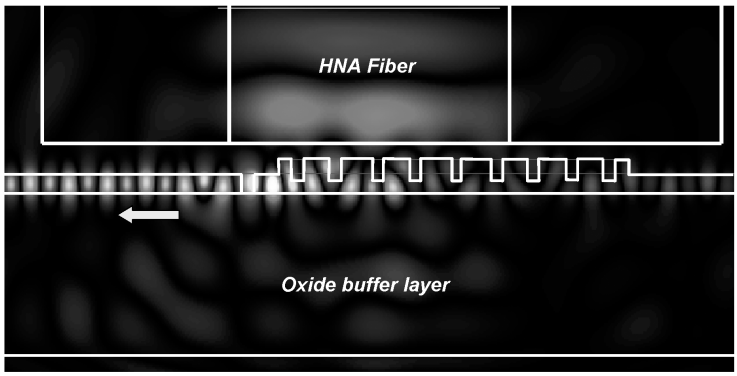


Figure 4.76: Field plot of the optimized coupling structure - a non-uniform grating coupler and a high numerical aperture fiber is used (excitation from HNA fiber)

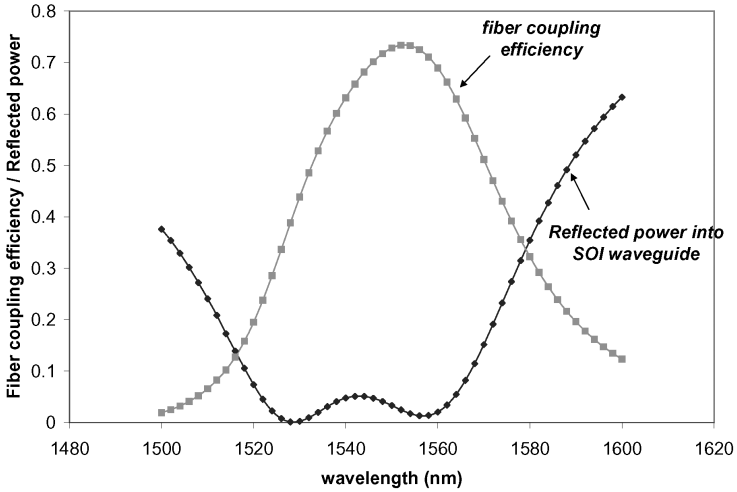


Figure 4.77: Non-uniform grating coupler: fiber coupling efficiency and reflection back into the SOI waveguide for a double slit configuration

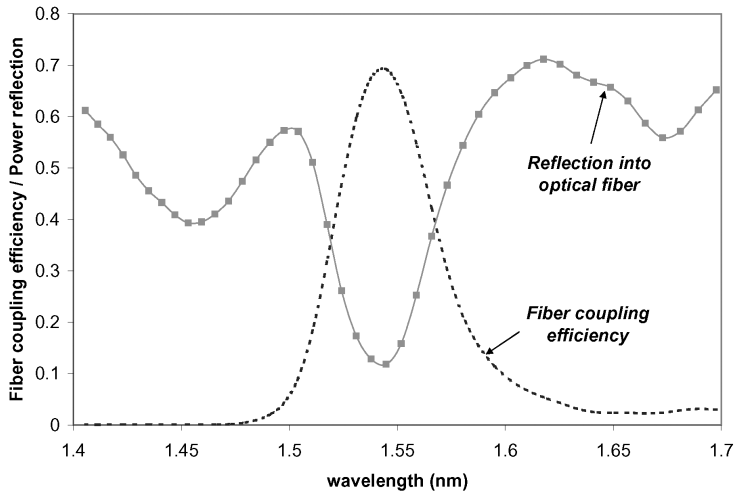


Figure 4.78: Non-uniform grating coupler: power reflection into the optical fiber for a double slit configuration

As can be seen from this simulation, the effective bandwidth of the device has improved, at the expense of maximal fiber coupling efficiency compared to the single slit configuration.

When used as a coupling structure to couple light from an optical fiber into the SOI waveguide circuit, the power reflection into the single-mode fiber needs to be considered. For the non-uniform two slit configuration, this power reflection spectrum is plotted in figure 4.78. As can be seen from this simulation, the power reflection is relatively high for a slight detuning from the central wavelength. This is related to the excitation of the "quasi-Bloch mode" at the Γ-point, which was designed to have a high directionality towards the optical fiber, hence resulting in a high reflection coefficient for the wavelengths that are not efficiently coupled to the SOI waveguide. While this drawback can be circumvented by implementing an optical isolator in the optical fiber path, the application of an anti-reflection layer stack on top of the grating structure could reduce this parasitic reflection. This is however beyond the scope of this work.

While device optimization was performed for a one-dimensional grating coupler, the same approach can be used to optimize a two-dimensional grating coupler structure for polarization diversity operation.

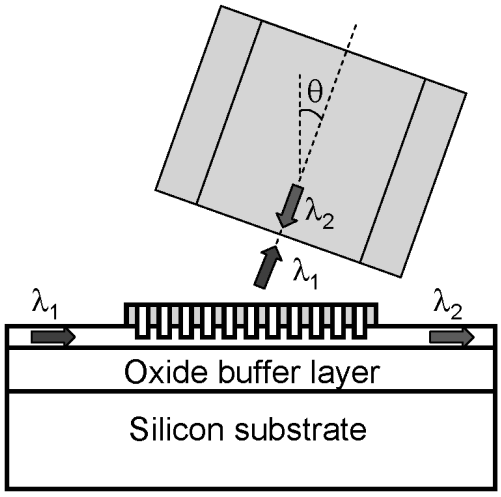


Figure 4.79: Layout of the one-dimensional grating structure proposed for duplexer operation

Although the device structure was presented here as a structure to couple light exiting a vertically positioned single-mode optical fiber into the SOI waveguide circuit, the same device structure can be used to achieve optical coupling between an integrated VCSEL and the SOI waveguide circuit. In case the VCSEL structure is polarization stable, a one-dimensional grating structure can be used. In the case where polarization switching can occur (either through the lack of polarization stabilization features in the VCSEL layout or through the different reflection coefficient for TE and TM polarization from the one-dimensional grating structure), a two-dimensional grating structure can be used in polarization diversity configuration.

Grating coupler as a wavelength duplexer

Additional functionality for the grating coupler structure can be obtained, by utilizing both waveguides that originate from the 1D grating coupler as shown in figure 4.79. This structure can be used to spatially separate two wavelength bands in the two waveguides and is therefore referred to as a duplexer.

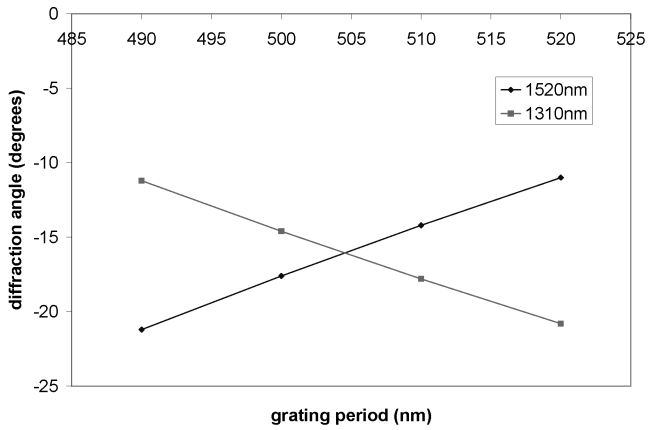


Figure 4.80: Design of the grating period and fiber tilt for duplexer operation

Typical application is the separation of wavelength channels around 1300nm and 1550nm, although other pairs of wavelength bands can be envisaged. Due to reciprocity, both wavelength bands can be used both for downstream and for upstream data traffic. In order to obtain a high coupling efficiency, a silicon overlay approach can be used. By optimizing the grating coupler period and tilt angle of the optical fiber, a set of two - not too closely spaced - wavelength bands can be spatially separated. As the grating directionality is only moderately dependent on the grating period as was shown in figure 4.64, the same silicon overlay thickness (150nm), grating etch depth (220nm) and grating duty cycle (50 percent) is used as in the previous section. In figure 4.80, the diffraction angle θ of a 1520nm (1310nm) wavelength beam, when the grating duplexer is excited by the fundamental waveguide mode incident from the left (right) side of the grating, is plotted as a function of the grating period. By varying the grating period, the diffraction angles can be matched, which is the required condition for duplexer operation.

Additional design parameters to consider are the number of grating periods and the position of the optical fiber, which is dependent on the grating coupling strength. This involves making a compromise to obtain a maximum average coupling efficiency for the center wavelengths of both wavelength bands to be separated. The coupling efficiency for both center wavelengths can be written as

$$C_1 = \left| \int_0^L \sqrt{D_1 \kappa_1} \exp(-\frac{\kappa_1 z}{2}) \frac{1}{\sqrt{w\sqrt{(\frac{\pi}{2})}}} \exp(-\frac{(z-\mu)^2}{w^2}) dz \right|^2$$
$$C_2 = \left| \int_0^L \sqrt{D_2 \kappa_2} \exp(-\frac{\kappa_2 (L-z)}{2}) \frac{1}{\sqrt{w\sqrt{(\frac{\pi}{2})}}} \exp(-\frac{(z-\mu)^2}{w^2}) dz \right|^2 \quad (4.12)$$

in which C_1 and C_2 are the coupling efficiencies of the 1520nm center wavelength and the 1310nm center wavelength respectively. κ_1 and κ_2 are the power attenuation coefficients for both wavelengths and D_1 and D_2 are the grating directionalities for the respective wavelengths. L is the length of the grating structure, while the parameters of the mode profile of the optical fiber are determined by w (determining the mode field diameter $2w$) and μ, determining the center of the mode profile. Approximately, D_1 equals D_2 and κ_1 equals κ_2, which both depend on the parameters of the grating unit cell. For a power attenuation coefficient of 0.36μm^{-1}, a grating directionality D normalized to 1 and a mode field diameter $2w$ of 10.4μm, the average coupling efficiency $(C_1 + C_2)/2$ can be written as a function of L and μ and is plotted for a grating length L of 5, 8, 11 and 14μm in figure 4.81. From this plot it is clear that there exists an optimum grating length for maximum average coupling efficiency, which lies around 70 percent (assuming a directionality D equal to 1).

A coupling spectrum and field plot of the optimized duplexer structure for the center wavelengths is plotted in figure 4.82 and 4.83 (for both wavelengths the optical fiber mode is excited). The grating period is 505nm and the tilt of the optical fiber is 16 degrees off vertical as can be deduced from figure 4.80. A coupling efficiency of 60 percent for both wavelength bands can be obtained.

While the grating length can be optimized to achieve a maximal average coupling efficiency, the length of the device also determines the crosstalk between both wavelength bands, in the case one wavelength band is used for upstream traffic, while the other wavelength band is used for downstream traffic, as shown in figure 4.84. The influence of the grating length on the average fiber coupling efficiency, the 1310nm wavelength band crosstalk and the 1520nm wavelength band crosstalk levels are plotted in figure 4.85. As only modest crosstalk levels can be achieved, while maintaining a high average fiber coupling efficiency, additional spectral filtering will be required in practical applications.

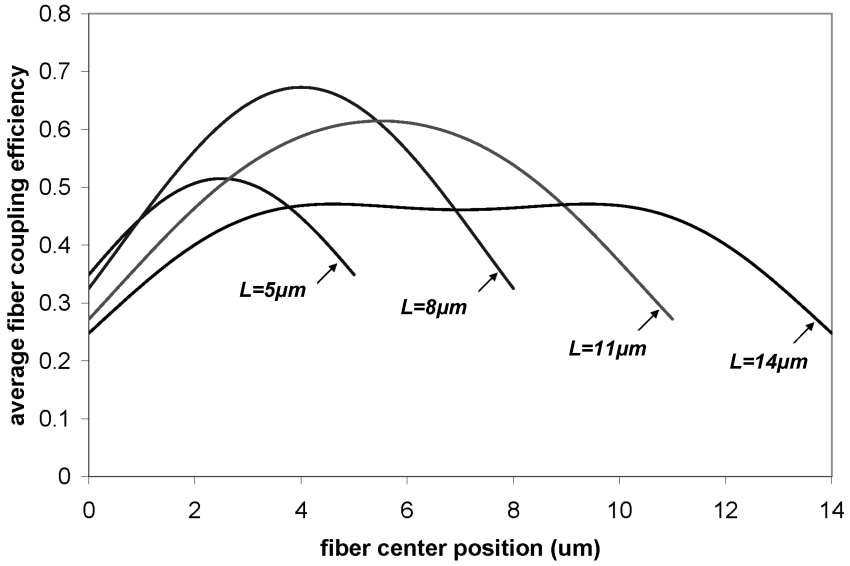


Figure 4.81: Influence of the grating length L and the fiber center position μ on the average coupling efficiency - a grating coupling strength of $0.36\mu\text{m}^{-1}$ for both center wavelengths is assumed

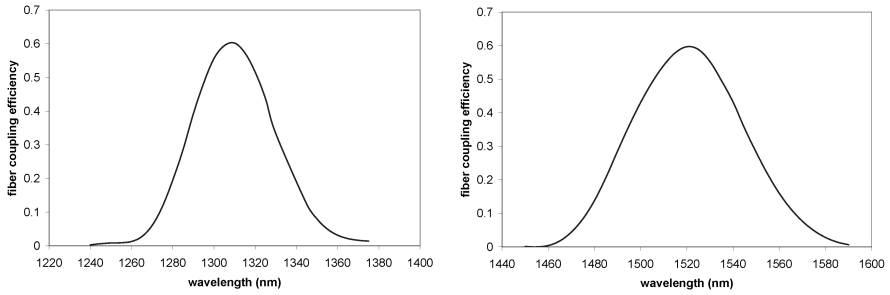


Figure 4.82: Duplexer fiber coupling efficiency spectrum for both wavelength bands

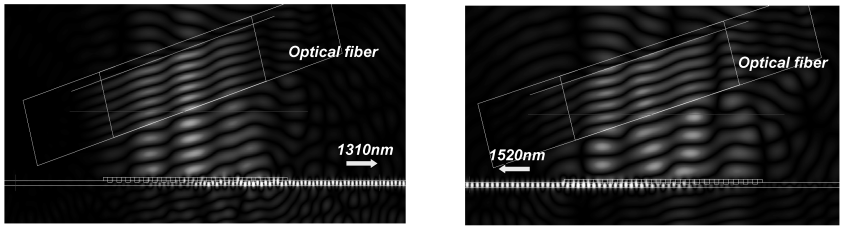


Figure 4.83: Duplexer fiber coupling field plot for 1310nm and 1520nm center wavelength (excitation from the optical fiber)

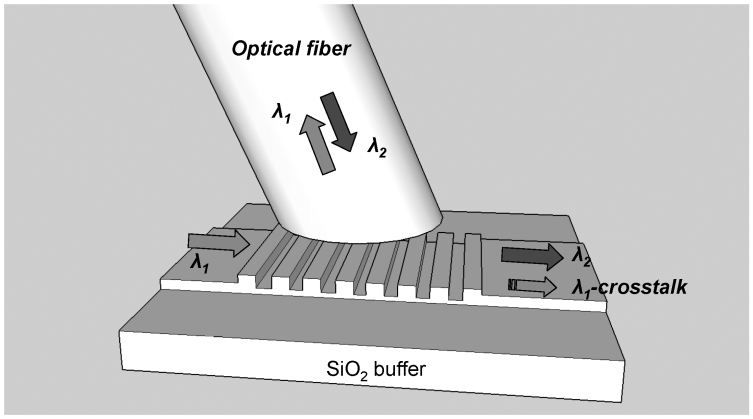


Figure 4.84: Origin of crosstalk for a one-dimensional duplexer device

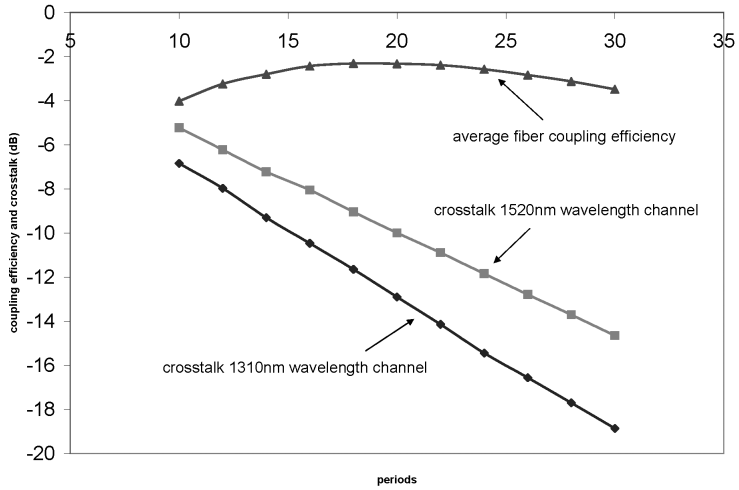


Figure 4.85: Crosstalk as a function of the number of grating periods for a one-dimensional duplexer device

The bandwidth of the fiber coupling spectrum can further be expanded by using a high numerical aperture fiber, which has a reduced core size and a larger acceptance angle, thereby increasing the wavelength span that is efficiently collected at the expense of reduced alignment tolerance. This can be required for the application of the duplexer in a FTTH (fiber-to-the-home) network in which both 1490nm and 1550nm downstream wavelength channels are used at the subscriber side (next to the 1310nm upstream wavelength channel).

While only one-dimensional grating coupler structures were discussed, the extension to two-dimensional grating structures to obtain polarization insensitivity [139] can be made. Rigorous simulation of these grating structures requires extensive computational resources however, as a complete three-dimensional structure - multiple wavelengths wide on each side - needs to be simulated. In the next section we will show however, that the analysis of the Bloch modes of the grating structures can give insight in the diffraction properties of the finite grating structures (i.e. the obtainable coupling efficiency and grating diffraction angle). As these Bloch modes can be calculated, even in three dimensions, with limited computational resources, the number of full three-dimensional analyses required to obtain a high-efficiency grating coupler design, can be dramatically reduced.

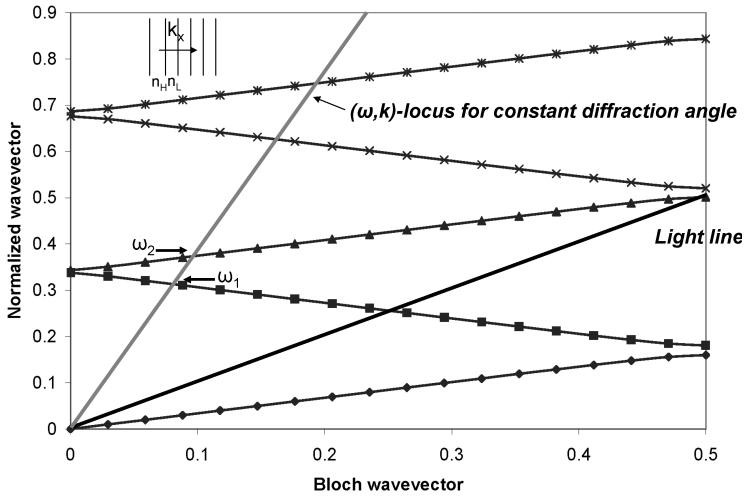


Figure 4.86: Band structure of a one-dimensional periodic structure - duplexer operation

Bloch mode analysis of the duplexer operation of the grating coupler structures

In order to acquire a better understanding of these grating structures for duplexer operation, it is interesting to relate this duplexer behavior to the band diagram of the periodic structure under investigation. The band diagram for TE polarization in the irreducible Brillouin zone for a one-dimensional grating structure ($n_H = 3.22$, $n_L = 2.66$ and 50 percent duty cycle) in an effective index approximation is plotted in figure 4.86, together with (ω,k)-locus for radiating modes with a constant angle of light diffraction in air. Normalized frequency and normalized Bloch wavevectors are used.

As the diffraction angle is given by

$$\tan(\theta) = \frac{k}{\omega} \tag{4.13}$$

this equation describes a line starting in the origin of the band diagram, forming an angle with the vertical axis determined by the diffraction angle θ. As can be seen, this line intersects the second and third band, determining the normalized frequencies ω_1 and ω_2 for which duplexer operation can be expected. Moreover, the group velocity $v_g = \frac{d\omega}{dk}$ of both Bloch modes have opposite signs as is clear from the operation

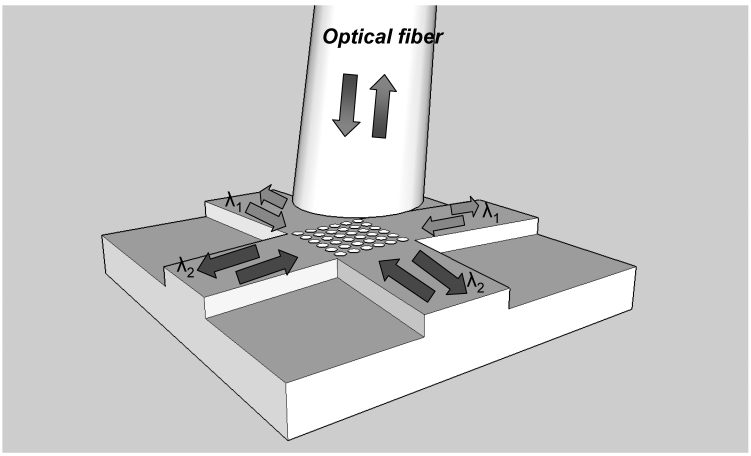


Figure 4.87: Four port duplexer device configuration for polarization insensitive operation for both wavelength bands

principle of the device. The choice of the diffraction angle determines the ratio of the optical wavelengths for which duplexer operation can be obtained. The actual wavelengths are tuned by scaling the grating dimensions, due to the scale invariance of Maxwell's equations. From this "geometrical" analysis it is clear that the duplexer operation is not limited to the specific wavelength bands for FTTH applications as described above, but can be extended to other wavelength bands of interest.

As in the previously discussed case of a one-dimensional grating structure, the behavior of the grating structure is very different for TE and TM polarization, a two-dimensional grating structure is required to achieve polarization independent operation. Two configurations can be envisaged. In the four port device shown in figure 4.87, polarization independent operation can be achieved for both spatially separated wavelength bands, while in the three port configuration, shown in figure 4.88, only polarization independent operation can be achieved for a single wavelength band, while there is still a strong polarization selectivity for the other wavelength band. At the intersection of the waveguides, a two-dimensional square lattice grating is required.

In order to achieve insight in the operation principle of this two-dimensional grating structure, a two-dimensional analysis of the band diagram in the irreducible Brillouin zone was performed, as shown in figure 4.89. The two-dimensional grating structure that is analyzed is

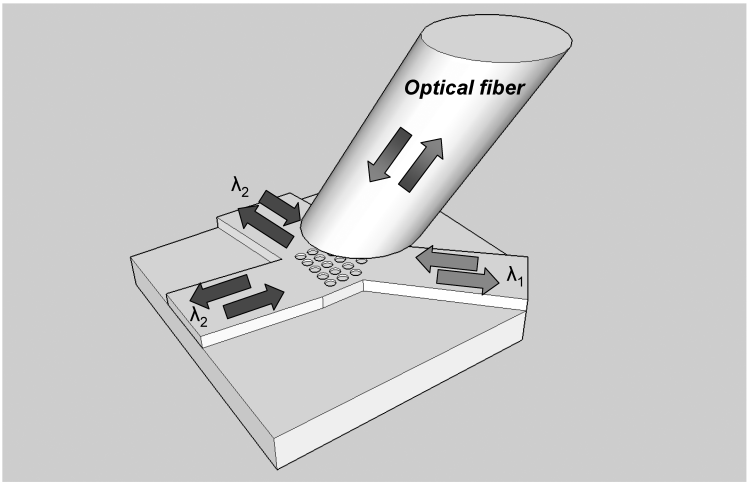


Figure 4.88: Three port duplexer device configuration for polarization insensitive operation for a single wavelength band

shown in the inset. It consists of low refractive index rods ($n_L = 2.66$, diameter $0.4a$) in a high refractive index material ($n_H = 3.22$). Only the TE polarized bands lying along the (Γ,M)-direction are shown in figure 4.89, as only these modes have the required symmetry along the bisection line of the grating structure in order to achieve polarization independent operation. Again, the (ω,k)-locus for radiating modes with a constant angle of light diffraction in air, intersects several bands.

From this picture, the two duplexer configurations depicted in figure 4.87 and 4.88 can be deduced, depending on which Bloch modes that intersect with the (ω,k)-locus are considered. To clarify this, the associated electric field profiles of the corresponding Bloch modes are plotted in figure 4.90.

As the bands (2a,2b) and (3a,3b) nearly coincide, these are the set of bands that allow for polarization independent operation. Selecting bands (2a,2b) and (3a,3b) for duplexer operation results in the four port duplexer configuration shown in figure 4.87. Note the opposite direction of the group velocity for both set of bands. For the three port duplexer configuration, bands (3a,3b) and band 4 are selected. Again, the Bloch modes have an opposite group velocity direction.

As the excited Bloch modes contain a non-zero Bloch wavevector component along the grating/waveguide interface (at least for the wavelength bands used in polarization diversity configuration), the wave-

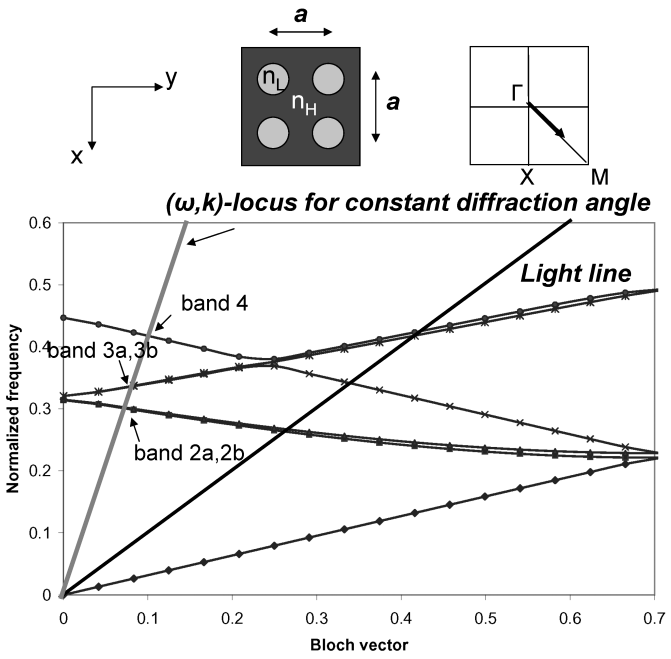


Figure 4.89: Band structure along the (Γ,M)-direction of a two-dimensional periodic structure - duplexer operation

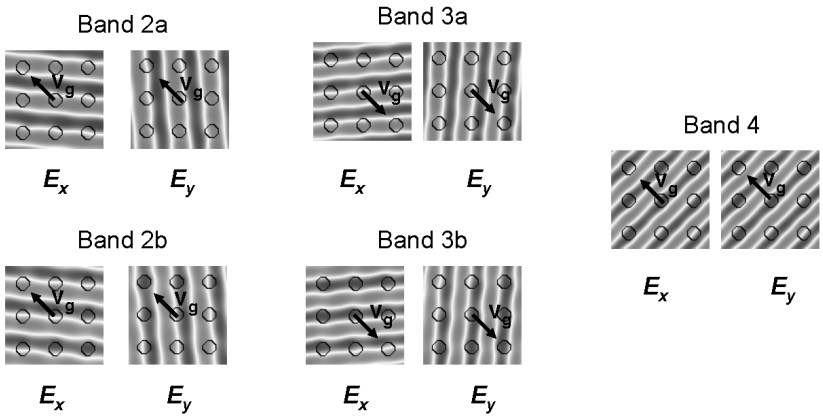


Figure 4.90: Electric field profiles of the duplexer Bloch modes - the group velocity direction of the Bloch mode is also indicated

guides originating from the two-dimensional grating structure need to be tilted accordingly, in order to obtain a high coupling efficiency to the fundamental mode of the waveguide. This tilt depends on the dispersion relation of the fundamental waveguide mode and can be geometrically constructed, as continuity of the Bloch wavevector component along the grating/waveguide interface is required.

While in this section a two-dimensional analysis was carried out in order to get insight in the operation principle of the polarization independent operation of the duplexer structure, a three-dimensional analysis is required in order to optimize the directionality of the Bloch modes, and assess the fiber coupling efficiency and crosstalk of the proposed grating structure. This lies however outside the scope of this work.

Due to the relevance of this type of device for application in FTTH transceivers, a patent application was filed for this type of devices.

4.7 Conclusions

In this chapter, different coupling schemes were designed for optical coupling between an SOI waveguide layer and a bonded InP/InGaAsP device layer on top. Comparison of the different coupling schemes showed that adiabatic coupling provides the best combination of optical performance and fabrication tolerance for in-plane operating devices. From a fabrication point of view the structure based on polymer waveguides is less complicated. The inverted adiabatic structure requires ultra-thin bonding layers however. An alternative for thick bonding layers was also proposed, but in this case processing is more complicated. Also, the use of beveled facets and a grating coupler allows high-efficiency coupling on a small footprint, using a thick bonding layer approach. This requires the development of a fabrication process for the beveled facets however. For vertically operating devices, a coupling scheme based on a diffractive grating structure was presented.

As an additional result, two of the developed coupling schemes (adiabatic taper coupler and grating coupler scheme) were adapted to coupling to optical fiber, resulting in improved fabrication tolerance and improved coupling efficiency respectively compared to previously published results. In this work, the idea of using the grating structure as a wavelength duplexer, to spatially separate two wavelength bands, was developed.

The work presented in this chapter has been the subject of 4 publications in international journals (Appendix B.2-1,B.2-4 and B.2-8, B.2-11 and B.2-12) and one patent application.

Chapter 5

Waveguide technology

Smooth
Santana

In the previous chapters, the use of SOI and InP/InGaAsP waveguide structures for photonic integrated circuits was discussed. In this chapter we will outline the technology used for fabrication of both SOI waveguides and InP/InGaAsP waveguides. Results on waveguide losses in both material systems will be presented. As a part of the waveguide technology development, we will present in this chapter the fabrication and properties of two types of fiber-to-waveguide coupler structures: the inverted adiabatic taper structure and a grating coupler based on a silicon overlay.

5.1 Materials

5.1.1 Silicon-on-insulator

There are several methods to fabricate silicon-on-insulator wafers. The highest quality layer structures are obtained using a direct wafer bonding process (the UNIBOND process by SOITEC). The fabrication procedure is outlined in figure 5.1. One starts from two bare silicon wafers (A and B) of which wafer A is thermally oxidized (the thickness of this oxide layer determines the buried oxide layer thickness). After implantation of hydrogen in wafer A to a certain depth (determining the final silicon core layer thickness), the surfaces of both wafers are cleaned and chemically activated and wafer A and B are bonded at room temperature (a hydrophilic direct bonding process is used). After bonding, first

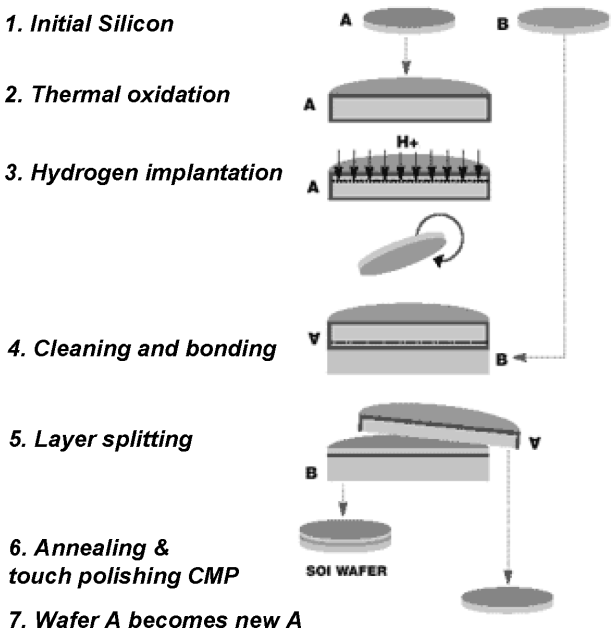


Figure 5.1: Fabrication process of SOI wafers by direct wafer bonding and applying the SmartCut process

a low temperature annealing step is performed to enhance the bonding strength, after which a high temperature anneal is performed to split the hydrogen implanted silicon wafer from the device layer. This splitting is caused by the formation of micro-cracks in the silicon due to the implantation of hydrogen. The annealing at high temperature increases the internal pressure of the formed H_2 molecules in the micro-cracks, which allows the crack to propagate and finally split off the wafer. After splitting, the silicon top layer is CMP polished to reduce the roughness of the silicon surface. After polishing, the split-off wafer can be used in the fabrication of the next silicon-on-insulator wafer.

5.1.2 InP/InGaAsP heterostructures

InP/InGaAsP epitaxial layer structures were grown on 2 inch InP substrates, using metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). While MOCVD grown wafers typically show a larger micro-roughness compared to MBE grown wafers, DVS-BCB bonding was successful on both types of substrates.

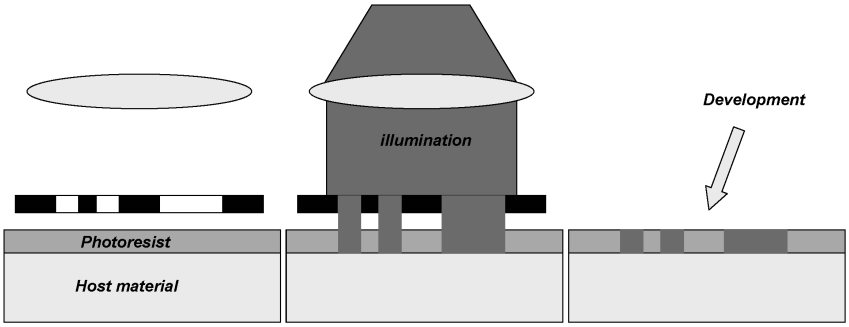


Figure 5.2: Contact lithography

5.2 Optical lithography

As structures need to be defined in the semiconductor material, the pattern from a mask needs to be transferred to the substrate. This is done by illumination of a photo-sensitive layer, a so called photoresist, through a mask, which contains the structure that needs to be printed in the photoresist. Two types of lithography processes can be used: either a contact lithography process, in which the mask makes contact with the photoresist coated substrate, or a projection lithography system, in which the pattern is projected onto the structure using intermediate optics. In contact lithography the quality of the mask degrades over time as it is in direct contact with the substrate. In projection lithography the mask is not in contact and the patterns are typically four times magnified on the mask (and reduced to the original size by the projection optics).

5.2.1 Contact lithography

Contact lithography (see figure 5.2) is mostly used for the definition of patterns in photoresist on InP/InGaAsP epitaxial layer structures due to the lower cost of the lithography system. As the illumination wavelength typically is limited to 320nm, the feature size for dense features is limited to approximately 500nm. While this is sufficient for standard III-V processing, this resolution is insufficient for nanophotonic structures.

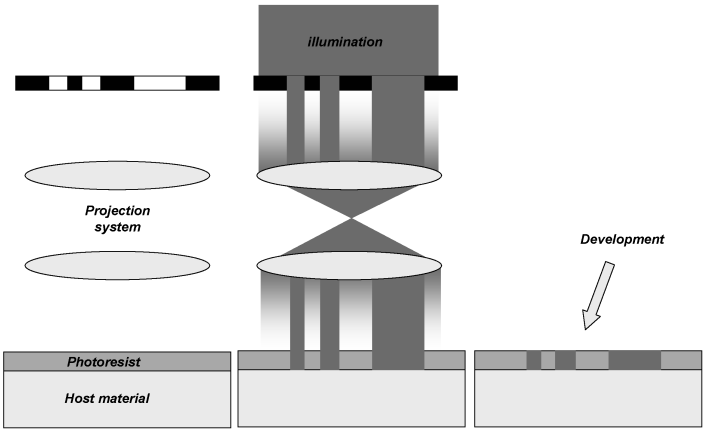


Figure 5.3: Projection lithography

5.2.2 Deep UV projection lithography

Deep UV lithography differs from conventional lithography in the illumination wavelength and illumination optics. With wavelengths of 248nm, 193nm and in the future 157nm, and high numerical aperture optics, much higher resolutions can be reached. However, this comes at considerable cost. The high quality projection optics for deep UV wavelengths are extremely complex. As the obtainable resolution for dense features is much higher, this is the preferred technology for the fabrication of nanophotonic structures, with the ability of mass manufacturing.

5.3 Focused ion beam etching

For rapid prototyping of nanophotonic devices, both e-beam lithography and focused ion beam (FIB) etching can be used. As these are inherently slow writing processes, they cannot be used for mass fabrication. While in e-beam lithography a resist is exposed to a fine electron beam and developed afterwards, in focused ion beam etching a pattern is directly written into the material without using a resist mask.

The basic principle of focused ion beam etching is to use a fine beam of high energy particles (in practice these are gallium ions with an energy ranging from 1keV to 100keV). Due to their high energy, incident ions cause multiple collisions with the atoms of the host material, al-

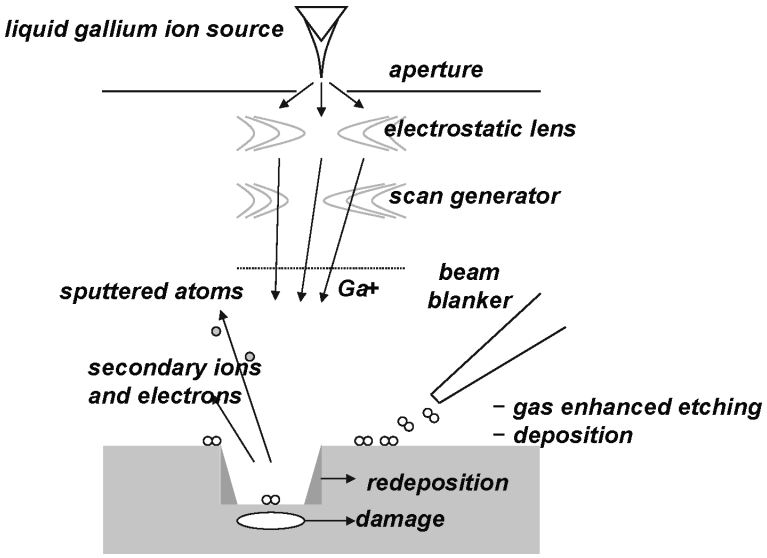


Figure 5.4: Focused ion beam etching

lowing for some atoms to leave the material (referred to as sputtering or milling). This process always leaves an area of amorphous material and gallium ions are incorporated in the material. Besides this direct milling process, FIB can also be used to deposit material or selectively etch materials due to the presence of a gas in the etching chamber.

The operation principle of focused ion beam etching is shown in figure 5.4.

5.4 Silicon waveguide technology

5.4.1 Lithography process

Photoresist is coated on top of a 200mm SOI wafer, and then pre-baked. On top of the photoresist, an anti-reflective coating is spun to eliminate reflections at the interface between the air and the photoresist. These reflections would induce standing waves in the photoresist, and therefore lead to inhomogeneous illumination. After photoresist coating, the wafer is sent to the stepper, which illuminates the photoresist with the pattern on the mask. As a 200mm wafer can contain many dies, the pattern is repeated across the wafer. While stepping over the wafer surface, the exposure conditions (focus and exposure dose) can be var-

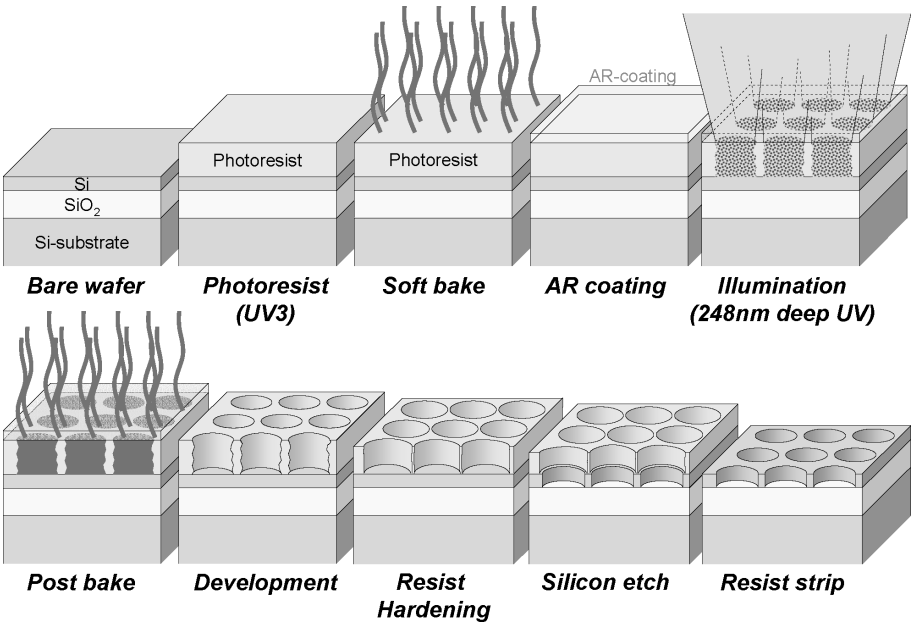


Figure 5.5: Processing of SOI nanophotonic structures

ied, which makes it possible to do detailed process characterization. After lithography, the resist goes through a post-exposure bake, and is then developed. For our experiments, Shipley UV3 resist is used. The developed photoresist is then used directly as a mask for etching. The process flow is depicted in figure 5.5.

5.4.2 Silicon etching process

For the silicon etch, a low-pressure/high-density $Cl_2/O_2/He/HBr$ plasma chemistry is used. The etch recipe consists of a break-through etch and a main etch, with different chemistry. More information on the waveguide fabrication process can be found in [13].

5.4.3 SOI waveguide losses

Losses down to 2.4dB/cm (λ=1.55μm, TE polarization) were presented in literature on 500nm wide photonic wires, fabricated using the process described above [15]. These loss values are sufficiently low to fabricate high quality optical functions in silicon-on-insulator. While losses are low for 500nm wide photonic wires, they increase rapidly with de-

Figure 5.6: SEM image of an overexposed and an on-target taper tip

creasing waveguide width (i.e. the loss of a 400nm wide photonic wire is about 35dB/cm). More information on this type of components can be found in the PhD of P. Dumon.

5.4.4 Fabrication of SOI taper tips

As discussed in the previous chapter, a coupling scheme based on an adiabatic inverted taper approach, shows the best performance in terms of optical bandwidth, efficiency and fabrication tolerance. However, the fabrication of the taper tips using deep UV lithography can be a cause of concern.

Deep UV lithography versus e-beam lithography

While adiabatic inverted tapers were already published in literature before this work [145, 162], the taper tips in these structures were always sub 100nm wide and defined using e-beam lithography. Although e-beam lithography is an excellent tool for research, providing very high resolution lithography, it is an inherently slow writing process and not suitable for mass fabrication. Therefore, the use of 248nm deep UV lithography was explored in this work for the fabrication of the taper tips. By varying the exposure dose of the taper structures and varying the taper tip widths on the (e-beam written) mask, we could conclude that an effective taper tip width of 175nm can be achieved. An SEM image of an overexposed and an on-target taper tip is plotted in figure 5.6.

The overexposure of the photoresist led to a delamination of the photoresist during development, resulting in an uncontrolled structure. A top view and a cross-section image of an on-target taper tip is also shown. The trapezoidal shape of the wire is clear, leading to the definition of an effective taper tip width for which the same coupling efficiency to the polymer waveguide is obtained using a vertically etched waveguide as for the trapezoidal shaped waveguide. The effective taper tip width is about 200nm in this case.

While only the standard lithography process was used in this work to define the taper tips, additional refinement could be done to further decrease this taper tip width. Photoresist trimming using a plasma process could be used to further decrease the feature size of the taper tips, at the expense of inducing the same dimensional changes in the other defined structures. Another way of overcoming the problem is local thermal oxidation of the taper using Si_3N_4 as an oxidation mask (LOCOS process) [165]. As the required taper tip width could be reached using the standard process, due to the inclusion of a DVS-BCB spacer layer as discussed in section 4.6.4, these additional processes were not further explored.

5.4.5 SOI inverted adiabatic taper coupler

Fabrication procedure

In order to find the optimal processing parameters for lithography of the taper tips, in this work a set of tapers, with varying taper tip widths on the mask, were printed on a silicon-on-insulator wafer, varying the exposure dose over the wafer. After etching the silicon waveguide core, the dimensions of the fabricated structures were measured. The results are plotted in figure 5.7.

As the cross-section of the taper tips is trapezoidal, both the top and bottom width of the waveguides were measured. Increasing exposure dose resulted in a decrease in taper tip width. When the exposure dose exceeded a critical value (depending on the original taper tip width on the mask), the photoresist delaminated from the silicon-on-insulator substrate during development. Therefore, these structures were omitted from the measurements. From this characterization we can conclude that the narrowest taper tips that can be defined are obtained using a 190nm wide taper tip on the mask and an exposure dose of 12mJ/cm^2. The 120nm top and 210nm bottom waveguide width lead to an effective taper tip width (as defined in section 5.4.4) of 175nm.

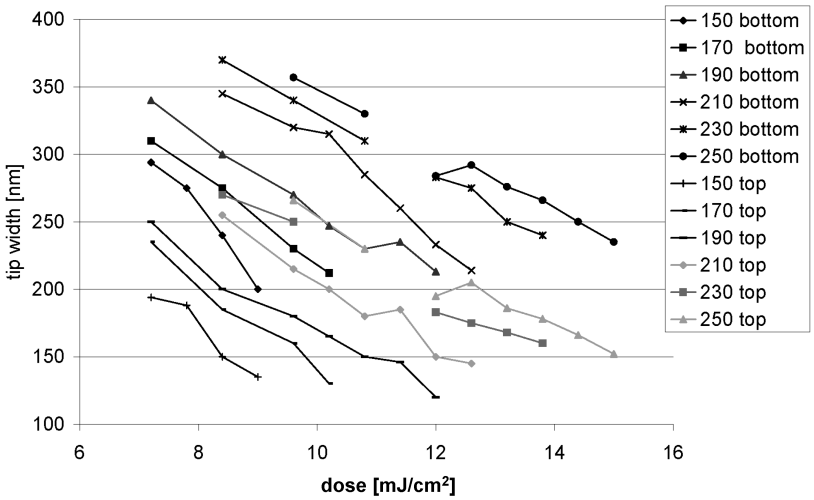


Figure 5.7: Characterization of the taper tip definition process - influence of the lithography dose on the waveguide tip cross-sectional dimensions (for various taper tip widths on the mask)

After definition of the taper structures (with the parameters of figure 4.58), a 200nm DVS-BCB film was spin coated on top of the SOI waveguide structure. After curing, a polyimide waveguide core layer of 1.3μm thick was applied and the polymer waveguide core was etched using a 100nm titanium mask and ICP plasma etching. After removal of the titanium mask using diluted HF, a thick DVS-BCB top cladding was applied. The refractive index of the polyimide and DVS-BCB for TE polarization at 1.55μm is 1.67 and 1.54 respectively, characterized using a Metricon 2010 prism coupling setup.

Measurement results

The structure used to characterize the inverted taper adiabatic spot size converters in this work is shown in figure 5.8. A grating coupler was used to inject light into the fundamental TE waveguide mode of the SOI waveguide, while a lensed fiber with a spot size of 2.5μmx2.5μm or an objective lens was used to collect the light at the polymer waveguide facet. The lensed fiber had a specified loss of 0.5dB while the loss of the objective lens light collection was negligible. The grating coupler used in the experiments was characterized to have 7dB loss and a 60nm 3dB bandwidth. Figure 5.9 shows a transmission spectrum, measured

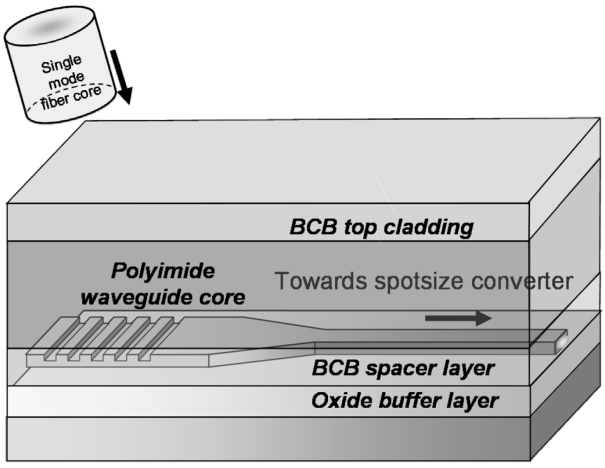


Figure 5.8: Structure used to characterize the spot size converters

by light collection using an objective lens. The coupling efficiency of the grating coupler is superimposed. This measurement implies that the SOI spot size converter itself shows 1dB loss. Transmission experiments using a lensed fiber were also carried out. A coupling loss from lensed fiber to a 590nm wide SOI waveguide of 1.9dB was measured. This 0.9dB extra loss is caused by the mode mismatch between the polymer waveguide mode and the lensed fiber mode and the additional 0.5dB specified loss of the lensed fiber.

A microscope view of the fabricated structures, showing the polyimide waveguides and fiber grating couplers is shown in figure 5.10.

5.4.6 SOI grating coupler with silicon overlay

In the previous chapter, the use of an SOI grating structure to couple light from an optical fiber into an SOI waveguide, was discussed. We predicted an improved fiber coupling efficiency by defining an additional silicon layer on top of the standard 220nm SOI waveguide layer, prior to grating definition. This silicon layer can be epitaxially grown, or a poly-crystalline or amorphous silicon layer can be deposited. As epitaxially grown silicon has superior optical properties compared to poly-crystalline or amorphous silicon, in figure 5.11 a proposed processing sequence for these grating coupler structures using an epitax-

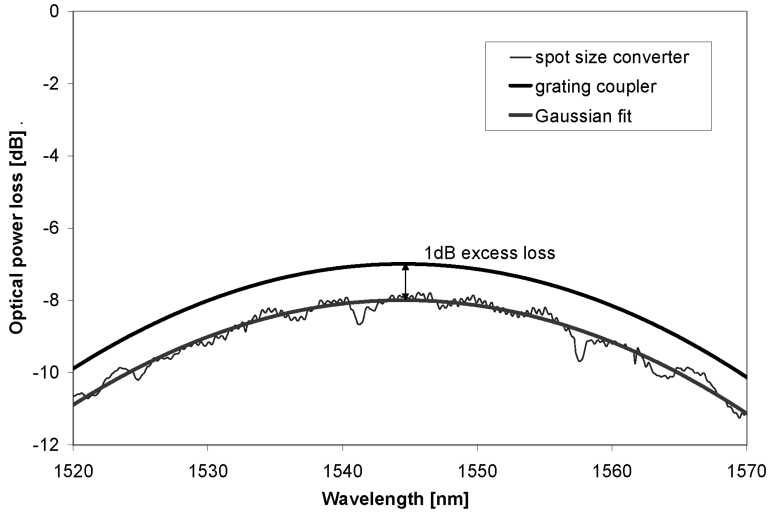


Figure 5.9: Measurement of the coupling efficiency of the inverted adiabatic taper structure

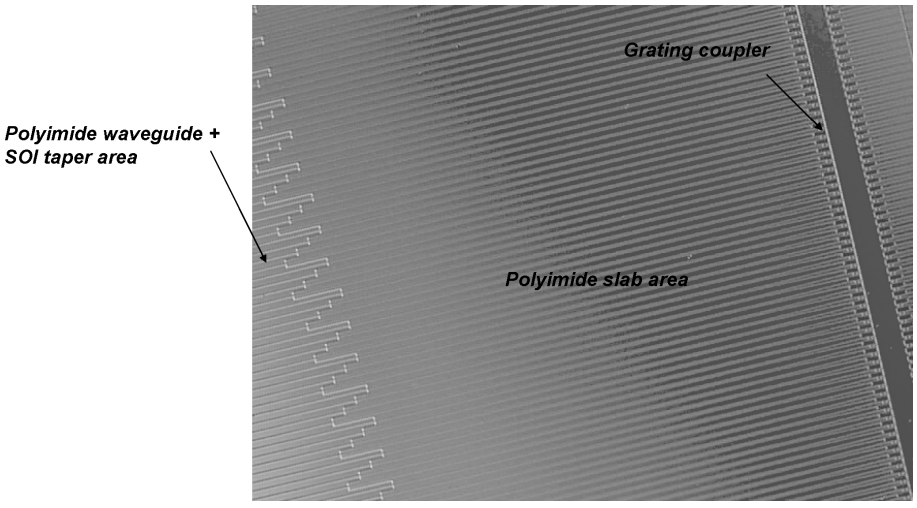


Figure 5.10: Fabricated inverted taper structures

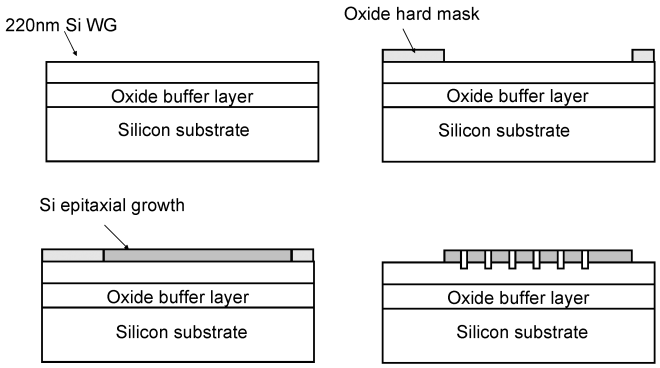


Figure 5.11: Process flow for the fabrication of high-efficiency grating coupler structures using an epitaxially grown silicon mesa

ially grown silicon layer, is shown. After the definition of an opening in an oxide hard mask, silicon is epitaxially grown in the window, after which the grating is etched.

In order to demonstrate the enhancement of the fiber coupling efficiency with in-house available processing tools in this work, a prototype fiber coupler structure was defined, by electron gun evaporation of amorphous silicon on the SOI waveguide substrate and using a lift-off technique. After deposition of the amorphous silicon layer, the grating structure was defined using focused ion beam etching (see section 5.3). Details about the focused ion beam etching process can be found in [166]. The processing sequence for these prototype devices is shown in figure 5.12.

In figure 5.13, an SEM image of a deposited amorphous silicon layer and a focused ion beam fabricated uniform grating structure is shown (a 150nm amorphous silicon layer was deposited). The grating etch depth is 220nm, while the grating period is 610nm and the grating duty cycle 50 percent.

The measured coupling efficiency to a 10 degree off vertical tilted optical fiber is plotted in figure 5.14. The obtained coupling spectrum is compared to the coupler spectrum for a standard grating coupler structure in a 220nm silicon waveguide layer, defined using deep UV lithography and plasma-etching (see section 5.4.2).

The improvement of the fiber coupling efficiency is clear. The shift of the coupling spectrum to shorter wavelengths is presumably related to a difference in refractive index between the amorphous silicon layer and crystalline silicon (which was not taken into account in the design

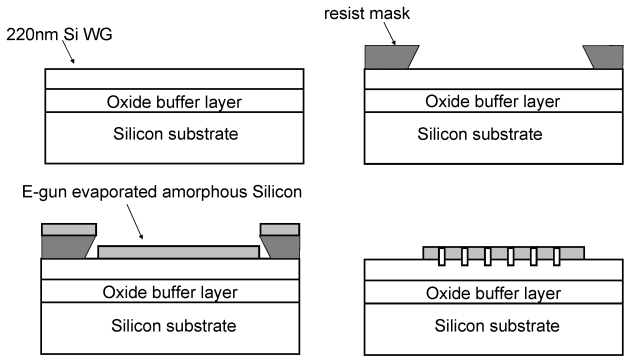


Figure 5.12: Process flow for the demonstration of high-efficiency grating coupler structures with in-house available tools

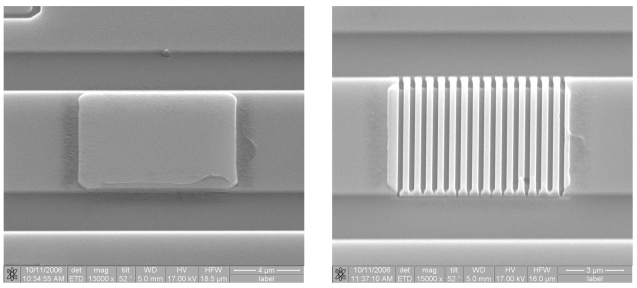


Figure 5.13: SEM view of a deposited 150nm thick amorphous silicon layer on top of a standard SOI waveguide and a focused ion beam fabricated uniform grating structure

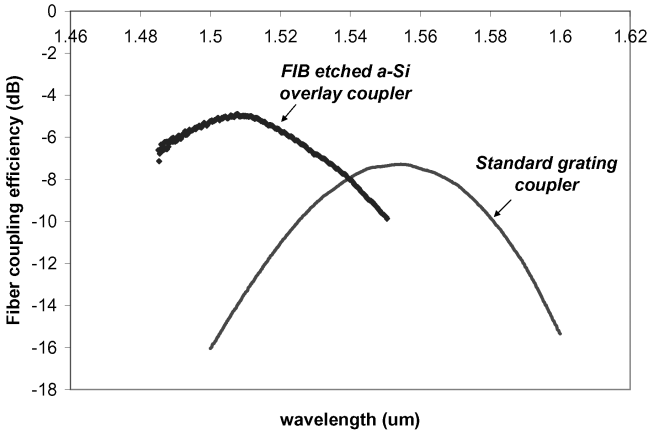


Figure 5.14: Demonstration of the coupling efficiency enhancement by deposition of an amorphous silicon layer

of the structure). While an improvement in fiber coupling efficiency of 2dB was observed in this work, this experimentally obtained efficiency is still substantially lower than the theoretically expected coupling efficiency of -1.7dB (67 percent) as predicted in the previous chapter. This discrepancy is probably related to the large optical absorption of the amorphous silicon, the damage induced into the material by the focused ion beam etching and the incorporation of gallium ions in the silicon host, substantially increasing the optical loss [166].

5.5 InP/InGaAsP waveguide technology

The development of an InP/InGaAsP waveguide etching process to obtain smooth, low loss waveguides and vertically etched facets, consists of optimizing the lithography process, the etching of the hard mask (100nm titanium in our case) and finally the optimization of the InP/InGaAsP etching process. The process development carried out in the context of this PhD, will be discussed in the subsequent sections.

5.5.1 Lithography process

A high resolution MicroChemicals MIR701 photoresist was used to define the patterns. The positive tone photoresist is spin coated at 4000rpm and baked at 100C to obtain a final layer thickness of 0.9μm (the use of

a primer to improve the adhesion of the photoresist to the substrate is optional). After bake, the photoresist is illuminated in a Karl Suss MA-6 mask aligner using 320nm illumination. A resolution of 500nm is obtainable in this way. The exposure dose is about 210mJ/cm^2, depending on the quality of the mask plate (a higher dose is required when the mask plate absorption at the illumination wavelength is higher). After lithography, the photoresist is post-baked at 110C to reduce the vertical striations in the resist pattern, due to the reflections occurring at the hard mask/photoresist interface. After post-bake, the photoresist is developed in an AZ 726 MIF developer for 45 seconds. As it is likely that after development still some photoresist remains in the developed areas, the pattern is exposed to a short oxygen plasma (30 sec. - 50sccm O_2 - 75W RF/25W ICP power, 40mTorr chamber pressure - 60C). A post-bake at 125C is performed to make the photoresist more resistant to the subsequent ICP plasma etching of the hard mask.

5.5.2 Hard mask

The 100nm titanium hard mask is etched in an ICP plasma (2 min. - 50sccm SF_6 / 3sccm O_2 - 100W RF/50W ICP power, 40mTorr chamber pressure - 60C). After the etching of the hard mask, the photoresist is removed prior to InP/InGaAsP etching. This is done by exposing the photoresist to an O_2 plasma (30 min. - 50sccm O_2 - 100W RF/150W ICP power, 40mTorr chamber pressure - 100C). Removing the photoresist using acetone and ultrasonic agitation results in inferior removal compared to the plasma removal.

5.5.3 InP/InGaAsP etching process

The InP/InGaAsP waveguide etching process consists of several cycles of CH_4:H_2 and O_2 plasma. During the CH_4:H_2 plasma step (90 sec. - 15sccm CH_4 / 40sccm H_2 - 240W RF/100W ICP power, 20mTorr chamber pressure - 100C), the InP and InGaAsP material is etched. Besides etching, there is also significant polymer deposition on the surface. A key detriment of polymer deposition during CH_4:H_2 plasma etching is the resulting degradation of the etch anisotropy. Polymers deposit primarily on the inert etch mask materials and minimally on the actively etched InP/InGaAsP surfaces. As the etch rates of InP/InGaAsP are low (typically 20nm-30nm per cycle), the long etch durations can lead to considerable build up of polymers that create an overhang, which eventually induces a positive slope in etched InP/InGaAsP structures.

This polymer film build up can be alleviated by introducing a periodic O_2 cleaning plasma (1 min. - 50sccm O_2 - 100W RF/150W ICP power, 40mTorr chamber pressure - 100C) to remove the deposited polymers. By optimizing the parameters of both plasma processes, smooth sidewalls and nearly vertical facets were obtained in this work.

5.5.4 Hard mask removal

The hard mask is removed by wet chemical etching in a HF:H_2O solution. When polymers are exposed to the etchant, strongly diluted solutions (1 to 4 percent) are needed to avoid delamination or attack of the polymer by the HF.

5.5.5 InP/InGaAsP waveguide losses

The obtained waveguide quality and waveguide losses using the process developed in this work are shown in figure 5.15. Smooth waveguides are obtained with sidewalls that are about 4 degrees off vertical. Low waveguide losses were obtained, however there is a large scattering of the measured data. This scattering is not completely understood, but can be related to the quality of the mask used for defining the waveguide structures.

5.6 Conclusions

In this chapter, the fabrication of SOI structures and InP/InGaAsP waveguide structures was outlined. As a demonstration of the SOI fabrication technology, the fabrication and measurement of SOI inverted taper structures and SOI grating couplers with silicon overlay were discussed. Improved fabrication tolerance and improved fiber coupling efficiency were shown respectively. The InP/InGaAsP etching process was optimized to obtain low loss waveguides (about 1dB/cm at 3μm waveguide width) and close to vertical etched facets (4 degrees off vertical).

The work presented in this chapter has been the subject of 1 publication in international journals (Appendix B.2-4).

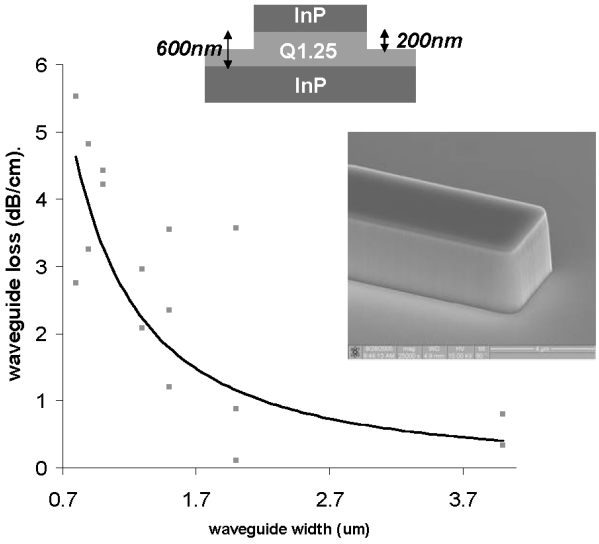


Figure 5.15: InP/InGaAsP waveguide losses at a wavelength of 1.55μm as a function of waveguide width (TE polarization) - the cross-section of the waveguide structures used to characterize the optical losses is shown in the inset

Chapter 6

Bonded light emitting devices

Light my fire
The Doors

In this chapter, we will discuss the fabrication and characterization of DVS-BCB bonded LEDs and laser diodes. The coupling of light from a bonded laser diode to a silicon-on-insulator waveguide will be demonstrated. At the end of this chapter the thermal behavior of the bonded active opto-electronic devices will be analyzed and results on the design and fabrication of a laser diode with an integrated heat sink structure will be presented.

6.1 DVS-BCB bonded LEDs

6.1.1 Fabrication procedure

As a first demonstrator of the viability of the DVS-BCB bonding technique for the fabrication of bonded active opto-electronic components, DVS-BCB bonded LEDs were fabricated in this work. The bonding procedure was based on standard DVS-BCB bonding. On the InP/InGaAsP epitaxial layer structure a TiAu contact was applied first. This layer structure was then bonded upside down onto the silicon transfer substrate using a 7.5μm thick DVS-BCB layer. Next, the original InP substrate and etch stop layer were removed using mechanical grinding and wet chemical etching. After substrate removal, the LED was processed in the bonded epitaxial layer structure by etching through the epitaxial

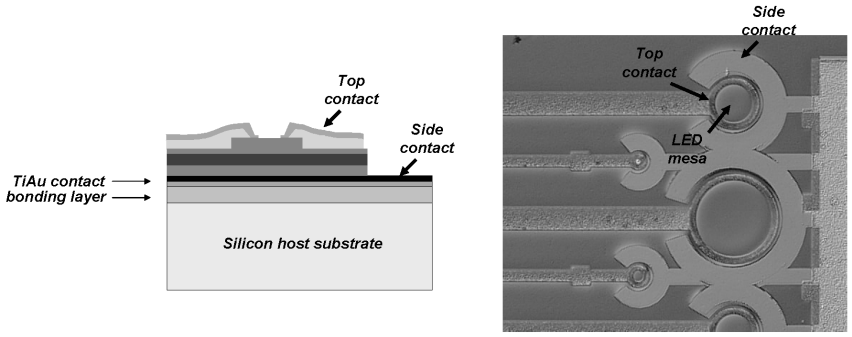


Figure 6.1: Cross-sectional view of DVS-BCB bonded LEDs and a top view of fabricated structures

layer stack to reach the TiAu contact and by defining an LED mesa. A polyimide isolation layer was deposited, through which contact openings were defined, and a top contact was deposited. The top contact in figure 6.1 is a ring contact to allow top side light emission from the LED.

6.1.2 Device characteristics

The power versus current and voltage versus current characteristics of the bonded LEDs are shown in figure 6.2, for LEDs with a mesa radius of 50μm and 100μm respectively. From the power versus current characteristics we can see the influence of the DVS-BCB bonding layer, as the thermal rollover by self-heating of the device occurs at a current of about 80mA for a device with 50μm LED radius (corresponding to a current density of 1kA/cm^2). The low current density for which thermal rollover occurs, limits the maximum output power of the LED. For the case of an LED with a mesa radius of 100μm, this thermal rollover occurs at higher currents due to the reduced current density in the device.

The spectral properties of the light emitted by the bonded LEDs is plotted in figure 6.3. This spectrum deviates from the standard LED emission spectrum of an unbonded LED by the occurrence of a dip in the spectral characteristic. This is related to a microcavity effect [138], as the InP/air and InP/TiAu interface form reflecting interfaces, in between which the light emitting dipoles are located. This leads to a sup-

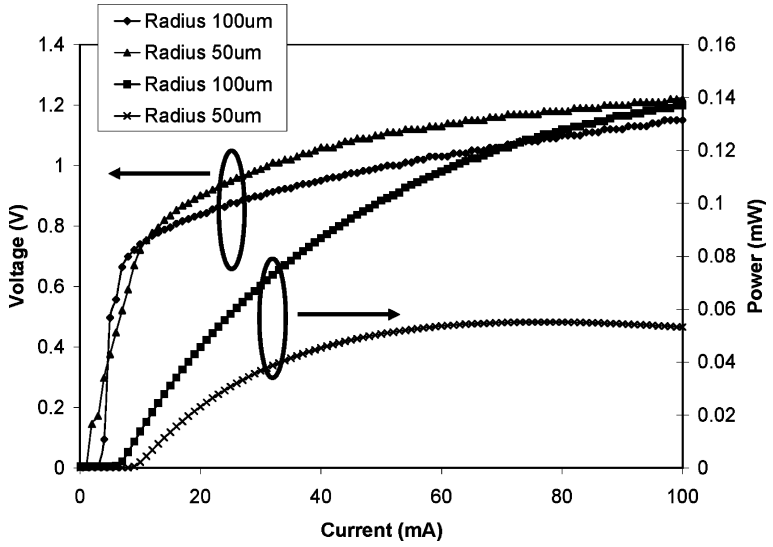


Figure 6.2: PI and VI characteristics of DVS-BCB bonded LEDs

pression and enhancement of certain wavelength components in the emitted spectrum, which explains the dip in the spectrum.

6.2 DVS-BCB bonded laser diodes

6.2.1 DVS-BCB bonded Fabry-Perot laser diodes

Fabrication procedure

Besides light emitting diodes also DVS-BCB bonded laser diodes were fabricated in this work. The fabrication procedure only slightly differs from the case of the bonded light emitting diodes. A standard laser diode epitaxial layer structure was used, on which a uniform TiAu contact was deposited. A GaAs substrate was used as a host substrate, as this allows easier cleaving of the laser diodes compared to a silicon substrate. On the GaAs substrate also a TiAu contact was deposited to be used as a common contact for all bonded devices. The epitaxial layer structure was bonded using standard DVS-BCB bonding and the InP substrate was removed by a combination of mechanical grinding and wet chemical etching. After substrate removal the laser mesa was etched and a n-type contact was defined. This top contact was used as an etch mask to etch through the epitaxial layer structure, to be able to

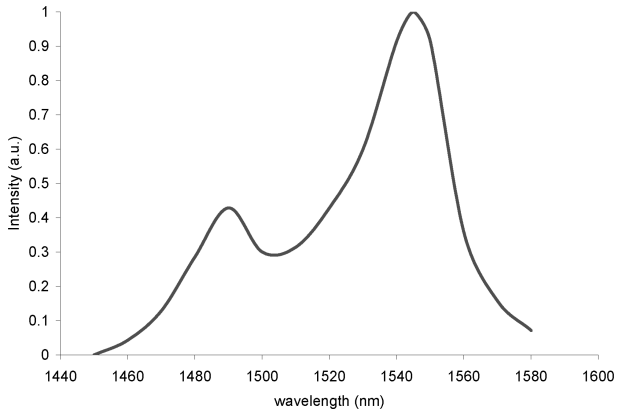


Figure 6.3: Spectral characteristics of the light emitted by a DVS-BCB bonded LED

make an electrical via through the bonding layer. An additional polyimide layer was deposited and opened to form the p-contact and the connection of the n-contact to the GaAs substrate, as can be seen in figure 6.4. An SEM view of a fabricated and cleaved laser diode is shown in figure 6.5.

Device characteristics

Edge emitting lasers (length=1mm, width=7.5μm) were demonstrated in this work, in pulsed regime, with a threshold current density around 2.65kA/cm^2, which is about double the threshold current density of standard lasers that were processed on the same wafer. Figure 6.5 plots the measured peak optical power versus current for different duty cycles. The high thermal resistivity of the bonded device prohibited continuous wave operation (as will be discussed in section 6.5).

To assess the quality and reliability of the DVS-BCB bonding process, in this work damp-heat tests were performed on the bonded laser diodes. The devices were subjected to 85C and 85 percent relative humidity for up to 500 hours. The PI curves and electrical characteristics of the devices were measured before the tests and after 48, 100, 250 and 500 hours of degradation. Figure 6.6 shows the results for a particular laser. The characteristics almost do not degrade and form a clear indication of the DVS-BCB bonding quality.

As the laser diodes are etched through the active layer structure and the laser ridges are typically a few μm wide, these waveguide struc-

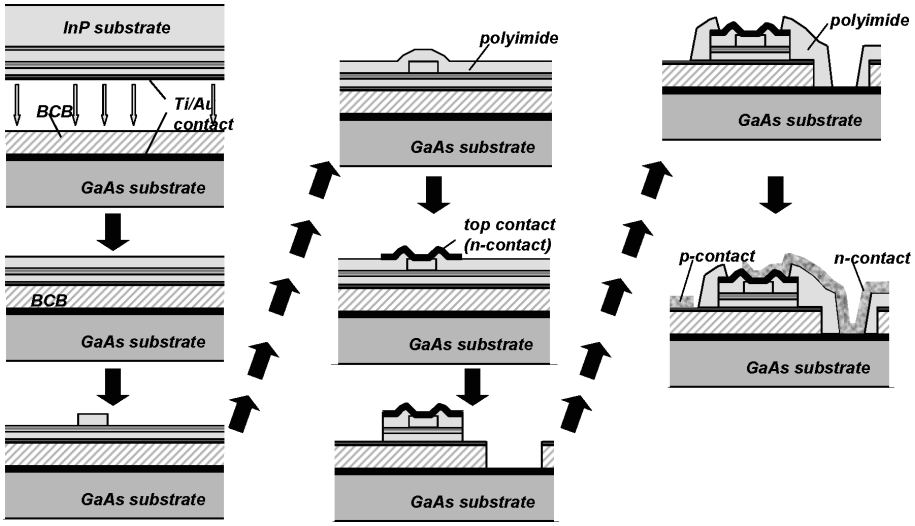


Figure 6.4: Fabrication procedure for DVS-BCB bonded laser diodes

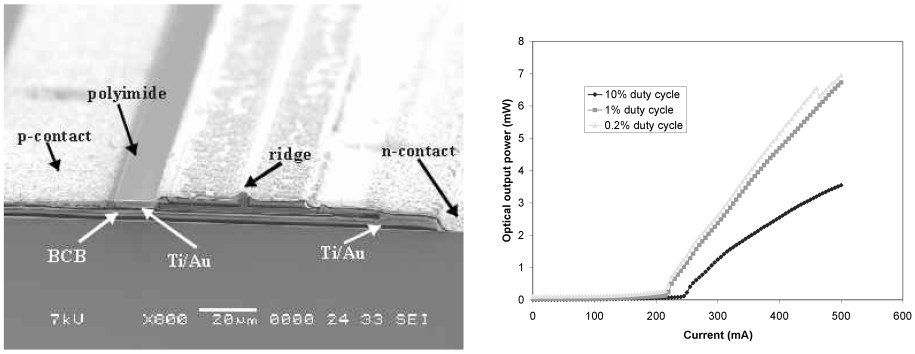


Figure 6.5: SEM view and PI characteristics of DVS-BCB bonded laser diodes

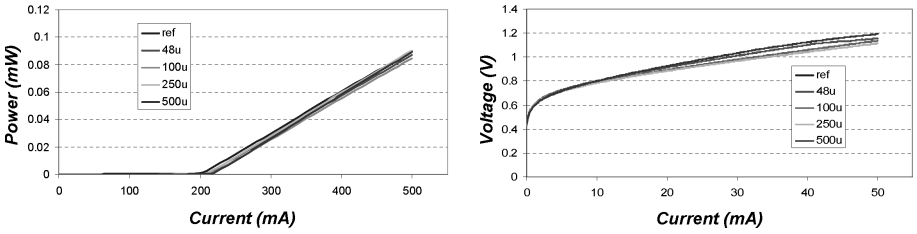


Figure 6.6: PI and VI characteristics of DVS-BCB bonded laser diodes after damp heat testing (85C and 85 percent relative humidity)

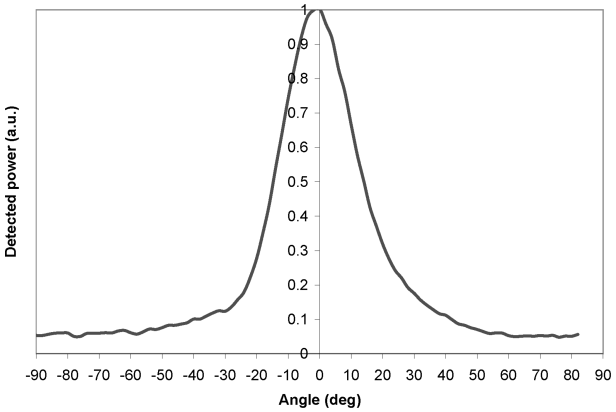


Figure 6.7: In-plane far field pattern of a bonded laser diode

tures are laterally multimode. In order to assess the nature of the lasing mode, a far field pattern of the emitted light in the plane of the layer structure was measured, as shown in figure 6.7. As this is a single-lobed far field pattern, we can conclude that these laser diodes predominantly lase in the fundamental lateral mode, which is important, both for coupling to single-mode optical fiber and for coupling to the fundamental waveguide mode of an underlying passive waveguide.

6.2.2 DVS-BCB bonded DFB laser diodes

Besides the fabrication of bonded Fabry-Perot laser diodes, the viability of fabricating DVS-BCB bonded distributed feedback laser diodes was assessed in this work. This was achieved by defining a first order grating (using interference lithography) in the InP/InGaAsP layer structure to be bonded. After standard DVS-BCB bonding and InP substrate removal, a laser diode was defined by etching through the active core and defining a top and side contact. A schematic view of the processing procedure is shown in figure 6.8. This type of DFB laser diode has the advantage of not requiring any epitaxial overgrowth during the fabrication.

A first batch of laser diodes was characterized in pulsed operation. Threshold current densities were comparable to the Fabry-Perot type bonded laser diodes. Due to a mismatch between the Bragg wavelength of the first order grating and the gain spectrum of the active layer structure, the spectrum of the emitted light consisted of a Bragg peak at 1.55μm in the tail of the gain spectrum and a set of Fabry-Perot

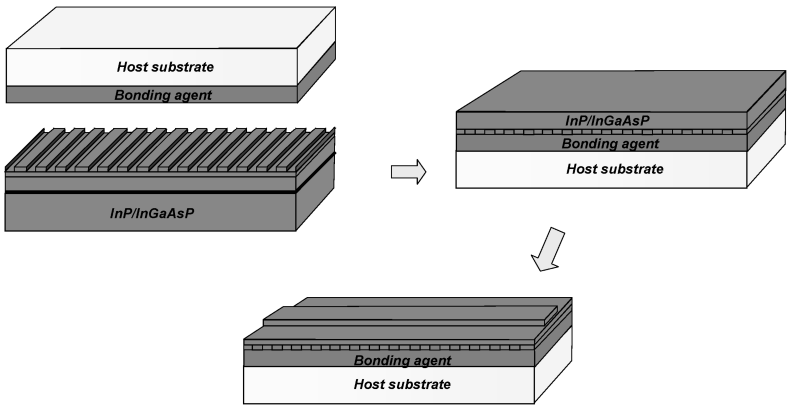


Figure 6.8: Fabrication of a DFB laser diode by means of die-to-wafer bonding

peaks near the maximum of the gain spectrum, as is shown in figure 6.9. This work is described in detail in [167].

6.3 Integrated laser diodes coupled to an SOI waveguide

6.3.1 Device structure

Coupling of light from a DVS-BCB bonded laser diode to an underlying SOI waveguide circuit was discussed in section 4.3.6. The adiabatic taper approach based on butt-coupling to a polymer waveguide and ultra-thin DVS-BCB bonding turned out to be favorable. The structure is depicted in figure 6.10, showing the bonded laser diode, the SOI inverted taper underneath the polyimide waveguide core and the DVS-BCB bonding layer. The laser diode contacts and the DVS-BCB cladding layer of the polymer waveguide were omitted for clarity.

6.3.2 Facet etching technology

A major difference in fabrication compared to the previously presented bonded laser diodes, is the definition of the laser facets. As the laser diode is integrated on an SOI waveguide circuit, laser facets can no longer be cleaved.

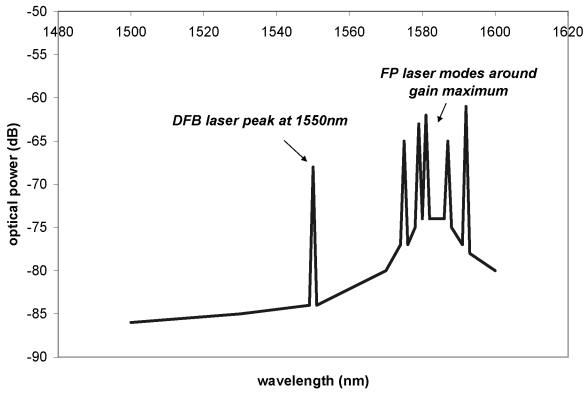


Figure 6.9: Spectrum of the DVS-BCB bonded DFB laser diodes above threshold - due to the mismatch between the Bragg wavelength of the grating and the center of the gain spectrum both Fabry-Perot and distributed feedback laser modes can be seen

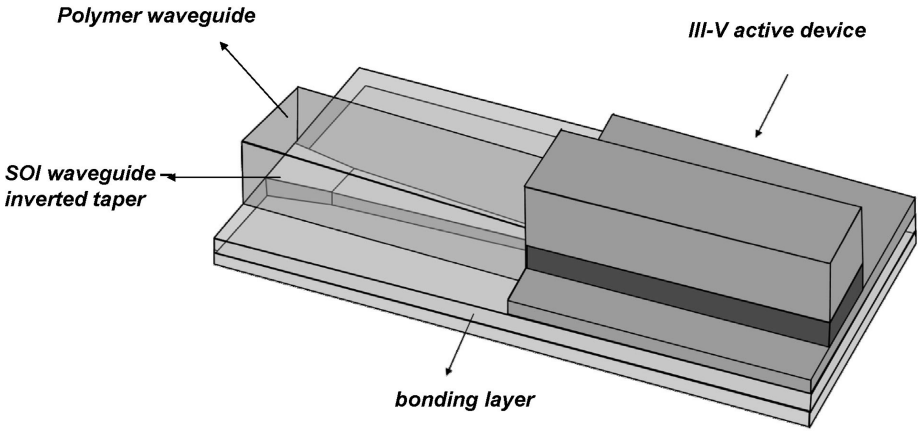


Figure 6.10: Structure of the fabricated device, for coupling of light from a bonded laser diode to an SOI waveguide circuit

Material	Thickness	Doping
InP	600nm	n-type 10^{18}
InGaAsP ($\lambda = 1.25\mu m$)	150nm	n.i.d.
4 x quantum wells ($\lambda = 1.55\mu m$)	2.25nm	n.i.d.
3 x InGaAsP barriers ($\lambda = 1.25\mu m$)	10nm	n.i.d.
InGaAsP ($\lambda = 1.25\mu m$)	150nm	n.i.d.
InP	150nm	n.i.d.
InP	1850nm	p-type $4x10^{17}$
InGaAs	150nm	heavily p-type doped
InP	50nm	not relevant
InGaAs	150nm	not relevant
InP substrate	not relevant	not relevant

Table 6.1: Epitaxial layer structure for the fabrication of bonded laser diodes

In literature, different solutions have been proposed to address this problem. In epitaxial lift-off processes, wedge induced facet cleaving can be used by etching wedges in the epitaxy and transferring the epitaxial layers to a flexible substrate. By bending the flexible substrate, stress is induced in the structure and the epitaxial layers are cleaved. Afterwards, the individual cleaved parts can be bonded on a substrate [90]. As this requires precise alignment in bonding the individual parts, this approach is not used here. Wet etching of laser diode facets on unbonded substrates has been widely used in literature [168, 169, 170]. It was acknowledged however that wet chemical etching shows poor reproducibility, the wall slopes are generally curved and masks are usually significantly undercut. Therefore, this approach was also not adopted. Instead, a dry etching process, as discussed in section 5.5, was used for laser facet definition. Using this process, nearly vertical facets were obtained in a reproducible way, overcoming the disadvantages of the previously discussed methods.

6.3.3 Epitaxial layer structure

The epitaxial layer structure designed for the fabrication of the bonded laser diodes (and for the fabrication of butt-coupled pin-photodetectors as will be discussed in the next chapter) is tabulated in table 6.1. The thickness of the n-type InP cladding layer and the thickness of the separate confinement heterostructure layers was chosen to optimize the overlap of the laser waveguide mode and the polymer waveguide mode.

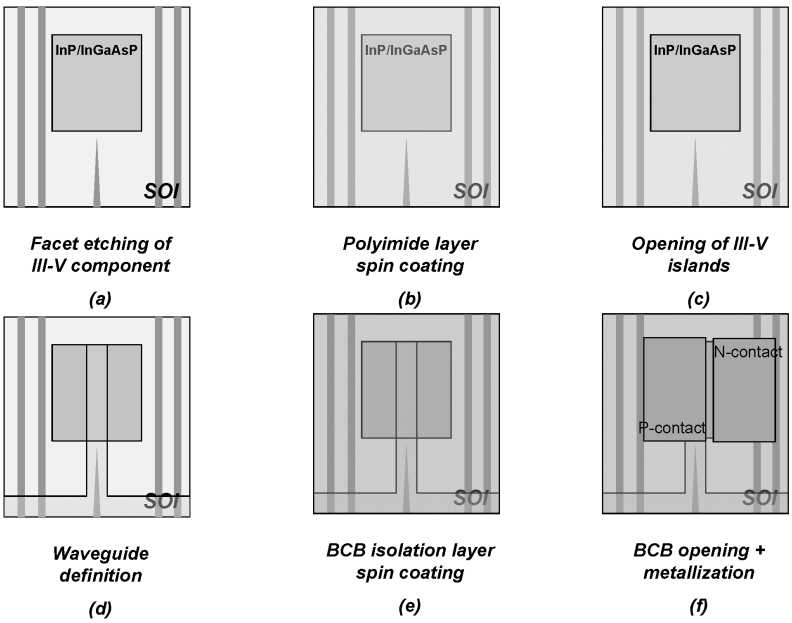


Figure 6.11: Fabrication process of bonded laser diodes on SOI

6.3.4 Fabrication procedure

Silicon-on-insulator waveguides and inverted taper structures were defined using 248nm deep UV lithography and etched through the silicon waveguide layer using a low pressure/high density $Cl_2/O_2/He/Hbr$ plasma, as discussed in section 5.4. The fabrication sequence of the active devices is outlined in figure 6.11.

After transfer of the epitaxial layers to the silicon-on-insulator waveguide substrate using the ultra-thin DVS-BCB bonding process described in section 3.6, the laser cavity facets are defined by dry etching (see section 5.5), using a CH_4:H_2/O_2 plasma (a). A 100nm titanium hard mask is used for the 3.1μm deep etch. After facet etching, a polyimide layer was spin coated over the surface (b) and after curing at 300C for 1 hour it was again removed on top of the InP/InGaAsP material, using a photoresist mask (c). This defines the polymer waveguide layer for the inverse adiabatic taper structure. In a next step, the laser diode waveguide was defined together with the polymer waveguide structure using a CH_4:H_2/O_2 plasma, such that there is no misalign-

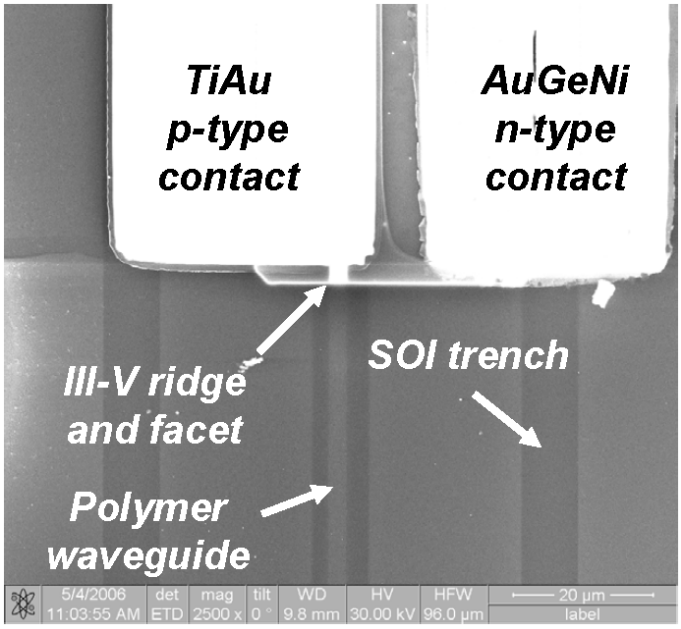


Figure 6.12: Top view of the fabricated laser diodes coupled to the SOI waveguide circuit

ment at the polymer/III-V interface (d). The polyimide waveguide layer is predominantly etched during the O_2 cleaning plasma. The laser ridges were 2.8μm wide. III-V waveguides were etched through the active layer, to be able to access the n-type contact layer. The polyimide waveguide layer was completely etched through. A DVS-BCB isolation layer was spin coated (which also serves as a cladding layer for the polyimide waveguide) (e) and openings are made to define the p-type TiAu contact and the n-type AuGeNi contact, which where subjected to a rapid thermal annealing at 400C (f). All alignment was done with respect to the underlying SOI features. A top view of a fabricated structure is shown in figure 6.12, showing the InP/InGaAsP component butt-coupled to the polymer waveguide. The SOI inverted taper structure is not visible, as it is buried underneath the polymer waveguide.

A focused ion beam cross-section of the III-V/polymer interface, shown in figure 6.13, reveals the quality of the laser facets and the definition of the polymer waveguide layer next to the laser diode. The laser facet angle of 86 degrees is sufficiently steep to obtain high reflection

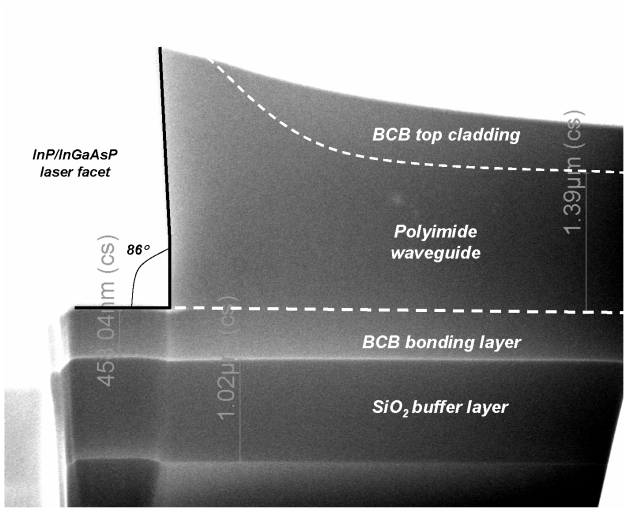


Figure 6.13: Focused ion beam cross-section of the polymer/III-V interface

into the laser mode and high transmission to the polymer waveguide mode, as was calculated in figure 4.27. The DVS-BCB bonding layer is 460nm thick in the SOI waveguide trenches (240nm above the SOI waveguide).

6.3.5 Device characteristics

Laser emission from bonded devices was observed in this work, in pulsed operation, as is shown in figure 6.14. Light was collected from the SOI waveguide using a lensed fiber. A 10 μs long square wave current pulse with a 1 percent duty cycle was applied to drive the laser. To assess the optical power in the SOI waveguide, the theoretical coupling efficiency between the lensed fiber and SOI waveguide was assumed. The threshold current density is relatively high (10.4kA/cm^2 for a 500 μm long device). This high threshold current density might be related to the roughness of the etched waveguides and can be reduced by further optimization of the etching process. Another reason could be that the rapid thermal anneal at 400C might have created a substantial density of threading dislocations in the active region (as discussed in section 3.9.2). No continuous wave operation was obtained, due to the high power dissipation of the bonded device. This problem can be cir-

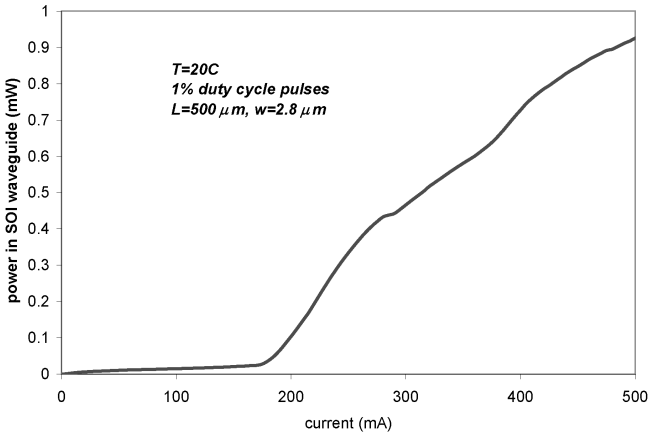


Figure 6.14: Power in the SOI waveguide versus laser diode current under pulsed operation

cumvented however by integrating a heat sink structure on the laser diode structure, as will be discussed in section 6.5.5, and by improving the device fabrication process. This is however outside the scope of this work.

6.4 Integrated microlasers

The microlasers discussed in section 4.3.8 are studied in the PhD of J. Van Campenhout. Three types of lasers are studied: vertically emitting photonic crystal lasers, DBR microlasers and microdisk lasers. In the latter case, the electrical injection is based on the double side contacting structure as discussed in figure 4.18. Whispering gallery mode lasing and coupling of light to an SOI waveguide was observed.

6.5 Thermal behavior of bonded devices

6.5.1 Simulation tools

In order to study the thermal behavior of a bonded active opto-electronic component, a two-dimensional finite element solver was used (DESSIS from Synopsis) [142], to solve the governing thermo-electrical-optical equations. For pure thermal calculations of a cross-section of a device, the Fourier equation

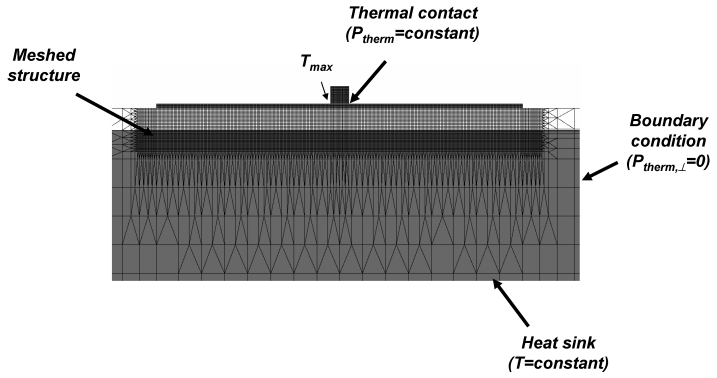


Figure 6.15: Overview of the thermal analysis of an opto-electronic device

$$\begin{aligned} \mathbf{q_{heat}} &= -\mathbf{k}\nabla\mathbf{T} \\ \nabla \cdot \mathbf{q_{heat}} &= \mathbf{0} \end{aligned} \tag{6.1}$$

and the appropriate boundary conditions at heat sinks (Dirichlet condition of constant temperature), the edges of the structure (Neumann condition, being $\frac{\delta T}{\partial n} = 0$ with n the surface normal direction) and at the heat source ($k\frac{\delta T}{\partial n} = -P_{therm}$ with P_{therm} the dissipated heat per unit area), need to be solved. The thermal resistivity of the device is then calculated as

$$R_{th} = \frac{T_{\max}}{P_{therm}}[Kcm^2/W] \tag{6.2}$$

as shown in figure 6.15. This approach will be used in the following sections to determine the thermal resistivity of a bonded opto-electronic device, as this thermal resistivity will influence the device performance.

The thermal conductivity of various materials used in the simulations is shown in table 6.2. Convection and radiation heat transport were not considered in this work.

6.5.2 Influence of self-heating on device characteristics

When the temperature of an active opto-electronic device changes, various parameters are affected. When considering the influence on the light power versus current characteristic, there are only a few parameters dominantly affecting these characteristics. In the case of an

Material	Thermal conductivity (W/mK)
SiO_2	1.24
Silicon	130
DVS-BCB	0.3
Polyimide	0.3
InP	68
InGaAs	10
Au	320
Ti	22

Table 6.2: Thermal conductivity of various materials

LED, the optical power versus current characteristic is mainly affected by the temperature dependence of the bimolecular recombination constant [171]

$$B(T) = B_{300K}\frac{300}{T} \tag{6.3}$$

and the temperature dependence of the Auger recombination constant [171]

$$C(T) = C_{300K}\exp(-\frac{E_A}{k_B}(\frac{1}{T} - \frac{1}{300})) \tag{6.4}$$

with k_B the Boltzmann constant and E_A a material dependent activation energy (about 60meV for InGaAsP active layers). In the case of a laser diode, there is the additional influence of the temperature dependence of the gain. Higher temperature causes a wider Fermi spreading of carriers, lowering the optical gain. A linear drop of the gain as a function of temperature is assumed.

$$g(T) = g(300K)(1 - \left.\frac{dg}{dT}\right|_{300K}\frac{(T-300)}{g(300K)}) \tag{6.5}$$

Besides these dependencies, in literature, also the temperature dependence of the intervalence band absorption (IVBA), thermionic carrier emission from the active region, lateral carrier spreading and Shockley-Read-Hall recombination are considered. In [172] it was argued however that the influence of these mechanisms is small, except at very high temperatures (above 100C), where the vertical leakage of carriers over the heterostructure becomes the dominant mechanism.

The thermal red-shift of the laser gain peak and LED emission spectrum is not considered here in simulating the influence of temperature on the optical power versus current characteristic. While this is a good approximation for LEDs and Fabry-Perot laser diodes, in the case of

DFB-type and DBR-type laser diodes where the lasing wavelength is determined by the period of an etched grating, this effect should be taken into account.

Based on the temperature dependencies described above, a model was derived to assess the influence of the thermal resistivity of a bonded active opto-electronic device on the power versus current characteristics.

In the case of an LED the temperature increase due to injection of current into a circularly shaped LED mesa (diameter D), is given by

$$\Delta T = R_{th} J (V_{th} + \rho J) \tag{6.6}$$

with J the current density through the device active layer

$$J = \frac{4I}{\pi D^2} \tag{6.7}$$

and ρ the diode electrical resistivity. The temperature dependence of the threshold voltage V_{th} and ρ is not taken into account. In this equation, it is assumed that all electrical power is dissipated in the device, neglecting the radiated optical power.

The carrier concentration in the active layer is then given by

$$\eta_i J = qd(AN + B(T)N^2 + C(T)N^3) \tag{6.8}$$

with d the thickness of the active layer and η_i the injection efficiency. The optical power leaving the device is given by

$$P = \frac{h\nu}{q} B(T) N^2 \frac{\pi D^2}{4} \eta_{extr} \tag{6.9}$$

with η_{extr} the extraction efficiency from the LED active layer and $h\nu$ the photon energy (about 0.8eV for 1.55μm emitting LEDs).

Based on the voltage versus current relation measured in figure 6.2 and using a thermal resistivity of $R_{th} = 0.25 \frac{Kcm^2}{W}$, corresponding to a DVS-BCB bonding layer thickness of $7.5\mu m$, the power versus current characteristics of an LED with 50μm mesa radius and 100μm mesa radius were simulated and are shown in figure 6.16. A good correspondence between simulations and measured power versus current characteristics is obtained (see figure 6.2). For a $50\mu m$ radius LED mesa, thermal rollover occurs around 80mA injection current. For a $100\mu m$ radius LED thermal rollover occurs at higher currents, due to the lower current density in the latter device compared to the $50\mu m$ radius LED.

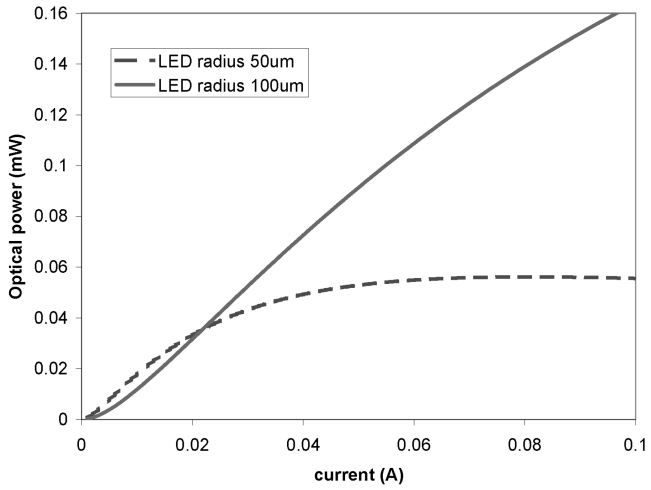


Figure 6.16: Thermal rollover in LED light emitting characteristics

For the simulation of the thermal behavior of a bonded laser diode, a rate equation model was developed to simulate the power versus current characteristics of the device.

Again, the temperature increase due to the power dissipated in the device is calculated by equation 6.6. The differential equation describing the time evolution of the total amount of photons S inside the cavity is given by

$$\frac{dS}{dt} - (G - L)S = \beta T_{sp} \tag{6.10}$$

In 6.10, G is the relative increase in amount of photons in the cavity per time unit and is given by $G = \Gamma v_g g(T)$, with Γ the confinement factor of the laser mode in the active region, v_g the group velocity of the laser mode and $g(T)$ the temperature dependent material gain of the active layer. In equation 6.10, the loss of photons per time unit L is given by $L = v_g(\alpha + \frac{1}{L_{cav}} \ln(\frac{1}{R}))$, with α the internal loss per unit length of the cavity and $\frac{1}{L_{cav}} \ln(\frac{1}{R})$ the distributed loss due to the facet reflectivity R, with L_{cav} the length of the laser cavity (a symmetric Fabry-Perot cavity is assumed). The right hand side of equation 6.10 is due to the coupling of spontaneous emission of light in the laser mode. β is the spontaneous emission factor and $T_{sp} = B(T)N^2V_{act}$ is the amount of

spontaneous emitted photons in the cavity per time unit (active volume V_{act}).

In steady-state, the number of photons in the cavity can be written as

$$S = \frac{\beta B(T) N^2 V_{act}}{v_g(\alpha + \frac{1}{L_{cav}} \ln(\frac{1}{R})) - \Gamma v_g g(T)} \tag{6.11}$$

To calculate the carrier concentration N in the laser diode, the following equation has to be solved

$$\frac{\eta_i I}{q V_{act}} = AN + B(T)N^2 + C(T)N^3 + \frac{\Gamma v_g g(T) S}{V_{act}} \tag{6.12}$$

in which the total number of injected carriers, per unit volume per time unit, equals the total number of recombined carriers (by spontaneous or stimulated recombination), per unit volume and per time unit.

The output power of the laser diode at one facet is given by

$$P_{out} = \frac{1}{2} h\nu \alpha_m v_g S \tag{6.13}$$

with $\alpha_m = \frac{1}{L_{cav}} ln(\frac{1}{R})$ the distributed mirror loss.

Using this model, the influence of the thermal resistivity of the bonded device characteristics can be calculated. While applicable for continuous wave light emission, the equations described above can be adapted to describe pulsed operation of the laser diode. Assuming that the pulse period is much shorter than the thermal time constant of the laser diode and the pulse width is large compared to the time constants involved in the laser dynamics, the above equations can still be used to calculate the peak optical power generated by the laser diode, by replacing equation 6.6 by

$$\Delta T = R_{th} J (V_{th} + \rho J) f_{DC} \tag{6.14}$$

with f_{DC} the duty cycle of the pulsed current waveform and J the peak current density through the device. For the case of the DVS-BCB bonded laser diodes, which were described in section 6.2, the simulated influence of the duty cycle on the peak optical power is plotted in figure 6.17. Due to the thick DVS-BCB bonding layer, no continuous wave operation can be achieved. Pulsed operation with sufficiently small duty cycles can be obtained, as shown in figure 6.17. The parameters used in the equations were tweaked to fit the measured pulsed power

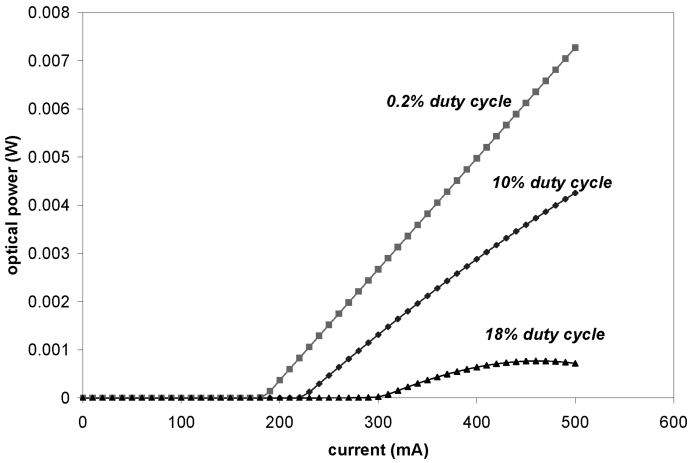


Figure 6.17: Thermal rollover in laser emission characteristics

versus current characteristics from figure 6.5. As can be seen, due to the temperature increase of the laser diode resulting from increasing the duty cycle, the laser diode threshold current increases, the slope efficiency of the device decreases and at sufficiently high current levels thermal rollover can be observed. For duty cycles larger than 20 percent no more laser action could be observed, due to the thermal runaway of the device. Therefore, a sufficiently low thermal resistivity is required to achieve continuous wave lasing.

From this type of simulations and fitting of real device characteristics to the model, one can predict the influence of a further reduction in thermal resistivity on the power versus current characteristics.

6.5.3 Influence of ambient temperature

Besides the self-heating of the device, the ambient temperature plays an additional role. While in the previous section the ambient temperature was assumed to be room temperature, when integrated for example on a CMOS substrate, this is no longer the case, as large amounts of heat can be dissipated in the electronic circuit. The influence of this temperature increase on the power versus current characteristic of a laser diode, is an increase of the laser diode threshold current, a reduction of the slope efficiency and the occurrence of thermal rollover at lower current injection levels. Also for the LED characteristics, external efficiency is decreasing, while thermal rollover again occurs at lower current injec-

tion levels. Besides the changes in power versus current characteristics, also the emission wavelength changes with temperature.

6.5.4 Design of a heat sink structure

From the previous discussion, it is clear that a low thermal resistivity of a bonded active opto-electronic device is crucial for its continuous wave operation. In this section we will discuss how we can decrease the thermal resistivity of the bonded device by modifying the layout of the laser diode.

A first approach is of course to change the bonding material. However, being restricted to optically transparent materials (thereby excluding metallic bonding layers with high thermal conductivity), typically only a factor of 2 can be gained (for example by going to spin-on glass layers). Another approach to alleviate the thermal problem is mounting the bonded active device p-side down onto a heat sink, using a metallic bonding approach. This would circumvent the above mentioned problems, but leads to an increased fabrication complexity. Therefore, a better approach is to adapt the parameters of the design in order to obtain a low thermal resistivity.

A basic parameter to change is the thickness of the bonding layer. In figure 6.18 and 6.19 the influence of the bonding layer thickness on the thermal resistivity of a 3μm wide laser diode, with a n-type InP undercladding of 600nm and a ridge height of 2μm, is plotted. The laser diode is assumed to be bonded onto a silicon-on-insulator wafer with a buried oxide layer thickness of 1μm and a silicon core layer of 220nm and onto a silicon-on-insulator wafer with the silicon core layer removed ("oxidized silicon wafer") respectively. For comparison, the thermal resistivity of an unbonded laser diode on a 150μm thick InP substrate ($1Kcm^2/kW$) is also shown.

Thinner bonding layers obviously lead to lower thermal resistivity. As the devices need to be bonded on processed silicon-on-insulator waveguide wafers, the lowest technologically obtainable spacing between the top of the silicon waveguide and the bottom of the InP/InGaAsP epitaxial layer stack is about 300nm with our process. In case the silicon core layer underneath the laser diode is etched away, this bonding layer thickness increases to 520nm. This results in a thermal resistivity of $2.9Kcm^2/kW$ and $3.6Kcm^2/kW$ respectively. So, although a thinner bonding layer reduces the thermal resistivity of the bonded device, the limitation in achievable bonding layer thickness still implies

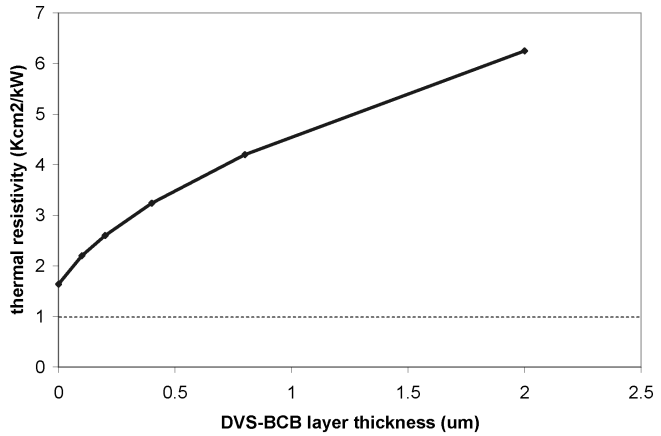


Figure 6.18: Thermal resistivity of a laser diode bonded onto a silicon-on-insulator wafer

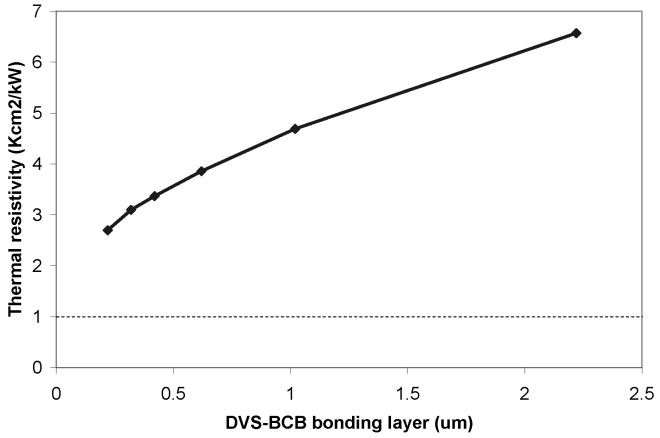


Figure 6.19: Thermal resistivity of a laser diode bonded onto an oxidized silicon wafer

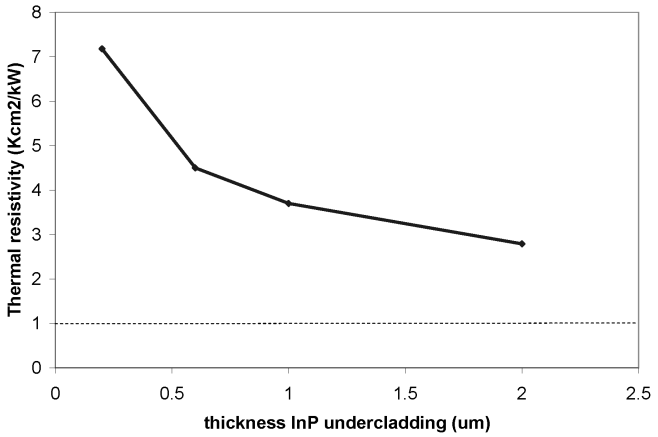


Figure 6.20: Influence of the InP undercladding thickness on the thermal resistivity of a bonded laser diode

a three times higher thermal resistivity compared to an unbonded device. While continuous wave operation could be obtained for high quality factor and low threshold current bonded laser diodes, this will no longer be the case when thicker bonding layers are required by the application. Therefore, we will discuss the use of the InP undercladding as a heat spreading layer and the use of the device contacts as a heat sink through the bonding layer.

The use of the InP undercladding as a heat spreading layer will have most effect when a thick DVS-BCB bonding layer is used. The influence of the thickness of the InP undercladding layer on the thermal resistivity of a 3μm wide laser diode bonded on a silicon-on-insulator wafer using a 1μm thick DVS-BCB bonding layer is plotted in figure 6.20.

From this simulation it can be seen that a 2μm thick InP cladding layer is needed to obtain a thermal resistivity comparable to the ultra-thin DVS-BCB bonding. The large increase in thermal resistivity with decreasing cladding layer thickness is a clear signature of the heat spreading action of this layer. A drawback of this approach is however that, as a thick InP cladding layer is required to obtain a significant effect, the optical coupling between the InP/InGaAsP waveguide layer and the SOI waveguide layer becomes more difficult.

Another approach to reduce the thermal resistivity of a bonded laser diode is to use the device contacts to fabricate a thermal via through the bonding layer. Both top and side contact can be used for this purpose.

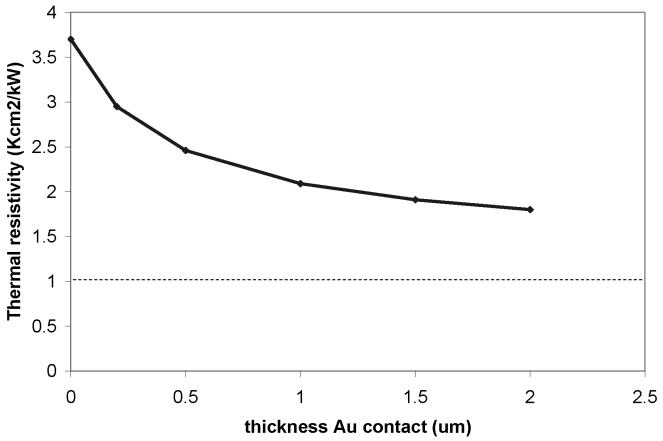


Figure 6.21: Influence of the thickness of the gold top contact thermal via on the thermal resistivity of the bonded laser diode

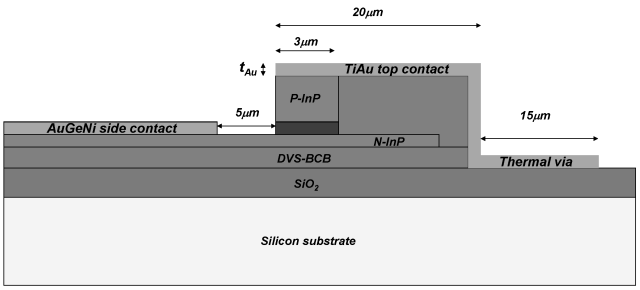


Figure 6.22: Simulated bonded laser structure

In figure 6.21, the influence of the thickness of the top gold contact on the thermal resistivity of the device shown in figure 6.22 is depicted.

The laser diode is bonded using 500nm DVS-BCB on a silicon wafer with a 1μm SiO_2 layer on top. The InP undercladding and top cladding layer are 0.6μm and 2μm thick respectively. From this simulation we can conclude that by using a 2μm thick gold top contact that is connected to the carrier substrate through a via in the DVS-BCB layer, we can decrease the thermal resistivity to about $1.8Kcm^2/kW$. Extending the via through the oxide layer and using a thick gold side contact only has a minor influence on the thermal resistivity. This is due to the higher thermal conductivity of the SiO_2 layer and the high thermal

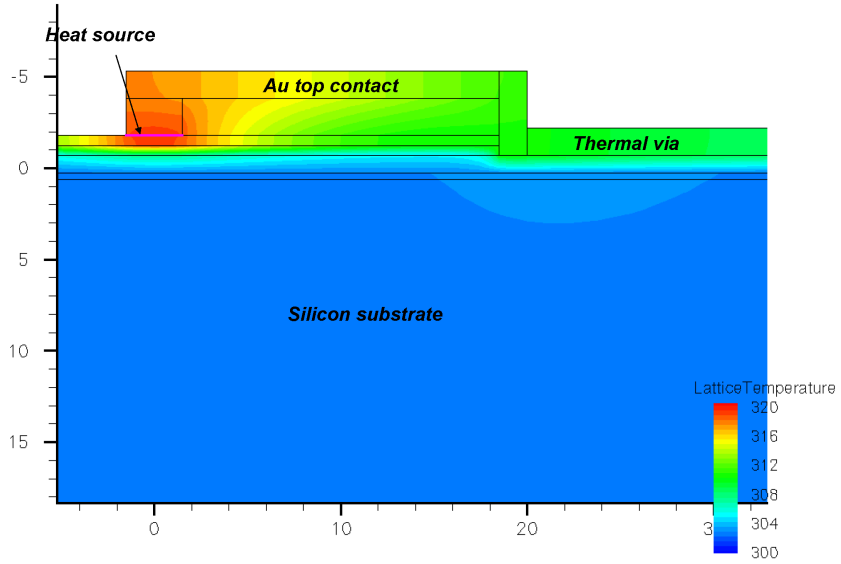


Figure 6.23: Temperature profile of an active laser diode with integrated heat sink

resistance between the heat source and the side contact. The temperature distribution in a bonded laser diode with an incorporated heat sink structure is shown in figure 6.23. Compared to a device without an incorporated thermal via, a temperature reduction by a factor of 2 is obtained.

6.5.5 DVS-BCB bonded laser diodes with integrated heat sink

As the high thermal resistivity of the previously presented bonded laser diodes was too high to achieve continuous wave lasing, a dedicated heat sink structure was designed in the previous section. The experimental realization of these bonded laser diodes with an integrated heat sink structure is shown in figure 6.24. An InP/InGaAsP epitaxial layer stack was bonded onto a GaAs carrier using a 1μm thick DVS-BCB bonding layer. After substrate removal, a 9μm wide laser diode was processed in the bonded epitaxial stack. The plated gold top and side contact (2.5μm thick) are connected to the GaAs substrate and function as a heat sink. A thin oxide layer is deposited below the n-type contact, in order to prevent a parallel current path between both contacts

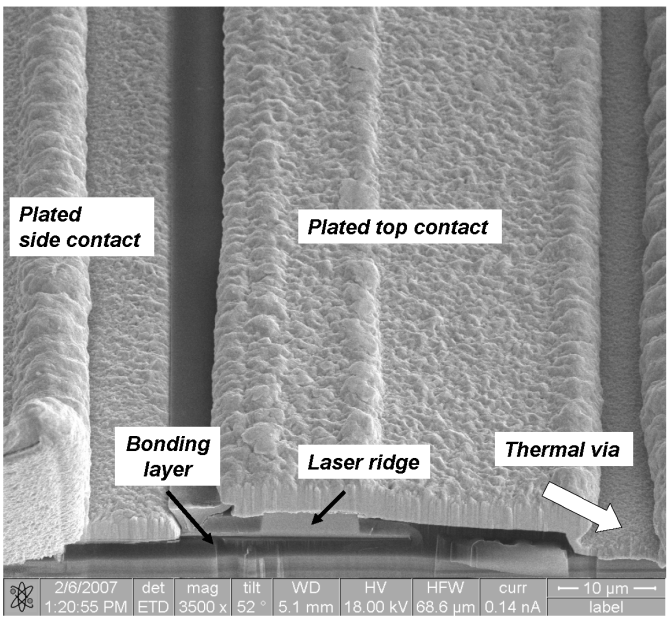


Figure 6.24: SEM picture of the fabricated bonded laser diodes with integrated heat sink structure

through the GaAs substrate. 700μm long laser cavities were defined by cleaving the GaAs substrate.

The influence of the duty cycle of the square wave current pulse applied to drive the laser diode on the PI curve of the bonded laser diode is shown in figure 6.25. Although degradation of the characteristics due to the self-heating of the device can be seen, continuous wave lasing was obtained. While improved performance could be expected by using narrower laser diode stripes (due to the lower thermal resistivity for narrower stripes), no lasing could be observed in 3μm wide laser diodes, even under pulsed operation. This is probably due to the inferior etching process used to fabricate this batch of bonded laser diodes. The lower thermal resistivity for narrower laser stripes can be understood from the fact that, as nearly all heat has to be laterally sunk through the gold plated top contact, this thermal resistivity scales with the width of the laser stripe.

Although the layout of the laser diodes presented here strongly resembles the laser diodes discussed in section 6.2, no continuous wave lasing was obtained in the latter case, as the thickness of the gold top

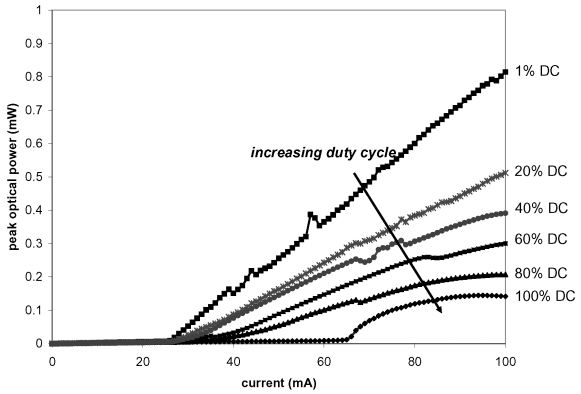


Figure 6.25: Influence of the duty cycle of the square wave current pulse applied to drive the laser diode on its PI characteristic

contact and distance of the thermal via from the laser stripe provided an insufficient reduction in thermal resistivity.

6.6 Conclusions

In this chapter several types of light emitting devices were fabricated and characterized. Both bonded light emitting diodes and bonded laser diodes were studied. An important issue in the design of bonded laser diodes is the thermal behavior of the bonded device. A thermal heat sink structure was designed and demonstrated to overcome the large thermal resistivity of the bonded devices. For the first time, the coupling of light from a bonded laser diode to an underlying passive waveguide circuit was demonstrated.

The work presented in this chapter has been the subject of 2 publication in international journals (Appendix B.2-6 and B.2-9).

Chapter 7

Bonded photodetectors

This is the end
The Doors

In this chapter, we will present the results on the fabrication and characterization of waveguide-coupled bonded InP/InGaAsP photodetectors. Three types of photodetectors will be discussed: a butt-coupled pin-type photodetector, a normal incidence operating pin-photodetector and a new type of waveguide-coupled metal-semiconductor-metal (MSM) photodetector.

7.1 Waveguide-coupled bonded pin-photodetectors

7.1.1 Butt-coupled pin-photodetector

Device layout

The device layout for the butt-coupled pin-photodetectors is identical to the case of the bonded laser diodes discussed in section 6.3. The only difference lies in the dimensions of the structure. As nearly all light is absorbed after a photodetector length of 50μm, the photodetector structure will be more compact than the laser diode. For a good understanding, the structure is again depicted in figure 7.1. The fabrication procedure is identical to that of the bonded laser diodes discussed in section 6.3.

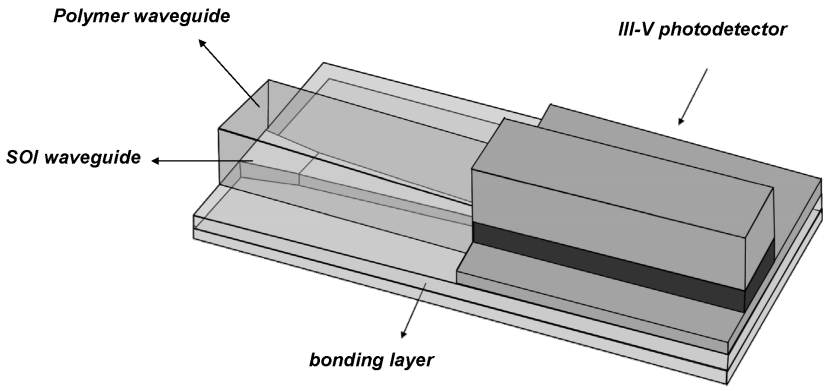


Figure 7.1: Butt-coupled photodetector layout

Device characteristics

The responsivity of photodetectors was measured by injecting light into the SOI waveguide using a lensed fiber. The theoretical coupling efficiency from lensed fiber to SOI waveguide was used to estimate the optical power travelling in the waveguide, therefore resulting in a lower boundary for the responsivity of the photodetector. A responsivity of 0.23A/W was obtained at a wavelength of 1555nm. The current versus voltage curves with and without illumination are shown in figure 7.2 (device length of 50 μm) for an estimated 95 μW waveguide power. The dark current of the device is about 50nA at 2V reverse bias.

7.1.2 Normal incidence bonded pin-photodetector

Device layout

In section 4.5.1, the use of a grating coupler was proposed to efficiently couple light from an SOI waveguide to a standard DVS-BCB bonded normal incidence photodetector. The principle of the coupling structure is shown in figure 7.3. While three types of grating couplers were presented in chapter 4, only the basic coupling scheme will be demonstrated here.

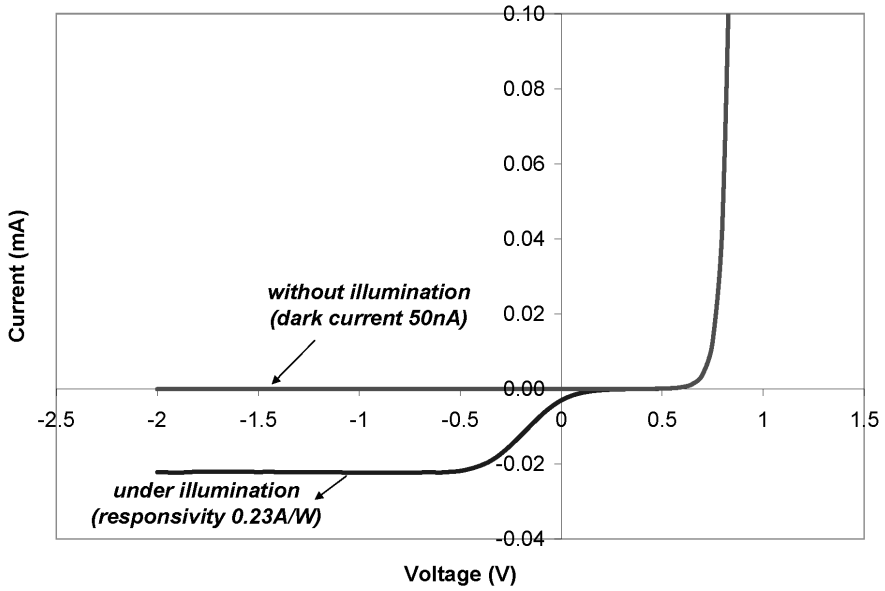


Figure 7.2: IV characteristic of a bonded photodetector

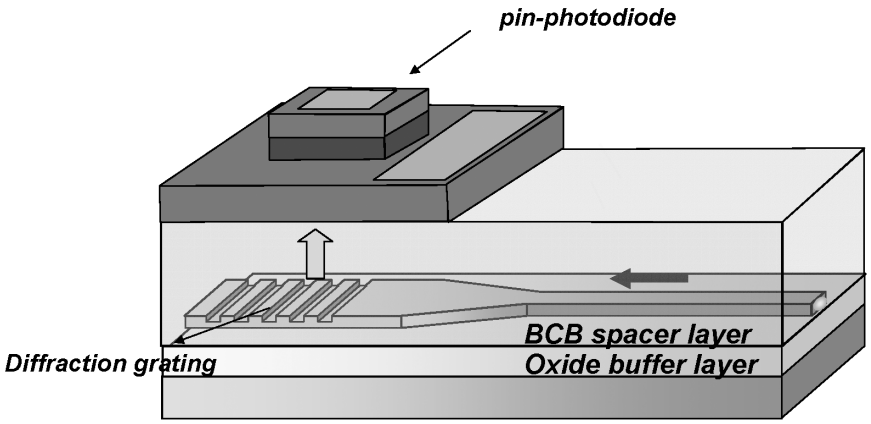


Figure 7.3: Grating-based photodetector layout

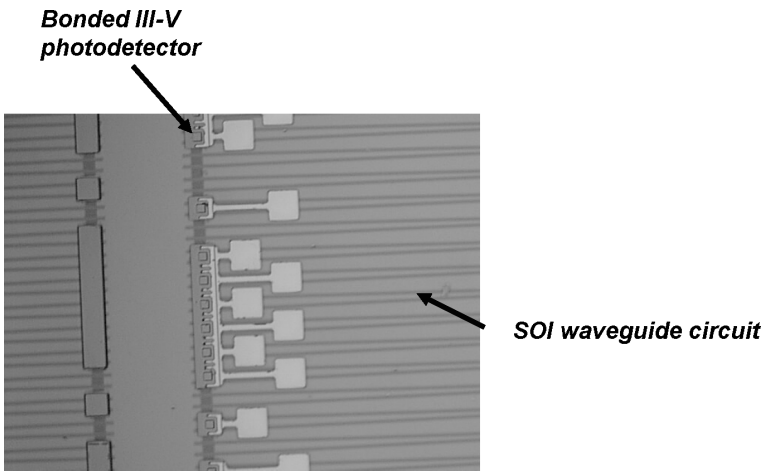


Figure 7.4: Top view of the fabricated grating-based photodetectors on top of the SOI waveguide circuit (prior to top contact definition)

Fabrication procedure

Silicon-on-insulator waveguides and grating structures were defined using 248nm deep UV lithography and etched using a low pressure/high density Cl_2/O_2/He/Hbr plasma as discussed in section 5.4. The grating coupler period is 610nm, has a duty cycle of 50 percent and is etched 50nm deep.

The epitaxial layer structure, consisting of an n-doped 1μm thick InP bottom cladding layer, a 120nm thick InGaAsP absorption layer (1.55 μm band gap wavelength) and a 1.8μm p-doped InP top cladding, was transferred to the SOI waveguide circuit using standard DVS-BCB bonding with a 3μm thick DVS-BCB layer, after which the InP substrate was removed by mechanical grinding and wet chemical etching.

The detector mesa was etched through the absorbing layer and a AuGeNi n-type contact was deposited. After applying a DVS-BCB isolation layer, top windows were opened and a TiAu p-type contact is deposited and annealed. A top view of the fabricated devices, before top contact definition, is shown in figure 7.4.

Device characteristics

The responsivity of the photodetectors was measured to be 0.022A/W referenced to the SOI waveguide power. This low responsivity is due to the non-optimized absorption layer thickness, which was only 120nm

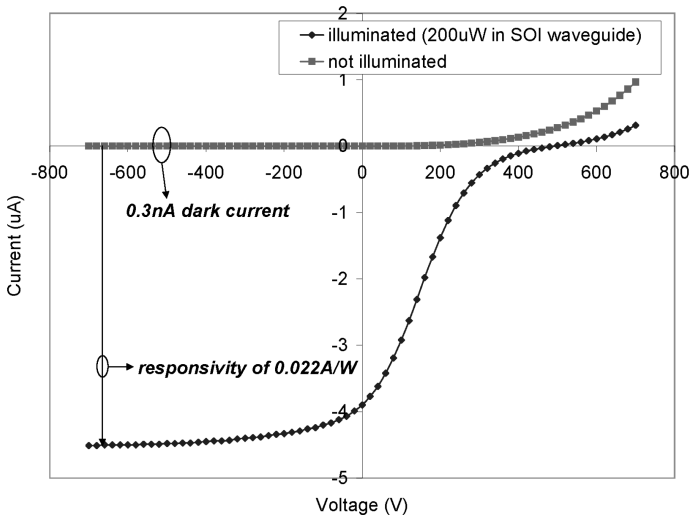


Figure 7.5: IV-characteristics of the grating-based photodetector

thick in our case. Simulations show that only 4 percent of the incident power is absorbed in this case. This can be largely improved by increasing the absorption layer thickness. The dark current of a 10 μm x 10 μm device was 0.3nA at a reverse bias of 1V.

The IV characteristics of a device with and without illumination is shown in figure 7.5.

Integration with functional SOI waveguide circuits

To show the feasibility of integration onto an SOI waveguide layer, InP/InGaAsP photodetectors were fabricated on top of passive wavelength selective SOI filters. The filter structure consists of 4 ring resonators placed in series, performing a wavelength selection operation. To inject light from an optical fiber into the SOI waveguide circuit, the same type of grating coupler for coupling to the photodetector was used. The SOI waveguide circuit is shown in figure 7.6, together with the measured photodetector current versus wavelength. The simulated spectrum of the light injection from an optical fiber into the SOI waveguide using a grating coupler is superimposed.

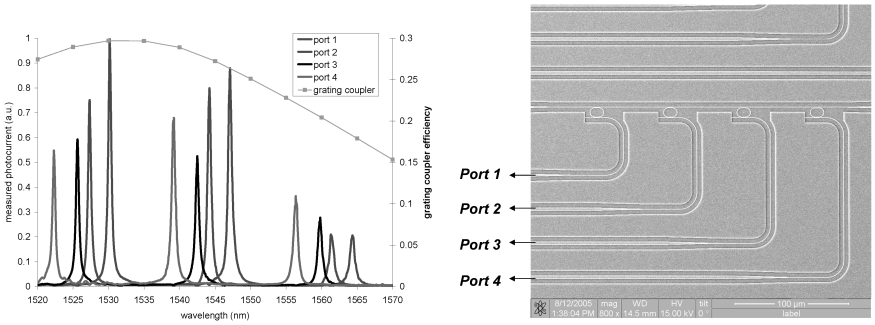


Figure 7.6: Grating-based photodetector bonded on a ring resonator filter structure

7.1.3 Influence of residual doping of the absorption layer

The non-ideal behavior of the IV curve for the illuminated devices in forward bias and around zero bias, as can be seen in figure 7.2 and 7.5, is related to a residual n-type doping of the absorbing layer of about $2x10^{16}/cm^3$. The IV characteristics of the device under illumination were simulated using DESSIS (see section 6.5). The InP/InGaAsP layer stack used in the simulations consists of a 600nm n-type InP undercladding, four InGaAsP quantum wells with a band gap wavelength of 1550nm in between two separate confinement layers of 150nm (band gap wavelength 1.25 μm) and a 2 μm p-type InP and 150nm p++ InGaAs contact layer. The resulting IV curves for different doping levels of the absorbing quantum wells are shown in figure 7.7, revealing the typical behavior seen in the experiments. At sufficiently high reverse bias the free carriers in the absorbing region are also swept away, resulting in the expected behavior of an illuminated photodetector.

7.2 Waveguide-coupled bonded MSM photodetectors

7.2.1 Operation principle

The operation principle of a metal-semiconductor-metal (MSM) photodetector is based on cascading two Schottky barriers on a common absorbing substrate, as is shown in figure 7.9. An external voltage applied between the two electrodes biases one of them in the forward and

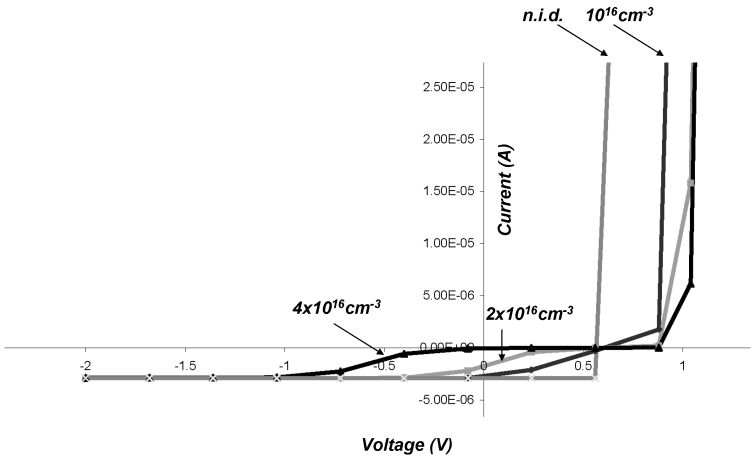


Figure 7.7: Influence of residual doping of the absorption layer on the IV characteristic of the device

the other in the reverse direction. At zero bias, the structure is symmetrical and the electrical field in the center of the structure is zero. Photoexcited electrons are trapped in the potential well and the nett photocurrent is zero. By applying a voltage across the Schottky diode, the potential barrier at the forward bias contact decreases and there is an electrical field between the Schottky electrodes. The majority of the photoexcited electrons still are trapped in the potential well as they do not have sufficient energy to traverse the potential barrier at the positive contact. The photoexcited holes cannot leave the active region due to the charge of the trapped electrons. When the voltage reaches a critical value (the flat band voltage V_{FB}), namely when the whole absorbing region below the electrodes is depleted and the electrical field is negative everywhere, all the excess carriers drift through the device since the potential barrier at the positive contact disappears. The width W of the depletion region in a reverse biased Schottky barrier contact is given by

$$W = \sqrt{\frac{2\varepsilon_r \varepsilon_0 V}{qN_d}} \tag{7.1}$$

in which ε_r is the relative permittivity of the semiconductor, N_d the doping level and V the applied voltage. The flat band voltage V_{FB} can then be found by replacing W by the spacing between the electrodes L. Therefore,

$$V_{FB} = \frac{qN_D}{2\varepsilon_r\varepsilon_0}L^2 \tag{7.2}$$

Above this flat band voltage the photocurrent remains constant in first order (although a slight increase in photocurrent can be observed due to a gain effect at increased voltages). The band diagram of the MSM photodetector structure for a zero volt bias, a bias below V_{FB} and above V_{FB} is shown in figure 7.8.

The Schottky barrier height of Ti/Au on an InGaAs absorbing layer is approximately 0.2eV. This low barrier height results in a large dark current, resulting in a signal to noise ratio that is too small for photodetector applications [173]. Therefore, a thin InAlAs layer is grown on top of the absorbing InGaAs layer, increasing the Schottky barrier height to approximately 0.7V (a so called Schottky barrier enhancement layer or SBEL).

The coupling of light from the SOI waveguide to the absorbing MSM layer is based on a directional coupling mechanism between the SOI fundamental mode and the waveguide mode existing in the MSM layer, laterally confined by the two metal contacts. Although it was discussed in section 4.3.1 that the directional coupling mechanism is not tolerant to fabrication errors, this is not the case here. As the waveguide is absorbing, the influence of fabrication errors is far less severe, as the device length can be increased to accommodate fabrication errors.

7.2.2 Fabrication procedure

Fabrication of bonded metal-semiconductor-metal photodetectors started by ultra-thin DVS-BCB bonding of the epitaxial layer structures on a processed SOI wafer containing 3μm wide SOI waveguides. The layer structure consists of a non-intentionally doped InGaAs absorption layer (165nm) and an InAlAs Schottky barrier enhancement layer (40nm). The spacing between the top of the SOI waveguide and the MSM epitaxial layer stack was 300nm. After removal of the InP substrate, the individual MSM photodetectors islands were defined. After applying and opening of a DVS-BCB isolation layer, the TiAu Schottky contacts were deposited. A top view of a fabricated device is shown in figure 7.10, showing the SOI waveguide, the InGaAs absorption layer and the TiAu Schottky contacts. The spacing of the electrodes was 3μm.

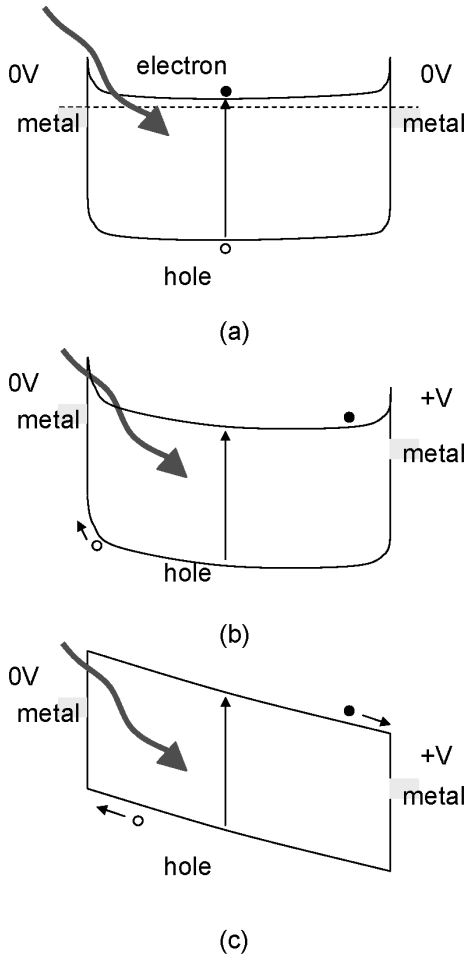


Figure 7.8: Metal-semiconductor-metal photodetector band diagrams (one-dimensional representation)

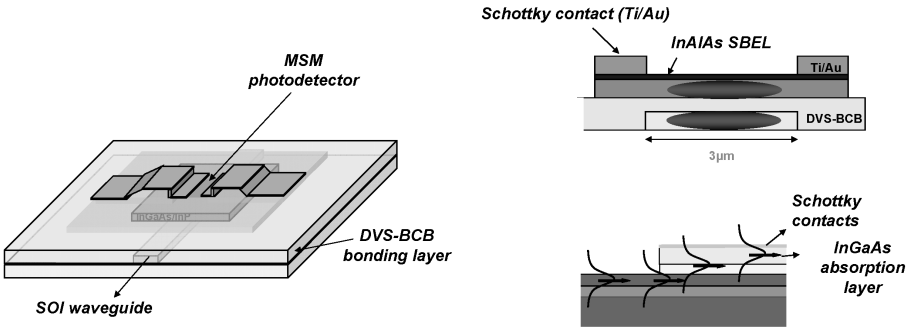


Figure 7.9: Metal-semiconductor-metal photodetector integrated above an SOI waveguide: device structure and layout

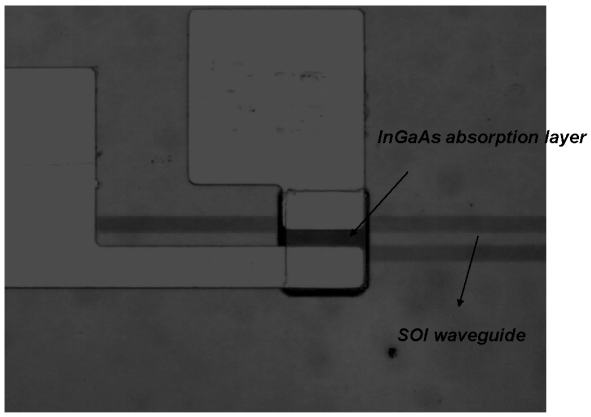


Figure 7.10: Metal-semiconductor-metal photodetector integrated on top of an SOI waveguide: experimental realization

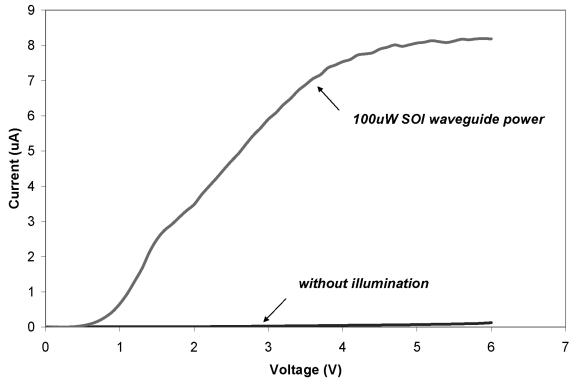


Figure 7.11: First IV curve results of a metal-semiconductor-metal photodetector integrated on top of an SOI waveguide

7.2.3 First results

A current versus voltage characteristic for this type of device is shown in figure 7.11. A device responsivity of 0.08A/W was obtained over a large wavelength range for a first batch of devices. The flat band voltage lies around 4V. This is due to the large spacing of the electrodes. The dark current of the device shown in figure 7.10 is 100nA at 5V bias.

This device was proposed originally in the context of this PhD and is now investigated in detail in the context of the PhD project of Joost Brouckaert.

7.3 Germanium versus III-V

In this chapter, the use of bonded InP/InGaAsP epitaxial layer structures to detect light in a wavelength range used for optical communication was discussed. An alternative solution is to use germanium containing materials. There are three main approaches that have been proposed to integrate germanium, each one based on a different type of active layer: $Si_{1-x}Ge_x$/Si heterostructures, SiGe or Ge quantum dots on silicon layers and the use of pure Ge. The objective of growing multiple quantum wells of SiGe/Si is to obtain strained SiGe layers with a reduced band gap as compared to unstrained SiGe layers. The lattice mismatch between silicon and SiGe limits however the deposited thickness to a critical value before the onset of dislocation generation. For the large germanium concentrations needed to extend the absorption

wavelength to 1.55μm, the thickness of a single strained layer, which can be grown without dislocations is limited to 10-20nm . This limits the effective absorption coefficient. This technology was used to fabricate SOI waveguide integrated photodetectors at 1.3μm, but rather small efficiencies and long detectors (several 100μm) were reported [174]. A second approach relies on the Stranski-Krastanow growth of pure germanium on silicon. This growth regime leads to the formation of germanium-rich quantum dots. Waveguide integrated photodetectors using a vertical stacking of self-assembled quantum dot layers were reported, however, absorption coefficients at 1.55μm remain low and therefore, only long devices (several millimeter) with low quantum efficiencies were reported [175]. A third, more promising approach to obtain high absorption at 1.3μm and 1.55μm is the use of strained pure germanium layers. Because of the large lattice mismatch of 4.2 percent between silicon and germanium, special growth strategies need to be applied. One of these strategies is to grow a thin low temperature germanium buffer layer, followed by a high quality strained germanium layer [176]. A number of vertically illuminated germanium-on-silicon detectors have been reported, which use this low-temperature germanium buffer layer method. In [177, 178], a responsivity of 0.25A/W at 1.55μm is obtained, while using a resonant cavity, a responsivity of 0.73A/W at 1.53μm was reported in [179]. The integration of germanium photodetectors and amorphous silicon waveguides was reported in [25]. A device responsivity of 1A/W was obtained. Dark current levels, due to defects in the grown germanium layer, were relatively high and the wavelength span over which the device operated was limited.

From this discussion it is clear that there is also a strong interest in using germanium as a photodetector material at optical telecommunication wavelengths. However, in order to cover the complete C-band and L-band of optical communication, InGaAs photodetectors are still required. We believe that heterogeneous integration of III-V compound semiconductors and in particular the approach based on bonding of unprocessed III-V dies onto SOI waveguide wafers can lead to higher performance: InGaAs has an unchallenged position in low dark current, high speed and high sensitivity integrated near-infrared photodetectors. On top of that, for the fabrication of SOI waveguide integrated laser diodes, integration of III-V material is so far the only viable solution and detectors and sources could be fabricated at the same time, using the same wafer-scale processing steps. The high processing tem-

perature for germanium growth is an additional hurdle for using this material, especially when the integration with electronics is envisaged.

7.4 Conclusions

In this chapter we presented various types of InP/InGaAsP photodetectors, each differing in required bonding technology, optical coupling structure, processing procedure and obtained responsivity. Both pin-photodetector structures and metal-semiconductor-metal structures were discussed. While butt-coupled pin-photodetectors are directly compatible with the fabrication of bonded laser diodes, their device footprint is rather large. From that point of view, the use of a grating-coupled vertically illuminated photodetector or MSM photodetector is preferable. While the first type of photodetector allows the use of standard DVS-BCB bonding technology, the number of processing steps are high compared to the MSM photodetector structure, which however requires the use of a sub-micron bonding layer thickness. From this we can conclude that all three types of photodetectors can be advantageous depending on the application and requirements.

The work presented in this chapter has been the subject of 2 publications in international journals (Appendix B.1-5 and B.1-6).

Chapter 8

Bonded passive components

Feeling single, Seeing double
Emmylou Harris

In this chapter, we will discuss the fabrication of passive optical components based on DVS-BCB adhesive bonding. Devices in a bonded silicon-on-insulator waveguide layer will be discussed. It concerns the fabrication of low optical power thermally bistable silicon-on-insulator ring resonators, a high-efficiency silicon-on-insulator fiber-to-waveguide grating coupler based on a gold bottom mirror approach and a passive photonic interconnection layer on CMOS.

8.1 Introduction

While in previous chapters DVS-BCB bonding was used to integrate different material systems due to their distinct advantages, in this chapter DVS-BCB bonding will be used to access both sides of the optical layer, either for processing or for interfacing with an optical fiber. As the bonding layer no longer has an optical function in these cases, standard DVS-BCB bonding was used, as this is easier to achieve than ultra-thin DVS-BCB bonding.

8.2 Double-sided processing of SOI waveguide layers

So far in this work, the DVS-BCB bonding process was only developed and used for transferring InP/InGaAsP epitaxial layer structures to a host substrate. However, the use of DVS-BCB bonding can also be used to improve the functionality of silicon-on-insulator based components. Therefore, we will discuss the development of a silicon-on-insulator bonding process carried out in the context of this PhD, and show three types of applications of this bonding process: low-power bistable bonded ring resonators, high-efficiency SOI fiber-to-waveguide grating couplers based on a gold bottom mirror and the integration of an SOI photonic layer on top of a (dummy) CMOS substrate.

8.3 Development of SOI waveguide layer transfer using DVS-BCB

The DVS-BCB bonding process developed for transferring silicon-on-insulator waveguide circuits to a host substrate is schematically depicted in figure 8.1.

The bonding procedure starts by cleaning the SOI die (using a SC-1 solution) and the host wafer. Subsequently, a DVS-BCB layer is spin coated on the SOI substrate in order to planarize the waveguide topography. Imprinting of the SOI structures in a DVS-BCB layer was also successful, although the reliability in terms of inclusion of voids at the bonding interface was lower. After spin coating, the DVS-BCB is soft-cured and the edge bead from the spin coating process is removed, by cleaving the edges of the SOI die (this would no longer be an issue when using full SOI wafers for which spin coaters are equipped with a dedicated edge bead removal system). On the host substrate, DVS-BCB is spin coated and both substrates are attached. The stack is cured as discussed in section 3.5. After bonding, the silicon substrate has to be removed. As silicon is a much harder material than InP, more care has to be taken not to damage the bonding interface during mechanical grinding. Two types of grinding slurries were tried: a SiC and an AlO_x suspension. While the thinning rate was much higher in the case of SiC, it tended to damage the bonding interface and was therefore no longer considered in this work. The mechanical grinding was stopped when about 150μm of the original silicon substrate remained. As the

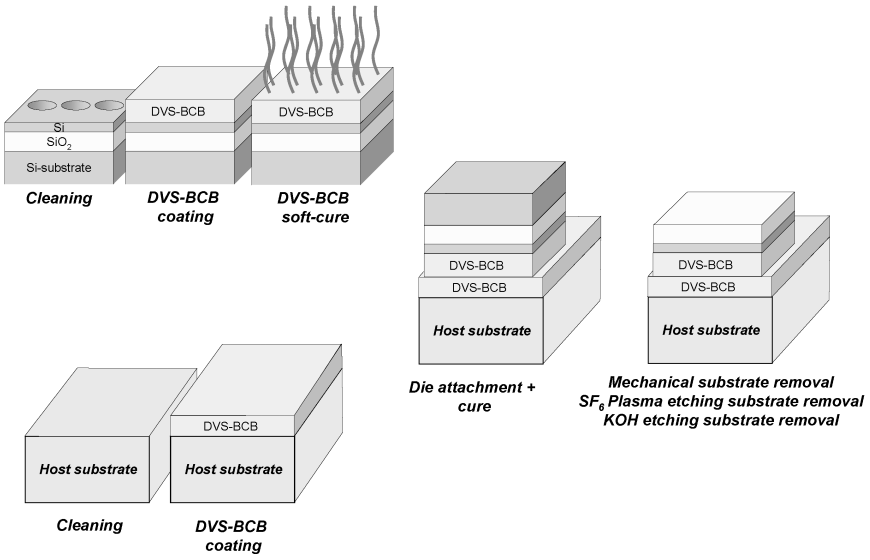


Figure 8.1: SOI layer transfer procedure

chemical etchants used for etching silicon (i.e. KOH) also attack the interface between DVS-BCB and the substrate, the immersion time in this solution must be kept to a minimum. Therefore, after mechanical grinding, a high power SF_6 inductively coupled plasma (ICP) etch was performed to further thin the substrate down to 10-20μm after which the sample was etched in a 20 percent KOH solution at 70C to remove the remaining silicon substrate, using the buried oxide layer as an etch stop layer.

Microscope images of transferred SOI waveguide structures (in this case bonded to a Pyrex host substrate) are shown in figure 8.2. High quality layer transfer was achieved.

8.4 Waveguide losses of bonded SOI waveguides

In order to further assess the bonding quality, the losses of SOI waveguides were compared before and after layer transfer. These losses were measured by a cut back method, using spiral waveguides of different length, as the one shown in figure 8.2. Assuming that the substrate leakage in the unbonded waveguide case is negligible (as was confirmed by simulation), the difference in waveguide loss can be to-

Figure 8.2: Top view of defect free transferred SOI waveguide layers

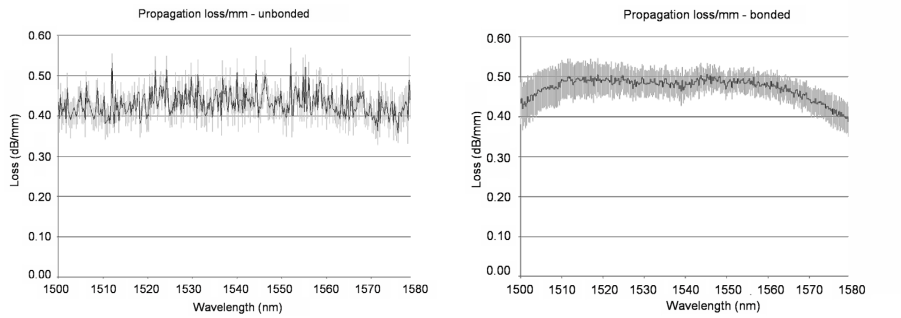


Figure 8.3: Comparison of waveguide losses before and after layer transfer (480nm waveguide width)

tally attributed to the bonding process (when a DVS-BCB upper cladding is used in the unbonded waveguide case). The measured losses are shown in figure 8.3. The waveguide losses in the bonded case are only marginally higher than those of the unbonded waveguides, indicating the good bonding quality.

8.5 Optical bistability of DVS-BCB bonded ring resonators

Active silicon photonic devices in which light is controlled by light are a long-standing goal in all-optical communication, but are challenging because of the relatively weak silicon non-linear optical properties. Optical bistability can be employed to allow all-optical functionalities, such as logic functions, modulation, switching, and memory. It has been achieved in compound semiconductor materials with strong non-linear optical properties. In silicon, one can achieve optical bistability by exploiting the thermal non-linear optical effect, because of the large thermo-optic effect ($^{\delta n}/_{\delta T} = 1.86 \times 10^{-4}/K$). The use of resonant cavities to enhance the bistability (i.e. bring this bistability to low input power levels) is widespread. In [180], optical bistability in a 5μm radius silicon-on-insulator ring resonator was observed using input optical powers around 1mW. The input power level at which bistable action occurs depends on the thermo-optic coefficient, which is a material property, the quality factor of the ring resonator, which depends on the quality of the fabrication process and the design of the cavity (i.e.

the coupling between bus waveguide and ring) and the thermal resistance of the cavity. In the case of a silicon-on-insulator ring resonator, nearly all heat (generated by the two-photon absorption induced free carrier absorption in the resonator) has to be sunk through the buried oxide layer, which determines the thermal resistance of the device. In this section we will discuss that, by standard DVS-BCB bonding of the devices onto a host substrate (in this case Pyrex), optical bistability at lower power levels can be achieved, due to the increased thermal resistance of the bonded device compared to the as-fabricated SOI ring resonator.

8.5.1 Origin of thermal bistability

To demonstrate optical bistability with a ring resonator, a pump wavelength slightly above the resonance wavelength of a ring resonator was used and the output power at the the drop port was measured while varying the input power. As the input power is modified, the ring resonance shifts due to the thermo-optic effect in silicon, thereby modifying the ring resonator transmittance. The resonance shift strongly depends on the optical power circulating inside the ring, which in turn strongly depends on the wavelength detuning between the optical source and the shifted resonance; the combined effect of these interrelated mechanisms leads to the bistability curve. The type of bistability and the power levels at which they occur strongly depend on the wavelength detuning.

At low optical power, the input wavelength is slightly larger than the resonant wavelength, and therefore the power transmission at the drop port is low as no resonance occurs. Increasing the input power shifts the resonance wavelength towards the input wavelength thereby increasing the transmission. Again decreasing the input power induces the opposite behavior, although switching occurs at a different input power level. This leads to the bistability curve shown in figure 8.4.

8.5.2 Measurement of thermal bistability and memory function

Optical bistability was observed in a bonded ring resonator with a ring radius of 10μm bonded using standard DVS-BCB bonding (3μm DVS-BCB bonding layer) to a Pyrex host substrate. After bonding, the silicon substrate was removed, leaving the ring resonator with its buried oxide cladding layer attached to the Pyrex substrate.

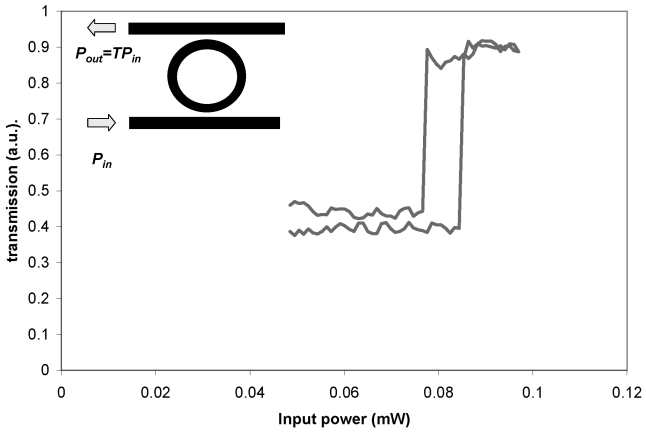


Figure 8.4: Low-power thermal bistability measured on a bonded SOI ring resonator: drop port characteristics (40pm detuning from the resonance wavelength)

At low power levels, a resonance at a wavelength of 1543.53nm was observed with a quality factor of about 15000. As the input wavelength was fixed at 1543.57nm, the transmission at low power levels is low. By increasing the input power, the resonance wavelength shifts and bistability is obtained at 80μW SOI waveguide input power as shown in figure 8.4. A 3dB increase in transmission is observed. This is low compared to the 10dB modulation reported in [180] and is related to the low input power levels at which the bistability occurs.

The most direct application of optical bistability is in all-optical memory. To demonstrate this functionality, we show in figure 8.6 switching of the output power between two stable states by modulation of the input power. To obtain a larger extinction ratio (thereby also increasing the power levels at which the bistability occurs), a different input wavelength of 1543.61nm was chosen. As this wavelength is more detuned from the resonance wavelength, the required optical power in the SOI waveguide to achieve bistability is larger and the extinction ratio is higher. The transmission efficiency at the pass port was recorded as a function of the input power and is plotted in figure 8.5. Optical bistability is observed around 600μW of input power and an extinction ratio of about 10dB was obtained.

Using this bistability, the memory function is demonstrated in figure 8.6 by using a bias input power level of about 600μW, lying in the

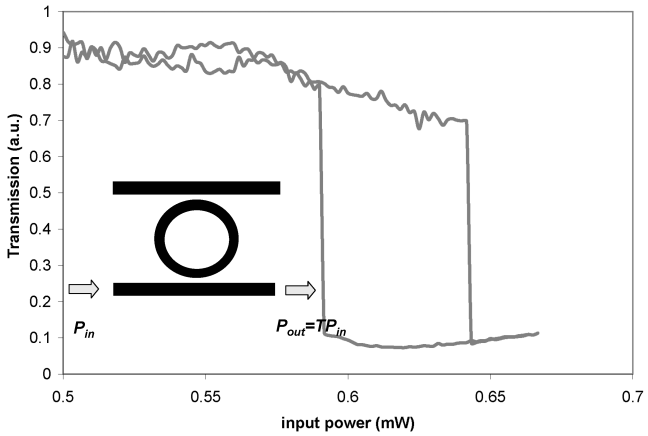


Figure 8.5: Transmission at the pass port as a function of input power (80pm detuning)

hysteresis loop. By slightly increasing or decreasing the input power, the ring resonator state can be modified, showing the memory function of an optically bistable ring resonator.

8.5.3 Influence of the thermal resistance: power versus speed

Although the modulation bandwidth of the bistable ring resonator was not assessed, it is clear that the increase in thermal resistance has an averse effect on the modulation speed, as the thermal time constant τ_{therm} is given by

$$\tau_{therm} = R_{th} C_{th} \tag{8.1}$$

As the temperature increase in the ring resonator, due to the presence of the circulating optical power, has a third power dependence on the optical power levels (this is due to the fact that a two-photon absorption process is responsible for the free carrier generation and an additional photon is required for the free carrier absorption and subsequent thermalization of the free carrier), the power levels at which bistability occurs decrease, according to

$$P_{bist} = P_{bist,0} \sqrt[3]{\frac{R_{th,0}}{R_{th}}} \tag{8.2}$$

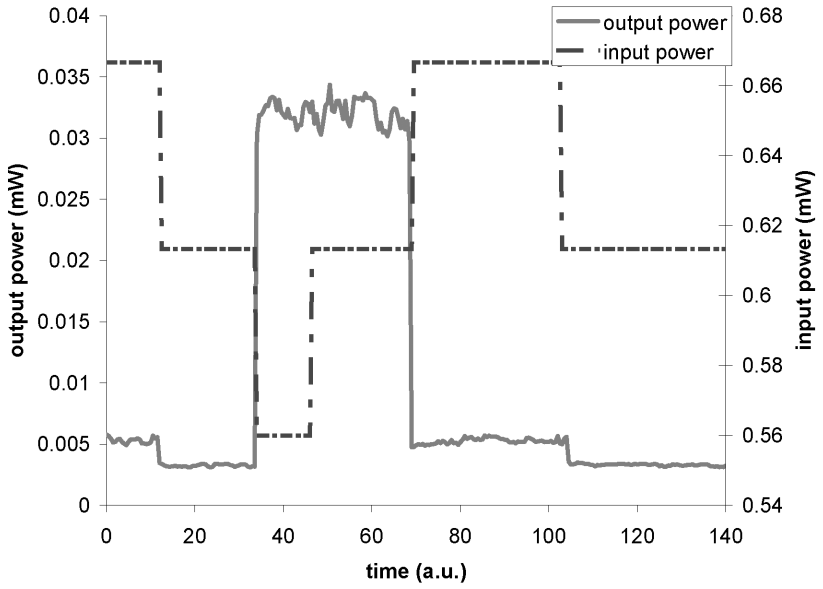


Figure 8.6: Demonstration of the memory function of a bistable ring resonator

which is much slower than the $1/R_{th}$ dependence of the modulation bandwidth of the device. As in [180] modulation bandwidths of 500kHz were reported for an unbonded device, we can conclude that the modulation bandwidth of the bonded device will be in the kilohertz range.

8.6 High-efficiency SOI fiber-to-waveguide grating couplers

As was discussed in section 4.6.5, a gold mirror can be used to dramatically increase the coupling efficiency between single-mode optical fiber and SOI waveguide. A field plot of the optimized design as discussed in section 4.6.5 is shown in figure 8.7.

8.6.1 Fabrication procedure

The fabrication procedure is outlined in figure 8.8. It starts by the cleaning of the SOI grating coupler dies and the Pyrex host substrate. A DVS-BCB spacer layer of an optimized thickness is spin coated on the

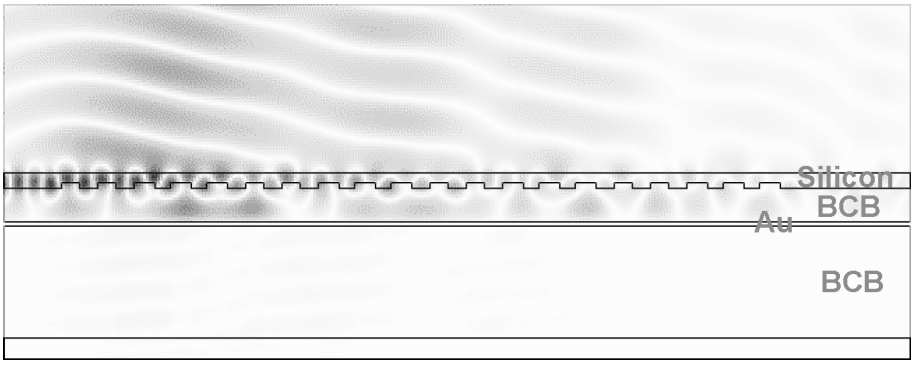


Figure 8.7: Integration of a gold bottom mirror to increase the fiber coupling efficiency

grating coupler die and soft-cured. As is clear from figure 4.62, the optimal spacer layer thickness was 850nm in this case. After DVS-BCB spin coating, a gold mirror was defined on top of the grating couplers using a lift-off process. After definition of the gold mirror, DVS-BCB is spin coated on the Pyrex substrate and the two substrates are attached and cured. The removal of the silicon substrate was discussed in section 8.3.

8.6.2 Measurement results

A top view of the bonded structures is shown in figure 8.9. The bonded waveguides, the gold bottom mirror and the grating couplers can be clearly identified. The coupling efficiency of this type of device is shown in figure 8.10 . Coupling efficiencies up to 69 percent were obtained, which is about a threefold increase in coupling efficiency compared to an unbonded grating coupler. This dramatic increase in coupling efficiency is extremely important for practical applications, as the requirements on the fiber insertion losses for a photonic integrated circuit are typically very high.

8.7 Integration of a photonic layer on top of CMOS

In the previous applications of SOI layer transfer, the host substrate only acted as a mechanical support for the bonded optical components. As was discussed in section 1.2, in future generation electronic circuits, a severe bottleneck is expected on the global electrical interconnect level, contacting the longest interconnection lengths on a chip.

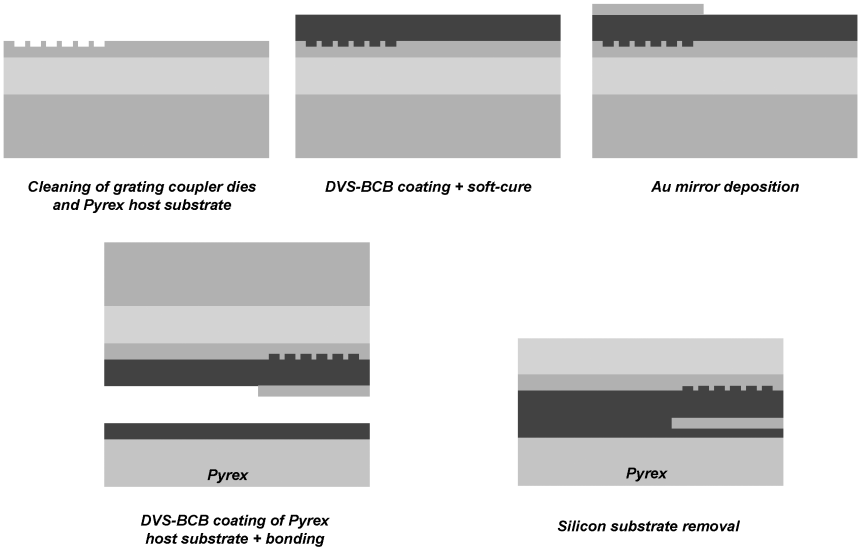


Figure 8.8: Fabrication procedure of an SOI mirror-clad fiber-to-waveguide grating coupler

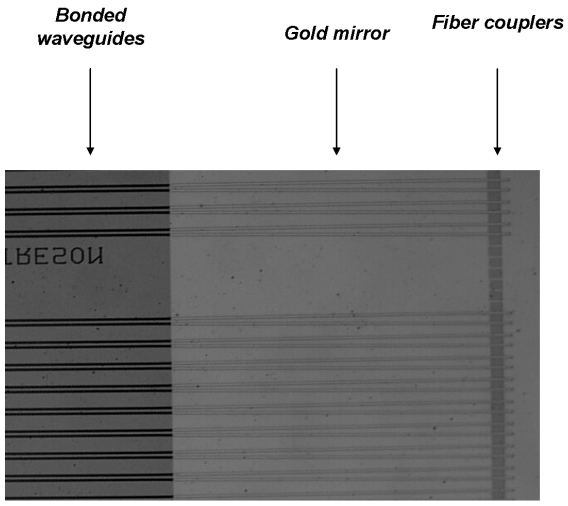


Figure 8.9: Top view of the fabricated grating coupler structures

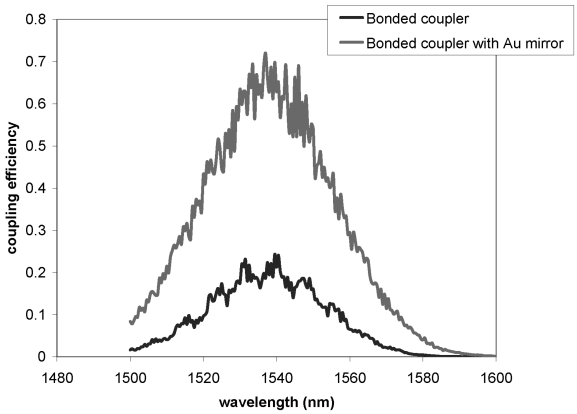


Figure 8.10: Measured fiber coupling efficiency using a gold bottom mirror

With decreasing device dimensions, it is increasingly difficult to keep propagation delays acceptable and even with the most optimistic estimates for conductor resistivity and dielectric permittivity, the projected performance road map will not be met. Therefore there is a need for radically different interconnect approaches and, as indicated by the ITRS road map, one of the most promising solutions is the use of an optical interconnect layer on CMOS. This interconnection layer could be defined in the CMOS layer (when SOI is used for high-performance electronic circuits). This approach however consumes CMOS silicon real estate and the processing of the photonic components could interfere with the CMOS processing. By using an additional SOI waveguide layer on top of the CMOS, both photonic processing and CMOS processing can be kept separate. The two approaches are shown in figure 8.11.

An example of the integration of an SOI waveguide layer on top of a dummy CMOS substrate using DVS-BCB bonding, carried out in this work, is shown in figure 8.12, indicating the silicon waveguides integrated on top of an oxide covered silicon wafer with metal pads.

While this basic demonstration is a starting point for the integration of optical interconnects on CMOS electronic circuits, the integration of active opto-electronic devices on top of this photonic/electronic substrate (as was discussed in chapter 6 and chapter 7) and the electrical connection of these devices to the electronic circuit still has to be demonstrated.

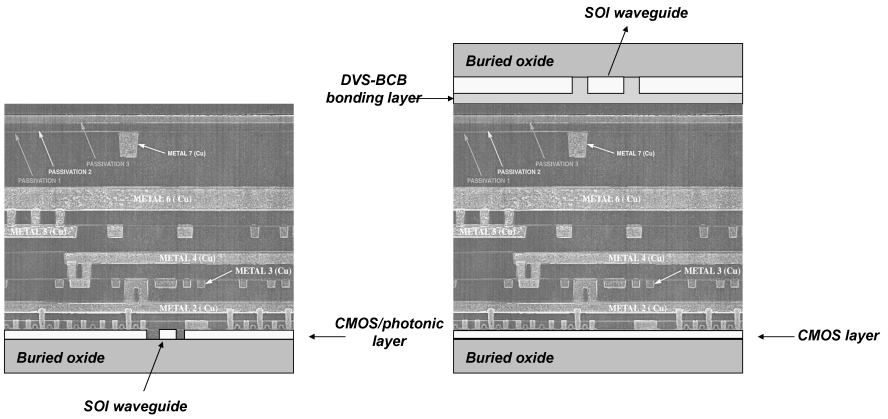


Figure 8.11: Integration of a photonic layer on a CMOS substrate: integration of the photonic interconnection layer in the CMOS layer and the integration of an interconnection layer on top of CMOS

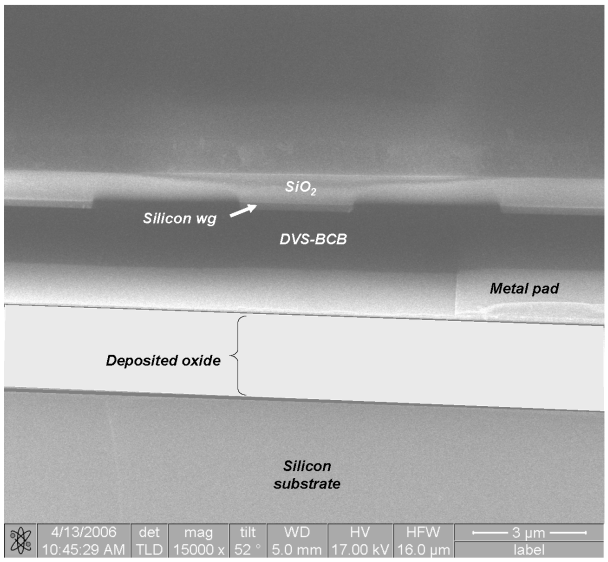


Figure 8.12: Integration of an optical interconnection layer above CMOS

8.8 Conclusions

In this chapter we presented the use of (standard) DVS-BCB bonding for improved functionality of passive optical components. Devices based on silicon-on-insulator layer transfer were described, in which the DVS-BCB bonding is used to be able to access both sides of the components (either for processing or for optical access with an optical fiber). This type of components can further be combined with an additional bonding step, for example for the integration of InP/InGaAsP active components on top of a bonded SOI interconnection layer or the integration of a bonded photodetector on top of an SOI grating coupler structure with gold bottom mirror.

The work presented in this chapter has been the subject of 1 publication in international journals (Appendix B.2-10).

Chapter 9

Conclusions

California Dreaming
The Mamas and the Papas

9.1 Conclusions

Like in electronics, photonic components can be integrated on a single chip. This improves performance and compactness, and lowers the cost of the fabricated devices by the economy of scale. The alignment of individual components is largely taken care of by wafer-scale lithographic processes. Silicon-on-insulator (SOI) is emerging as an promising platform to integrate these optical functions, due to the compactness of the devices and the fact that one can take advantage of the enormous CMOS infrastructure and processing capability available. While the integration of passive optical functions is straightforward, the integration of both active (light emission, light amplification, light detection) and passive optical functions is hampered by the indirect band gap of silicon. As state-of-the-art active devices for telecommunication are fabricated in III-V semiconductors, the heterogeneous integration of III-V components and silicon-on-insulator waveguide circuits is proposed in this work.

An adhesive die-to-wafer bonding process using DVS-BCB was proposed and developed in this work to achieve this integration. The process is based on transferring unprocessed InP/InGaAsP epitaxial layer structures to a silicon-on-insulator waveguide circuit, after which the III-V components are processed, lithographically aligned to the underlying SOI features. The die-to-wafer bonding process was optimized in

this work, in terms of cleanliness of the respective substrates, the degree of planarization of the DVS-BCB spin coating process, the attachment of dies on the substrate and the curing of the bonded stack. Sub-micron bonding layer thicknesses were demonstrated. Substantial characterization of the bonding interface was performed. We demonstrated that stress levels in the bonded stack are acceptable due to the low bonding temperature.

Besides the development of a heterogeneous integration process, several methods for coupling of light between the passive SOI waveguide circuit and the III-V device bonded on top were developed in this work and compared in terms of efficiency, fabrication tolerance, optical bandwidth and device footprint. A design based on an inverted adiabatic SOI taper was proposed, to efficiently couple in-plane operating bonded III-V devices to the SOI waveguide circuit, while a diffractive grating structure was proposed for surface-normal operating devices. As these coupling issues are comparable to the problem of efficient coupling of light from a single-mode optical fiber into a high index contrast waveguide, the same approaches were followed to design and fabricate high-efficiency fiber-to-waveguide coupling structures based both on an inverted adiabatic taper and a diffractive grating structure. The diffractive grating approach was even further extended in this work to allow duplexing operation, in order to spatially separate two wavelength bands.

Bonded light emitting devices were fabricated and characterized, both stand-alone device and devices coupled to an underlying SOI waveguide circuit. Bonded LEDs, bonded Fabry-Perot and DFB laser diodes were demonstrated, while an integrated Fabry-Perot laser diode was coupled to an SOI waveguide. The thermal behavior of these devices was thoroughly studied, as the low thermal conductivity of the DVS-BCB bonding layer hampers efficient heat sinking. We showed that this can be circumvented by integrating an additional heat sink circuit.

Three types of bonded photodetectors coupled to an SOI waveguide circuit were designed and fabricated. Bonded pin-type photodiodes, using the inverted adiabatic taper approach and the diffractive grating approach for optical coupling, were demonstrated and a new type of metal-semiconductor-metal (MSM) photodetector was demonstrated.

Besides for the integration of passive and active optical functions, the DVS-BCB layer transfer process can be used to fabricate new types of devices due to the possibility of double-sided processing (or optical access) and the creation of a high vertical refractive index contrast

for III-V materials, due to the low refractive index of the DVS-BCB layer. This led to the demonstration of low-power optically bistable bonded ring resonators and high-efficiency fiber-to-waveguide grating couplers based on a gold bottom mirror.

9.2 Prospects

Besides the analysis and demonstrations discussed in this work, an equally important (or even more important) aspect are the prospects for innovative research in the field of photonics and more in particular in the field of heterogeneous III-V/silicon photonics.

While the processes developed in this work were limited to bonding a single InP die on a host substrate, the extension of this principle to bonding multiple dies on a host substrate is to be developed. A logical continuation of this work is to explore the possibilities of optical coupling between the III-V waveguide layer and the SOI waveguide stack using a beveled laser diode facet and an SOI diffraction grating. This can lead to integrated tunable laser diodes, in which the tuning element is a wavelength selective optical function in the SOI. This could allow the fabrication of low-cost devices suitable for telecommunication purposes or tunable devices to interrogate an optical sensor integrated on the same SOI waveguide platform. A possible layout for the tunable laser is shown in figure 9.1. The ring resonators show a slightly different free spectral range in order to obtain a vernier-like tuning effect. Both slow thermal tuning of the rings or fast tuning by electrical carrier injection or depletion could be envisaged. The development of high-efficiency grating coupler structures based on a silicon overlay in this work, the continuous improvement of long-wavelength VCSELs and the insight of using grating coupler structures as duplexers, hold the promise of fabricating low-cost optical transceivers for fiber-to-the-home (FTTH) applications, in which a two-dimensional grating coupler structure is used for duplexing the downstream 1.5μm and upstream 1.3μm wavelength band at the subscriber side for voice, video and data transfer. The upstream 1.3μm light can be generated by a polarization controlled VCSEL, which is integrated on top of a one-dimensional grating coupler, to couple the light in the SOI waveguide circuit. The layout of the proposed transceiver is schematically shown in figure 9.2.

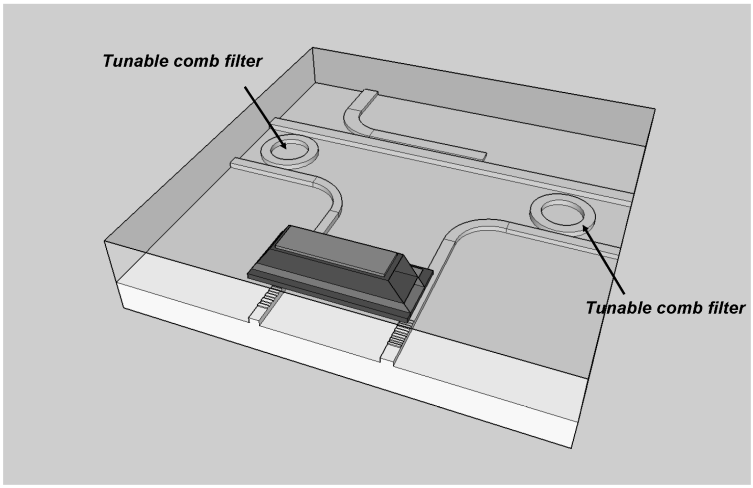


Figure 9.1: A widely tunable laser concept based on the heterogeneous integration of SOI and InP/InGaAsP epitaxial layers

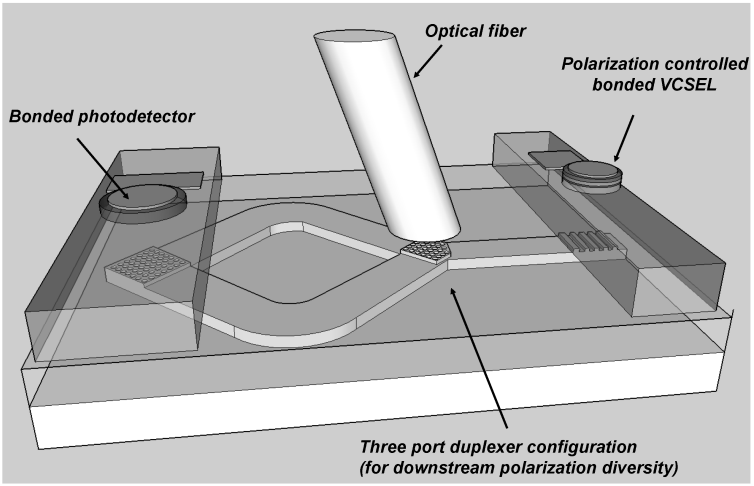


Figure 9.2: A concept for a transceiver circuit for fiber-to-the-home applications

Appendix A

Adiabaticity criterion

In an article published by Love [181], an adiabaticity criterion was derived based on coupled mode equations. These equations form the basis for the construction of a criterion for slow variation, i.e. a delineation of how fast the cross-section of a spot size converter is allowed to change before power is lost from the mode of interest.

The coupled mode equations for coupling between mode j and l in a z-dependent waveguide structure can be written as

$$\frac{db_j}{dz} - i\beta_j(z)b_j(z) = C_{jl}(z)\exp(i\int_0^z \beta_l(z)dz) \tag{A.1}$$

in the case of weak coupling. In equation A.1, β_j is the propagation constant and b_j the complex amplitude of mode j. As all modes are presumed to be power normalized, the power coupled to mode j is given by $|b_j|^2$ and must be kept small in order to obtain an adiabatic transition for mode l through the structure. In this differential equation, the coupling from mode l to mode j is characterized by a coupling coefficient C_{jl} given by

$$C_{jl} = \frac{k_0}{4}(\frac{\varepsilon_0}{\mu_0})^{\frac{1}{2}}\frac{1}{\beta_j(z)-\beta_l(z)}\int_S \mathbf{e_j}\cdot\mathbf{e_l}\frac{\mathbf{d}\varepsilon_\mathbf{r}}{\mathbf{dz}}\mathbf{dS} \tag{A.2}$$

with $\mathbf{e_j}$ and $\mathbf{e_l}$ the respective electrical fields of mode j and l.

Solving equation A.1, with the initial boundary condition of $b_j = 0$ ($j \neq l$), as only mode l is assumed to be excited in the structure, leads to

$$b_j(z) = e^{i\int_0^z \beta_j(\xi)d\xi} \int_0^z C_{jl}(\xi)\exp(j\delta\beta(\xi))d\xi \tag{A.3}$$

as can be verified by direct substitution in equation A.1. In equation A.3, $\delta\beta$ is defined as

$$\delta\beta(\xi) = \frac{1}{\xi}\int_0^\xi (\beta_l(\xi') - \beta_j(\xi'))d\xi' \tag{A.4}$$

The function $b_j(z)$ should remain close to zero along the waveguide structure for adiabatic operation. Equation A.1 strongly resembles the coupled mode equations for directional coupling (with C_{jl} the coupling coefficient and $\delta\beta$ the phase mismatch between the modes), only in this case the second differential equation describing the reverse coupling from mode j to mode l is omitted due to the weak coupling. From the theory of directional couplers, we know that nearly no coupling occurs when

$$\delta\beta >> C_{jl} \tag{A.5}$$

which is what is wanted everywhere along the waveguide for adiabatic transition. C_{jl} is most sensitive to the change in waveguide profile with z (equation A.2) and $\delta\beta$ determines the average beat length $^{2\pi}/_{\delta\beta}$ between the j^{th} and the l^{th} mode. This brings us to the following conclusion, which is also known as the adiabaticity criterion: a mode will propagate with negligible loss to another mode provided that the waveguide changes over a distance that is large compared to the local beat length between both modes.

When applying this criterion to a waveguide structure that adiabatically transforms its fundamental waveguide mode by changing the width of the waveguide, the criterion transforms to

$$\left|\frac{\partial w}{w}\right| << 1 \tag{A.6}$$

with ∂w the width variation corresponding to $\partial z = z_b$ with $z_b = \frac{2\pi}{(\beta_{fund} - \beta_{\max})}$. In equation A.6, β_{max} is the propagation constant of the first higher order mode to which the fundamental mode can couple. Accordingly, the adiabaticity criterion transforms to

$$\left| \frac{1}{w} \frac{dw}{dz} \frac{2\pi}{\beta_{fund} - \beta_{\max}} \right| << 1 \tag{A.7}$$

The adiabaticity criterion is only a qualitative criterion that provides insight into the required slowness in variation of the cross-section. It determines the shape (by solving the differential equation A.7 in which $<<$ is replaced by a equality). The exact length scale is not given as this depends in the interpretation of $<<$ or on the transformation loss one allows. Numerical calculation is needed for determination of the exact length of the device.

Appendix B

Publications

B.1 Patent applications

G. Roelkens, D. Van Thourhout and R. Baets, The use of a waveguide grating coupler as a duplexer.

B.2 International Journals

1. G. Roelkens, D. Van Thourhout, R. Baets, Coupling schemes for heterogeneous integration of III-V membrane devices, Journal of Lightwave Technology 23(11), p.3827-3831 (2005)

2. G. Roelkens, D. Van Thourhout, R. Baets, Ultra-thin benzocyclobutene bonding of III-V dies onto SOI substrates, Electronics Letters, 41(9), p.561-562 (2005)

3. I. Christiaens, G. Roelkens, K. De Mesel, D. Van Thourhout, R. Baets, Thin film devices fabricated with BCB waferbonding, Journal of Lightwave Technology, 23(2), p.517 (2005)

4. G. Roelkens, P. Dumon, W. Bogaerts, D. Van Thourhout, R. Baets, Efficient Silicon-On-Insulator fiber coupler fabricated using 248nm deep UV lithography, Photonics Technology Letters 17(12), p.2613-2615 (2005)

5. G. Roelkens, J. Brouckaert, D. Taillaert, P. Dumon, W. Bogaerts, D. Van Thourhout, R.Baets, Integration of InP/InGaAsP photodetectors onto Silicon-on-Insulator waveguide circuits, Optics Express 13(25), p.10102-10108 (2005)

6. G. Roelkens, D. Van Thourhout, R. Baets, R. Notzel, M. Smit, Laser emission and photodetection in an InP/InGaAsP layer integrated on and coupled to a Silicon-on-Insulator waveguide circuit, Optics Express 14(18), p. 8154-8159 (2006)

7. G. Roelkens, J. Brouckaert, D. Van Thourhout, R. Baets, R. Notzel, M. Smit, Adhesive bonding of InP/InGaAsP dies to processed Silicon-on-Insulator wafers using DVS-bis-Benzocyclobutene, Journal of Electrochemical Society, Vol. 153(12), pp. G1015-G1019 (2006)

8. G. Roelkens, D. Van Thourhout, R. Baets, High efficiency Silicon-on-Insulator grating coupler based on a poly-Silicon overlay, Optics Express 14(24), p. 11622-11630 (2006)

9. G. Roelkens, J. Van Campenhout, J. Brouckaert, D. Van Thourhout, R. Baets, P. Rojo Romeo, P. Regreny, A.azmierczak, C. Seassal, X. Letartre, G. Hollinger, J.M. Fedeli, L. Di Cioccio, C. Lagahe-Blanchard, A die-to-wafer bonding approach to photonic integration on a Silicon platform (*invited*), accepted for publication in Materials Today

10. F. Van Laere, G. Roelkens, M. Ayre, J. Schrauwen, D. Taillaert, D. Van Thourhout, T. Krauss and R. Baets, Compact and highly efficient grating couplers between optical fiber and nanophotonic waveguides, accepted for publication in Journal of Lightwave Technology

11. J. Brouckaert, G. Roelkens, D. Van Thourhout, R. Baets, Thin film III-V photodetectors integrated on Silicon-on-Insulator photonic IC's, accepted for publication in Journal of Lightwave Technology

12. G. Roelkens, D. Van Thourhout, R. Baets, High efficiency grating coupler between silicon-on-insulator waveguides and perfectly vertical optical fibers, accepted for publication in Optics Letters

B.3 International Conference Proceedings

13. G. Roelkens, D. Van Thourhout, R. Baets, Heterogeneous integration of III-V membrane devices and ultracompact SOI waveguides, Digest of the LEOS Summer Topical Meetings p.23-24, LEOS Summer Topicals, San Diego, United States (2004)

14. G. Roelkens, D. Van Thourhout, I. Christiaens, R. Baets, M. Smit, Ultra-thin BCB bonding for heterogeneous integration of III-V devices and SOI photonic components, ECIO, Grenoble, France (2005)

15. G. Roelkens, P. Dumon, W. Bogaerts, D. Van Thourhout, R. Baets, Efficient fiber to SOI photonic wire coupler fabricated using standard CMOS technology, p. TuD2, LEOS Annual, Sydney, Australia (2005)

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18. G. Roelkens, J. Brouckaert, D. Van Thourhout, R. Baets, Thin film III-V devices integrated on Silicon-on-Insulator waveguide circuits, 210th ECS meeting, Cancun, Mexico (2006)

19. G. Roelkens, J. Brouckaert, D. Van Thourhout, R. Baets, Adhesive bonding of III-V dies to Processed SOI using BCB for photonic applications, 210th ECS meeting, Cancun, Mexico (2006)

20. G. Roelkens, J. Van Campenhout, J. Brouckaert, D. Van Thourhout, R. Baets, Silicon and III-V based optoelectronics for optical interconnects (*invited*), accepted for publication on Frontiers in Optics, San Jose, United States (2007)

21. G. Roelkens, D. Van Thourhout, R. Baets, SOI grating structure for perfectly vertical fiber coupling, submitted for publication on ECIO, Copenhagen, Denmark (2007)

22. G. Roelkens, D. Van Thourhout, R. Baets, High efficiency Fiber to waveguide grating couplers in Silicon-on-Insulator waveguide structures, submitted for publication on IPNRA, Salt Lake City, United States (2007)

23. P. Dumon, G. Roelkens, W. Bogaerts, D. Van Thourhout, J. Wouters, S. Beckx, P. Jaenen, R. Baets, Basic Photonic Wire Components in Silicon-on-Insulator, Group IV Photonics, p.189-191, Antwerp, Belgium (2005)

24. D. Van Thourhout, G. Roelkens, J. Van Campenhout, J. Brouckaert, R. Baets, Technologies for On-Chip Optical Interconnects, LEOS Annual , p. TuE2, Sydney, Australia (2005)

25. F. Van Laere, G. Roelkens, J. Schrauwen, D. Taillaert, P. Dumon, W. Bogaerts, D. Van Thourhout, R. Baets, Compact grating couplers between optical fibers and Silicon-on-Insulator photonic wire waveguides with 69 percent coupling efficiency, p.PDP15, OFC, United States (2006)

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28. R. Baets, W. Bogaerts, P. Dumon, G. Roelkens, I. Christiaens, K. De Mesel, D. Taillaert, B. Luyssaert, J. Van Campenhout, P. Bienstman, D. Van Thourhout, Wiaux, Vincent, Wouters, Johan, Beckx, Stefan, Integration of photonic functions in and with Silicon,ESSDERC/ESSCIRC, Belgium, (2004)

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31. D. Van Thourhout, W. Bogaerts, P. Dumon, G. Roelkens, J. Van Campenhout, R. Baets, Functional Silicon wire waveguides, p. IWA6, IPRA, United States (2006)

B.4 International Workshops

32. G. Roelkens, J. Van Campenhout, D. Van Thourhout, R. Baets, P. Rojo-Romeo, C. Seassal, P. Regreny, P. Viktorovitch, I. O'Connor, L.Di Cioccio, J.M. Fedeli, Heterogeneous integration of light sources on an SOI waveguide platform for photonic interconnects on CMOS (PICMOS), DATE workshop Munich, Germany, March 2006

33. G. Roelkens, F. Van Laere, J. Brouckaert, D. Van Thourhout, R. Baets, DVS-BCB adhesive bonding for integrated optics, WAPITI workshop, Halle, Germany, November 2006

B.5 National Conference Proceedings

34. G. Roelkens, J. Brouckaert, I. Christiaens, K. De Mesel, P. Dumon, D. Van Thourhout, R. Baets, Heterogeneous integration of III-V material and silicon: fabrication and devices,Proceedings Symposium IEEE/LEOS Benelux Chapter, Belgium, p.83-86 (2004)

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37. J. Brouckaert, G. Roelkens, D. Van Thourhout, R. Baets, Thin film InGaAs MSM photodetectors integrated onto silicon-on-insulator waveguide circuits, LEOS Benelux annual symposium, Eindhoven, The Netherlands (2006)

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