Germanium-on-Silicon and Germanium-on-Silicon-on-Insulator
Thermally Tunable Filters for Wavelength Selection of Quantum Cascade Lasers

Thermisch afstembare filters op basis van germanium-op-silicium
en germanium-op-silicium-op-isolator voor golflengteselectie van kwantumcascadelasers

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Ghent, October 2019
Sanja Radosavljevic

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List of Acronyms

A

AWG	Arrayed Waveguide Grating
Au	Gold

B

BOX	Buried Oxide

C

C	Celsius
CMOS	Complementary Metal-Oxide-Semiconductor
Cr	Chromium

D

DBR	Distributed Bragg reflector

E

EC	External Cavity
EM	Electro-magnetic

F

FDTD	Finite Difference Time Domain
FP	Fabry-Perot
FSR	Free Spectral Range

G

Ge	Germanium

H

HF	Hydrofluoric acid

I

ICL	Interband Cascade Laser

K

K	Kelvin

M

MBE	Molecular Beam Epitaxy
MEMS	Microelectromechanical System
MMI	MultiMode Interferometer
MZI	Mach-Zehnder Interferometer

P

PCG	Planar Concave Grating
PIC	Photonic Integrated Circuit

Q

QCL	Quantum Cascade Laser

S

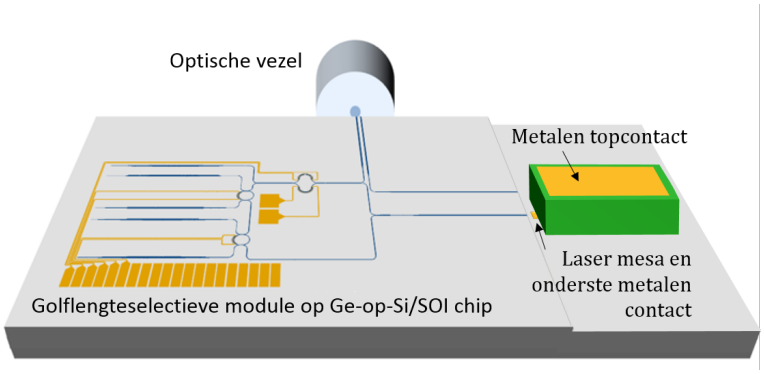
SEM	Scanning Electron Microscope
Si	Silicon
SiGe	Silicon-Germanium
SiO_2	Silicon Dioxide
SOI	Silicon on Insulator
SOS	Silicon on Sapphire

T

TE	Transverse Electric
Ti	Titanium
TM	Transverse Magnetic

Nederlandse samenvatting –Summary in Dutch–

Spectroscopie in het mid-infrarode golflengtegebied is een veelbelovende techniek om sensoren te bekomen die gevoeliger zijn en eenvoudiger kunnen differentiëren. Deze sensoren gebruiken een vingerafdruk van molecules, de absorptielijnen in het mid-infrarood, om de molecules kwalitatief en kwantitatief te detecteren. Niettemin zijn omvangrijke en dure toestellen, zoals gekoelde mid-infrarode detectoren en lichtbronnen, nodig voor conventionele systemen, hetgeen het gebruik van deze sensoren beperkt tot een laboratoriumomgeving. Het integreren van lasers met CMOS-compatibele platformen is een stap richting de creatie van geminiaturiseerde mid-infrarode sensoren. Kwantumcascadelasers werken in het hele mid-infrarode gebied met hoge uitgangsvermogens en brede afstemmingsbereiken, maar worden momenteel afgestemd met behulp van externe, draaiende diffractieroosters. Deze roosters worden ofwel gecontroleerd door een mechanisch platform met een piezo-controller, ofwel gerealiseerd als MEMS-chip. Over de jaren heen zijn verschillende golfgeleiderplatformen naar voren geschoven als geschikte kandidaten voor mid-infrarode spectroscopie. Deze platformen bieden elks verschillende voordelen, zoals het silicium-op-isolatorplatform dat een breed scala aan functionaliteit aanbiedt en bovendien CMOS-compatibel is. Germanium gebaseerde golfgeleiderplatformen zijn optisch transparant voorbij de limiet van het silicium-op-isolatorplatform ($> 3.8\ \mu\mathrm{m}$) en kunnen licht geleiden met lage verliezen in het hele mid-infrarood. Vergeleken met andere op germanium gebaseerde platformen, zoals het gegradeerde-index-germaniumplatform, bieden germanium-op-silicium en germanium-op-silicium-op-isolator een hoger indexcontrast. Dit leidt tot relatief kleine bochtstralen (de minimale bochtstraal met laag verlies voor een volledig geëtste golfgeleider is $75\,\mu\mathrm{m}$) en daardoor compactere circuits. Germanium-op-silicium-op-isolator heeft een bedekte oxidelaag die verhindert dat warmte naar het silicium substraat wegzinkt. Hierdoor is thermische afstemming efficiënter op dit platform. In deze thesis zullen we de ontwikkeling van deze op germanium gebaseerde platformen bespreken, alsook de combinatie met kwantumcascadeversterkerchips om afstembare kwantumcascadelasers met externe caviteiten te vormen, zoals schematisch geïllustreerd wordt in Fig. 1.

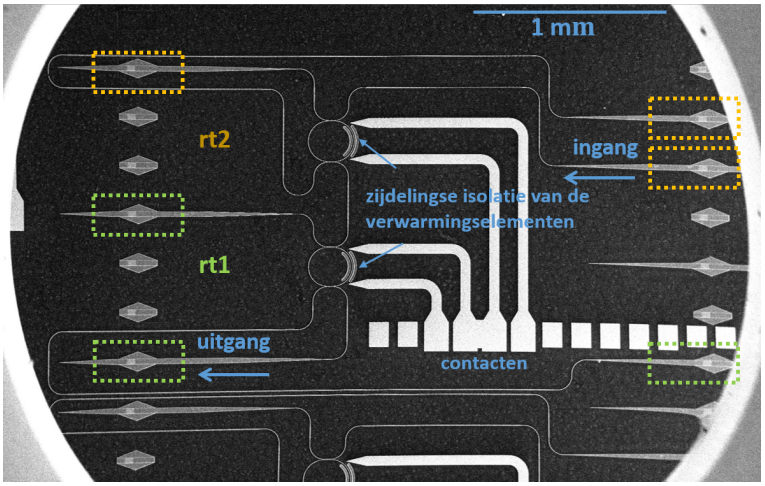


Figuur 1: Een versterkerchip wordt gekoppeld aan een externe caviteit op een germanium chip die gebruikt wordt om de werkingsgolflengte te kiezen en af te stemmen.

1 Fabricage van de Optische Circuits

Een processtroom werd ontwikkeld om de germanium-op-silicium- en germanium-op-silicium-op-isolatorcircuits te fabriceren. Dit wordt in detail beschreven in hoofdstuk 2. De fabricage begint met de epitaxiale groei van germanium op silicium- of silicium-op-isolatorwafers. De roosterconstantes van kristallijn germanium en silicium verschillen aanzienlijk, waardoor beide platformen defecten vertonen op het germanium-silicium grensvlak. Desondanks kunnen de verliezen die veroorzaakt worden door imperfecties op het grensvlak, geminimaliseerd worden door golfgeleiders en andere componenten zorgvuldig te ontwerpen. Vanwege zijn complexere lagenstapeling vertoont het germanium-op-silicium-op-isolator meer spanning, wat kan lijden tot barsten.

Afhankelijk van de kritische afmetingen van het circuit, werd contactlithografie of e-beamlithografie gebruikt in combinatie met een droog etsproces om de golfgeleiders te definiëren. Contactlithografie wordt verkozen voor grotere structuren, daar het een goedkoper en minder gevoelig proces is. E-beamlithografie biedt meer mogelijkheden voor het design, hoewel de maximale dikte van de elektrogevoelige lak kleiner is dan bij contactlithografie en bovendien beperkt wordt door de beoogde kritische afmeting. De dikte van de lak is een limiterende factor voor e-beamlithografie met twee stappen voor ons platform aangezien de bestaande topografie op de chip kan oplopen tot $1\,\mu\mathrm{m}$. Een combinatie van e-beam- en contactlithografie is nodig om de bestaande structuren op de chip efficient ervan te beschermen om weggeëtst te worden. Hoewel contact- en e-beamlithografie gebruikt worden voor de fabricage van testspecimens, moeten DUV lithografie en een droog-etsproces gebruikt worden om productie op waferniveau mogelijk te maken. Redelijke verliezen kunnen bekomen worden voor volledig en gedeeltelijk geëtste golfgeleiders met een DUV proces dat gebruikt wordt om een patroon te definiëren in een hard siliciumnitride masker, hetgeen voorts gebruikt wordt om

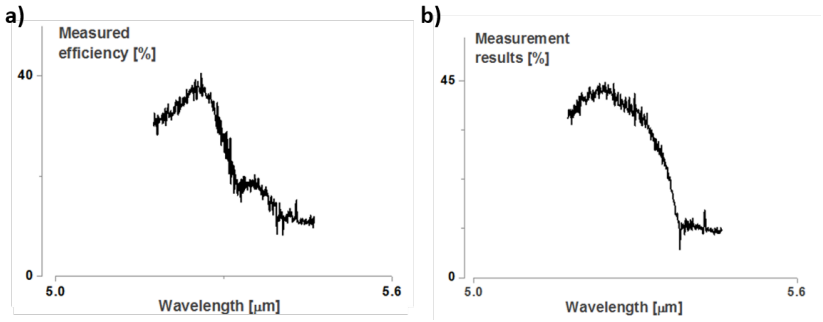


Figuur 2: SEM-afbeelding in bovenaanzicht van een thermisch afstembare Vernier renbaanresonator, geïmplementeerd op het germanium-op-SOI-platform.

het patroon over te zetten in de germaniumlaag. Voor de thermisch afgestemde circuits worden metalen verwarmingselementen gedeponeerd langs de golfgeleiders. Afhankelijk van de toepassing kan een bovencladding gedeponeerd worden zonder weinig bijkomende verliezen te introduceren. Tenslotte wordt de chip verdund tot een dikte die geschikt is om de chip te klieven, waarna een antireflectielaag gedeponeerd wordt. Simulaties die rekening hielden met imperfecties in de fabricage, zoals variaties in de dikte en de brekingsindex van de laag, duiden aan dat een antireflectielaag met parasitaire reflecties kleiner dan enkele procenten kan bekomen worden. Een voorbeeld van een gerealiseerd golfgeleider circuit wordt getoond in Fig. 2. Het circuit bevat mid-infrarode renbaanresonatorfilters en micro-verwarmingselementen om deze af te stemmen. Roostekoppelaars worden gebruikt als testpoorten. Om de invloed van de beperkingen van de e-beamfabricage te minimaliseren, worden monomodale golfgeleiders lokaal verbreed to multimodale golfgeleiders, zodat de stikselrand van het schrijfveld van de e-beam terecht komt op het bredere deel van de golfgeleiders.

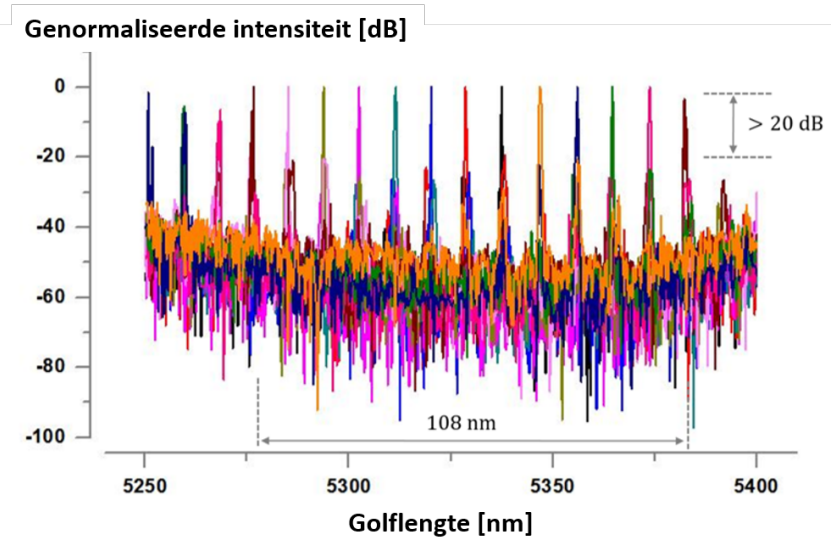
2 Simulaties and Karakterisatie

Een aantal componenten werden gesimuleerd en gekarakteriseerd: roosterkoppelaars, AWGs, gedistribueerde Bragg-reflectoren (DBR), multimode interferometers, Mach-Zehnder interferometers en renbaanresonatoren. Dit wordt voorgesteld in hoofdstukken 3, 4 en 5. Voor de karakterisatie werden verscheidene opstellingen gebouwd voor zowel facet- als roosterkoppeling. De opstelling bevat een lichtbron (ofwel een commercieel verkrijgbare QCL ofwel een kwantumcascadeversterkerchip), een polarisatiecontroller, een optische hakker om een continugolf-



Figuur 3: Roosterkoppelaars gerealiseerd rond 5.2 μm*: opgemeten koppelingsefficiëntie op germanium-op-silicium (a) en germanium-op-silicium-op-isolator (b).*

signaal in een gepulseerd signaal om te zetten, een FTIR voor spectrale analyse die eveneens kan gebruikt worden als golfmeter, optische vezels en detectoren (thermische en IbSb gekoeld met vloeibaar stikstof, in combinatie met een lock-in-versterker). De beste gedemonstreerde roosterkoppelaar heeft een maximale koppelingsefficiëntie van -3.5 dB en een halfvermogenbandbreedte van 220 nm rond 5.2 μm (Fig. 3). De propagatieverliezen in volledig en gedeeltelijk geëtste monomodale golfgeleiders zijn 3-5.5 dB/cm in het golflengtegebied rond 5 μm en het wordt aangetoond dat de insertieverliezen van de meeste componenten redelijk laag zijn. Hoewel de bochtstraal een beperkende factor is bij het design van circuits met een kleine voetafdruk, kunnen monomodale golfgeleiders verbreed worden tot multimodale golfgeleiders in rechte stukken om de totale propagatieverliezen in een circuit te verkleinen. De redelijk lage propagatieverliezen laten ons toe om deze apparaten te combineren tot optische filters gebaseerd op bemonsterde roosters, Mach-Zehnder interferometers of renbaanresonatorfilters. Filters gebaseerd op bemonsterede roosters kunnen een groot afstembereik ondersteunen met een goede onderdrukking van de zijmodes. Deze structuren zijn echter lang en vergen meer thermisch vermogen voor de afstemming in vergelijking met andere oplossingen. Mach-Zehnder interferometers hebben een zwakker golflengteselectie, met het voordeel van minder veeleisende fabricage vanwege de afmetingen van de onderdelen van deze structuren. Circuits gebaseerd op renbaanresonators bieden een golflengte-onderscheidingsvermogen dat een monomodale werking van een QCL mogelijk maakt, wat van hen de beste keuze maakt bij het bouwen van een optische filter voor golflengteselectie van een QCL. Meer geavanceerde filters zoals renbaanresonatorfilters worden aangetoond met een afstembereik van meer dan 100 nm en een onderdrukking van de zijmodes van $>$20 dB (Fig. 4). Dit type filter kan tevens een afstembereik van meer dan 425 nm hebben, ten koste van een beperkte onderdrukking van de zijmodes van slechts 3-4 dB. Het doel van het bouwen van thermisch afstembare filters is om kwantumcascadelasers met externe caviteiten te bouwen waarvan de golflengteselectie en -afstemming gerealiseerd worden in chipformaat, zoals getoond wordt in Fig. 5 voor een DBR filter op

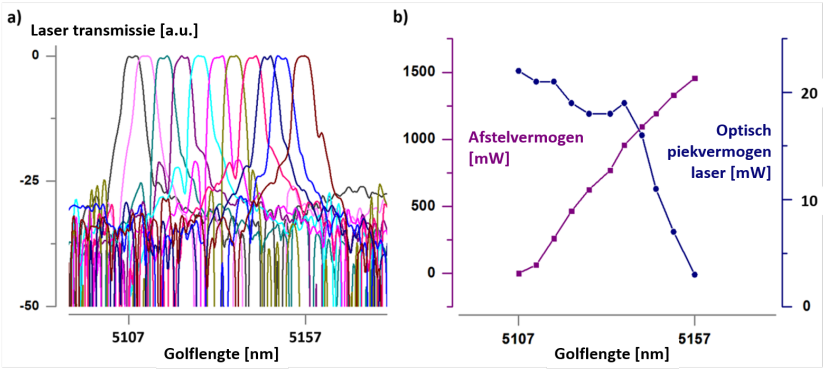


Figuur 4: Gekarakteriseerd Vernier renbaanfilter.

een germanium-op-silicium-op-isolatorplatform. Hoewel CW-operatie meer vermogen zou voorzien, wat goed is voor detectie toepassingen, werkt onze QCL met externe caviteit in een gepulseerd regime, wat hem minder vatbaar maakt voor thermische instabiliteit aangezien minder warmte geproduceerd wordt in vergelijking met CW-operatie van de versterkerchip.

3 Conclusie

Op germanium gebaseerde golfgeleiderplatformen tonen groot potentieel voor spectroscopie in het mid-infrarood, gebaseerd op fotonische integratie. Veel functionaliteiten van germanium circuits werden aangetoond in deze thesis, alsook the golflengteselectie van een kwantumcascadelaser met externe caviteit - proof-of-principle QCL met externe caviteit gebaseerd op een QC versterkerchip, facetgekoppeld aan een germanium-op-silicium-op-isolator DBR. Hoewel er zeker ruimte voor verbetering is in termen van de prestatie van het apparaat, en de huidige demonstratie nog twee chips bevat, geloven wij dat de resultaten die we tonen kunnen leiden tot de verwezenlijking van draagbare lasermodules of volledige spectroscopische systemen die opereren in het mid-infrarode golflengtegebied, allemaal geïntegreerd op germanium-op-silicium en germanium-op-silicium-op-isolator golfgeleiderplatformen.



Figuur 5: DBR filter gekoppeld via het facet aan een quantumcascadeversterkerchip. De centrale golflengte kan worden afgestemd over 50 nm in gepulseerde werking.

English summary

Mid-infrared spectroscopy promises more sensitive and easier differentiating sensors which rely on the fingerprint absorption lines of molecules in the mid-infrared band to detect the molecules qualitatively and quantitatively. Nevertheless, bulky and expensive equipment such as cooled mid-infrared detectors and light sources are required for conventional systems, which retains these sensors to a laboratory environment. One step forward in creating miniaturized mid-infrared sensors is laser integration with CMOS compatible platforms. Quantum cascade lasers operate over the entire mid-infrared region with high output power and large tuning range, but are currently tuned by an external rotating grating, either controlled by a mechanical stage with a piezo controller or realized as a MEMS chip. Over the years, different waveguide platforms emerged as candidates for mid-infrared spectroscopy. These platforms have different advantages, such as Silicon-on-Insulator which offers a wide range of functionalities and CMOS compatibility. Germanium-based waveguide platforms are optically transparent beyond the limits of Silicon-on-Insulator (> 3.8 μm) and can guide light with low losses in the entire mid-infrared. Comparing to other Germanium-based platforms, such as the graded-index Germanium platform, Germanium-on-Silicon and Germanium-on-Silicon-on-Insulator offer a higher index contrast which results in a relatively low bending radius (the minimal low-loss bend radius for a fully etched waveguide is 75 μm) and therefore, more compact circuits. Germanium-on-Silicon-on-insulator has a buried oxide layer which prevents the heat from sinking into the Silicon substrate. This makes thermal tuning on this platform more efficient. In this work we will discuss the development of these Germanium-based platforms and the combination with quantum cascade gain chips to form external-cavity quantum cascade tunable lasers, as schematically illustrated in Fig. 1.11.

4 Circuit Fabrication

A process flow was developed to fabricate the Germanium-on-Silicon and Germanium-on-Silicon-on-Insulator circuits, which is described in detail in Chapter 2. The fabrication begins by epitaxial growth of Germanium on Silicon or Silicon-on-Insulator wafers. The crystalline structure constant of Germanium and Silicon differ significantly, hence both platforms exhibit defects on the Germanium-Silicon interface. Nevertheless, by carefully designing waveguides and other components, it is possible to minimize losses caused by interface imperfections. Due to its more

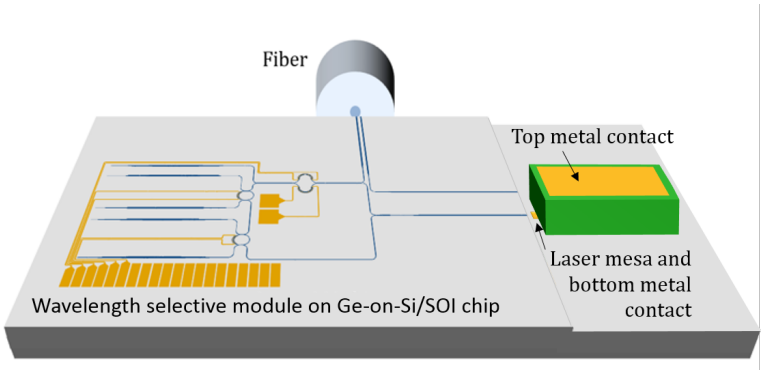


Figure 6: A gain chip is coupled to an external cavity on a Germanium chip which is used to select and tune the operating wavelength.

complex layer stack, the Germanium-on-Silicon-on-insulator platform shows more stress, which can lead to cracks.

Depending on the critical dimensions of the circuit, contact lithography or e-beam lithography in combination with dry etching is used to define waveguides. Contact lithography is preferred for larger structures, as it is a cheaper and less sensitive process. E-beam lithography offers more possibilities for the design, although the maximal resist thickness is lower than for contact litography and furthermore it is limited by the targeted critical dimension. The resist thickness is a limiting factor for two-step e-beam lithography for our platform since the existing topography on the chip can be as high as 1 μm. A combination of e-beam and contact lithography is needed to efficiently protect the existing structures on the chip from being etched away. Although contact and e-beam lithography are used for sample-size fabrication, to enable wafer-level production, DUV lithography and a dry etching process have to be used. Reasonable losses for fully and partially etched waveguides can be achieved with a DUV process used to pattern a Silicon-nitride hard mask, which is further used to pattern the Germanium layer. For the thermally tuned circuits, metal heaters are deposited along the heated waveguides. Depending on the application, a top cladding can be deposited, introducing low additional losses. Finally, the chip is thinned down to a thickness appropriate for cleaving, after which an anti-reflection coating is deposited. Simulations performed taking into account fabrication imperfections such as layer thickness and refractive index variation, show that an anti-reflection coating with parasitic reflections lower than a couple of percent can be achieved. An example of a realized waveguide circuit is shown in Fig. 7, comprising midIR racetrack resonator filters and micro-heaters to tune these. Grating couplers are used as test-ports. To minimize influence of e-beam fabrication limitations, single-mode waveguides are locally tapered up to multi-mode waveguides, such that the write-field stitching borders land on the wider part of the waveguides.

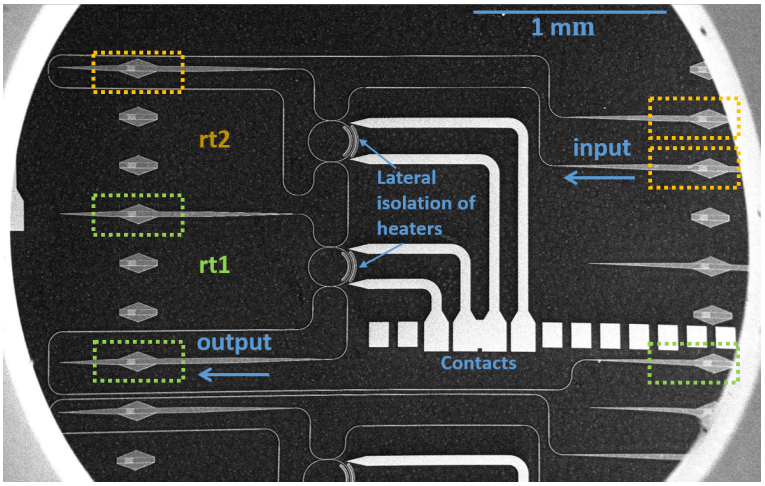


Figure 7: Top-view SEM of thermally tunable Vernier racetrack resonators implemented on the Germanium-on-SOI platform.

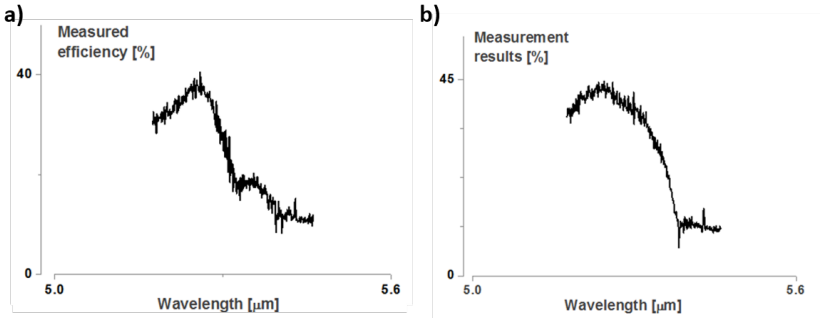


Figure 8: Grating couplers realized around 5.2 μm*: Germanium-on-Silicon (a) and Germanium-on-Silicon-on-Insulator (b) measured coupling efficiency.*

5 Simulations and Characterization

A number of devices has been simulated and characterized, which is presented in Chapters 3, 4 and 5: grating couplers, arrayed waveguide gratings, distributed Bragg reflectors (DBRs), multi-mode interferometers, Mach-Zehnder interferometers and racetrack resonators. For the characterization, various setups were built for both facet and grating coupler test ports. The setup includes a light source (either a commercially available QCL or a QC gain chip), a polarization controller, a chopper to turn CW into pulsed signal if needed, a FTIR for spectral analysis which can also be used as a wavemeter, optical fibers and detectors (thermal and liquid nitrogen cooled IbSb in combination with a lock-in amplifier). The best grating coupler

is demonstrated with -3.5 dB peak coupling efficiency and a 3 dB bandwidth of 220 nm around 5.2 μm wavelength (Fig. 8). Propagation losses in fully and partially etched single-mode waveguides are 3-5.5 dB/cm in the 5 μm wavelength range, and it is shown that the insertion losses in most devices are reasonably low. Although bending radius is a limiting factor when designing small footprint circuits, single-mode waveguides can be tapered to multi-mode waveguides in straight sections to reduce total propagation losses in a circuit. Reasonably low losses allowed us to combine these devices into optical filters based on sampled gratings, Mach-Zehnder interferometers or racetrack resonators. Filters based on sampled gratings can support large tuning range and good side-mode suppression. However, these structures are long and demand more thermal power for tuning comparing to other solutions. Mach-Zehnder interferometers have poor wavelength selection with an advantage of less demanding fabrication due to the feature size of these structures. Circuits based on racetrack resonators offer wavelength discrimination which can enable single-mode operation of a QCL which makes them the best choice when building an optical filter for QCL wavelength selection. More advanced filters such as Vernier racetracks are demonstrated with over 100 nm of tuning range with $>$20 dB of side mode suppression (Fig. 9). This type of filter can also achieve over 425 nm tuning range at the expense of only 3-4 dB of side mode suppression. The aim of building thermally tunable filters is to build external cavity quantum cascade lasers where the wavelength selection and tuning is realized in a chip form, as shown in Fig. 10 for a DBR filter on Germanium-on-Silicon-on-Insulator platform. Although CW operation would provide more power which is beneficial for the sensing applications, our external-cavity QCL operates in pulsed regime which makes it less prone to thermal instabilities as less heat is produced comparing to CW operation of the gain chip.

6 Conclusion

Germanium-based waveguide platforms show great potential for mid-infrared spectroscopy applications based on photonic integration. Many functionalities of Germanium circuits with reasonably low losses have been demonstrated in this work, as well as the wavelength selection of an external cavity quantum cascade laser - a proof-of-principle external cavity QCL based on a QC gain chip butt coupled to a Germanium-on-Silicon-on-Insulator DBR. While there is definitely room for improvement in terms of device performance and the current demonstration relies on two separate chips, we believe that the results that we showed can lead to realization of hand-held laser modules or complete spectroscopic systems operating in the mid-infrared wavelength range, all integrated by means of flip-chip on Germanium-on-Silicon and Germanium-on-Silicon-on-Insulator waveguide platforms.

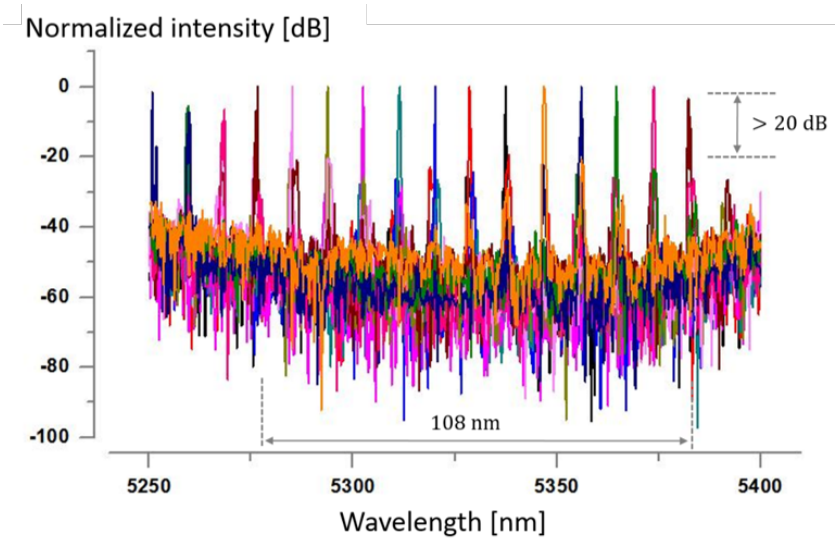


Figure 9: Characterized Vernier racetracks filter.

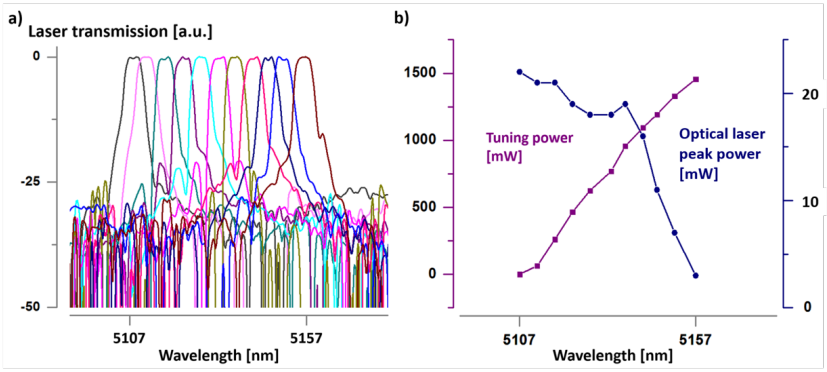


Figure 10: DBR filter butt-coupled to a quantum cascade gain chip. The central wavelength is tuned over 50 nm in pulsed operation.

1 Introduction

1.1 Mid-infrared Spectroscopy

The mid-infrared spectral region, from 2-14 µm (Fig. 1.1), also referred to as the fingerprint region, allows to probe fundamental absorption bands of molecules. The fingerprint region corresponds to the vibrational and rotational transitions and it is orders of magnitude stronger than the overtone and combination band in the near-infrared (Fig. 1.2), resulting in both highly selective and highly sensitive identification of chemicals. In addition, molecular spectra in the mid-infrared are less densely arranged, allowing for selective spectroscopic detection of a large

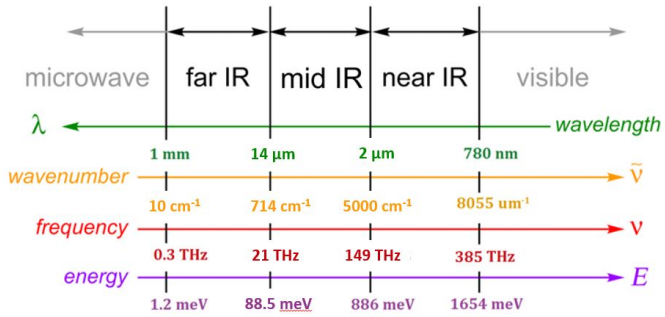


Figure 1.1: Mid-infrared wavelength range from 2 - 14 µm *on the electro-magnetic waves scale.*

number of molecules, while near-infrared and visible spectra in general consist of overlapping bands that may be difficult to resolve.

The vibrational and rotational transitions are specific to species in the gas, liquid and solid phase [1]. Spectroscopy in the mid-infrared wavelength region allows to detect many important gas molecules, such as carbon dioxide, methane, carbon monoxide, hydrogen chloride, hydrogen fluoride, nitrogen dioxide, sulfur dioxide, hydrogen peroxide etc. For example, CO has absorption bands near 1.55 μm [2], 2.3 μm [3] and 4.6 μm [4], which offer possibilities to detect very low concentrations of CO, with the strongest absorption coefficient at 4.6 μm. In fact, a multitude of molecules present strong and distinct absorption lines in the mid-infrared giving much interest for spectroscopic detection [5]. Detection of ammonia, benzene and several other greenhouse and dangerous industrial gases has been demonstrated in the mid-infrared [6].

A spectroscopic system can be realized in two ways (Fig. 1.3). The system shown in Fig. 1.3a) uses a broadband light source, which in return requires a spectrometer to distinguish between different wavelengths. Another option is to use a widely tunable, single-mode laser (Fig. 1.3b). Free-space spectrometers are bulky and expensive, while the resolution of an on-chip integrated spectrometer is a limiting factor for gas sensing [7]. Due to its lower wavelength discrimination, the broadband source scheme with a spectrometer is suited for solid and liquid analytes, while many applications, including chemical imaging and remote or photoacoustic gas sensing, prefer single-mode laser sources. To improve the detection sensitivity, various types of modulation spectroscopy have been developed, in which the wavelength of the diode laser is modulated while being scanned across an absorption line [8].

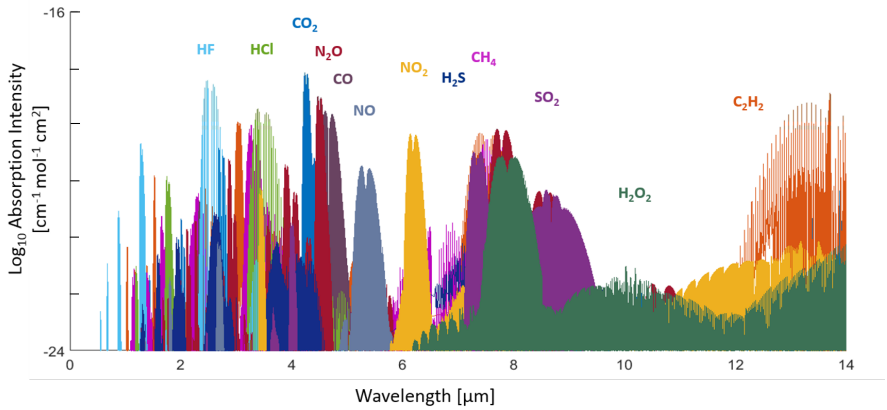


Figure 1.2: The absorption of many gasses is orders of magnitude stronger in the mid-infrared compared to the near-infrared and visible wavelength region.

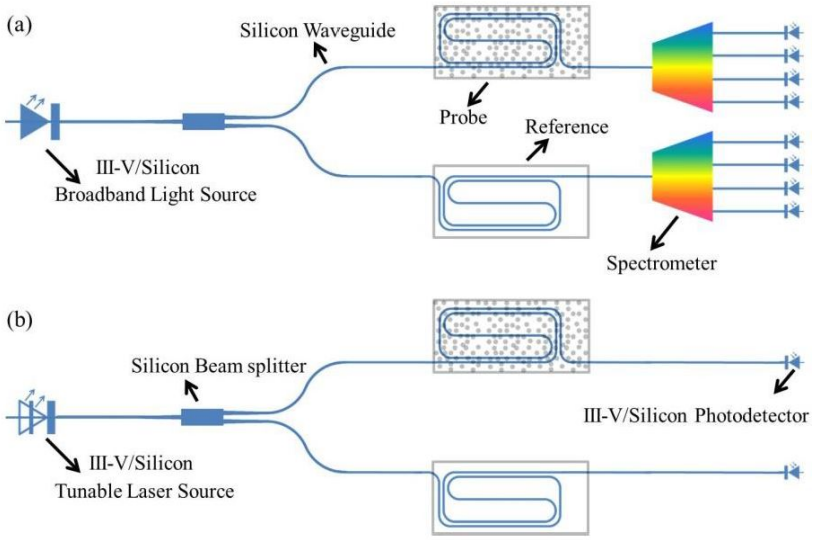


Figure 1.3: Light from a broadband source is split into two arms, a reference and a sensing arm, after which the difference in the signal vs. wavelength is recorded by a spectrometer (a). Tunable single mode laser source for trace gas detection (b) [3].

Mid-infrared sensing includes a number of spectroscopic techniques, predominantly based on absorption spectroscopy. However, beside a few commercialized sensors, most mid-infrared sensing techniques remain confined to a laboratory environment. The tunable laser sources are often based on rotating and translating a discrete grating, which makes these systems cumbersome and complex to build. Hence the need for on-chip mid-infrared spectroscopic sensing systems. In recent years, silicon photonics has attracted great interest in the field of spectroscopic sensing since well-established fabrication technologies and CMOS-compatible waveguide platforms on planar Si substrates offer a promising solution to realize low-cost and miniature optical sensors. With the progress in integrated silicon photonics technology and the recent development of efficient inter-band cascade lasers (ICL) [9] and quantum cascade lasers (QCL) [10], there is an opportunity to investigate new types of integrated gas sensors.

1.2 Mid-infrared Sources

To realize an efficient gas sensor, a single-mode light source with high spectral purity is required. Optical parametric oscillators (OPOs) or single-mode lasers fulfill this requirement. OPOs use a nonlinear crystal to convert the output of a pump laser to a shorter (signal) or longer (idler) wavelength. Nevertheless, OPOs are

complex devices and will require further improvements before they are practical for widespread deployment. Another disadvantage of OPOs for handheld applications is the need for a high-power pump laser. On the other hand, semiconductor lasers are coherent light emitters and are already widely deployed in various applications such as datacom, telecom, data storage etc.

The development of III-V quantum well lasers in the telecom wavelength range (around 1550 nm) has been supported by the strong interest in optical communication applications. Therefore the fabrication methods, such as molecular beam epitaxy and metal organic chemical vapor deposition, have been continuously improved in order to grow high quality III-V quantum well stacks. The development of semiconductor lasers operating beyond 2 μm wavelength at room temperature has, however, proved to be challenging. Gallium antimony (GaSb) based material combinations allowed to extend diode lasers to about 3 μm wavelength. In the wavelength region from 3-6 μm, interband cascade lasers (ICLs) replace the diode lasers, while room-temperature-operating quantum cascade lasers (QCLs) partially overlap with the ICLs and cover the rest of the mid-infrared region (4-14 μm).

1.2.1 InP and GaSb Diode Lasers

By properly designing the quantum well structure, indium phosphide (InP) based laser diodes can be made to operate in continuous-wave (CW) regime at room temperature up to 2.3 μm wavelength [11]. For longer wavelengths, the Al-content in the quantum wells should be reduced and In-content increased. This leads to a narrower band gap, at the cost of higher compressive stain in the layers. The high strain degrades the gain material and limits the operation of these structures to 2.3 μm [12]. This limitation led to the investigation of other III-V materials for emission in the mid-infrared part of the spectrum. The first GaSb-based laser was demonstrated in 1985 [13, 14]. A DFB laser array with central wavelength ranging from 1.8 μm up to 3 μm wavelength operating in CW at room temperature has recently been reported in this promising material system [15].

1.2.2 Interband Cascade Laser

ICLs are based on band-to-band (interband) transitions. The photons are produced from the transition between the electron state in the conduction band and the hole state in the valence band in a Sb-based type-II quantum well. The concept was first proposed by R. Q. Yang in 1995 [16]. The first experimental demonstration of an ICL (= 3.8 μm) was reported in 1997 [17]. In 2008, the first ICL operating in CW at room temperature, emitting at 3.75 μm was demonstrated [18]. Later, light generation in CW operation at room temperature has been shown in the 3-6 μm wavelength range [19, 20].

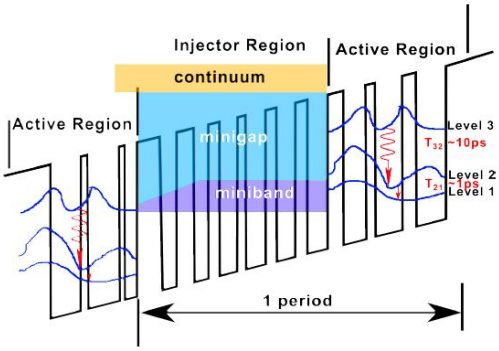


Figure 1.4: Schematic diagram explaining the working principle of a quantum cascade laser relying on intersubband transitions [22].

ICLs have the advantage that the band structure can be engineered and thus the emission wavelength can be tailored. Given that the transitions are interband, the loss arising from fast phonon scattering (as is typical in QCLs) is bypassed. Moreover, Auger recombination is reduced because of the type II nature of the transition. As a result of this, mid-infrared light generation is possible using ICLs with lower power consumption [21].

1.2.3 Quantum Cascade Laser

A QCL (Fig. 1.4) consists of a quantum well active region and an n-type electron injector region typically grown using molecular beam epitaxy (MBE). The injector region consists of several wells and barriers which create minibands separated by minigaps. When an electrical bias is applied, the electrons are injected from the ground state of a miniband to the uppermost level of the active region (denoted by level 3). Stimulated emission can therefore be obtained by the intersubband transition from level 3 to level 2. The electron then decays via phonon scattering to the ground level (denoted by level 1) of the active region from where it enters the miniband in the next stage via resonant tunneling. This process is repeated (cascaded) and another photon is emitted. A QCL typically contains 20 - 100 stages such that a substantial number of photons are generated per electron. As can be seen, the level 3 of the active region is not aligned with the miniband of the next stage and hence has a reasonably large lifetime (˜10 ps) and electron accumulation. Level 2 does not sustain population since decay to level 1 takes place via a fast non-radiative transition and subsequent tunneling towards the next miniband (˜1 ps).

There has been significant progress in both the design and the performance of QCLs in the last decades [23, 24]. Nowadays, achieving Watt-level output pow-

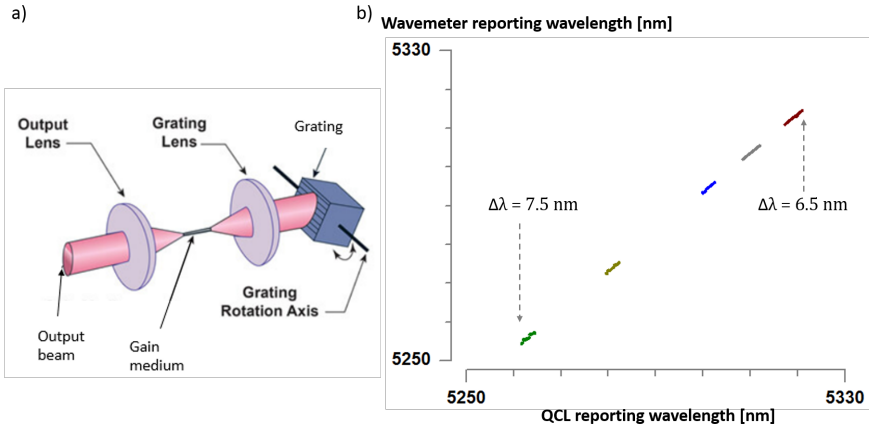


Figure 1.5: Tuning mechanism of the Daylight EC-QCL [35] (a). The wavelength selective element consists of a grating attached to a rotation stage which includes a piezo-translator to avoid mode hopping. (b) Due to misalignment, the wavelength reported by the QCL controller deviates from the actual wavelength measured in our laboratory

ers and single-mode operation is common [25, 26]. By tailoring the composition and the thickness of the active region layers, the peak wavelength at which the QCL lases is set. Both the active and the injector regions can be designed as a superlattice containing their own minibands and minigaps or by using the so-called bound-to-continuum scheme where lasing is achieved via a transition from a discrete upper state to a superlattice miniband [27]. Another design replaces the injector regions altogether and is based on the principle that the ground state of the active region gets aligned to the upper state of the next stage upon application of a suitable bias [28]. Due to the bound-state transitions, QCLs are transparent on both sides of the central frequency (i.e they exhibit a lorentzian gain spectrum) unlike traditional band-to-band semiconductor lasers which absorb all photons with energy larger than the band gap. Therefore, many different types of active regions can be cascaded together allowing either multi-wavelength lasing [29] or provide broadband gain [30, 31]. Due to the quantum mechanical selection rules, QCLs emit light with a polarization perpendicular to the layer structure (transverse magnetic (TM) polarization). The electrical field required to align the injector and the active regions are of the order of 50 kV/cm^{-1} ($>$ 0.5 V per stage), which results in a high bias voltage requirement. The high power consumption makes heat dissipation also an issue in QCLs and effective heat management is a key aspect of QCL design [32].

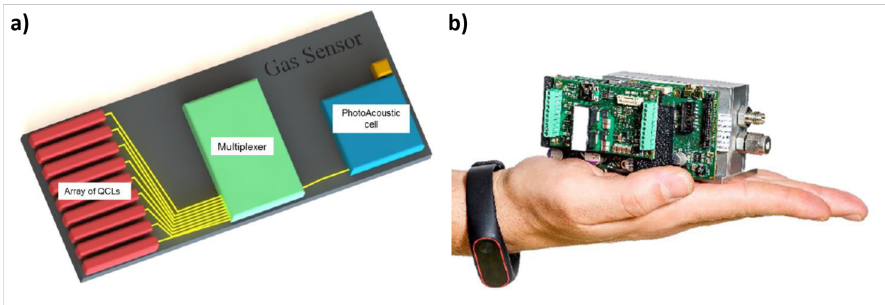


Figure 1.6: Architecture of the gas sensing system (a) and view of the multiSense product from mirSense (b) [36]. A QCL array is integrated to cover a wide range of wavelengths.

1.2.4 QCL Integration

The physics behind the operation of QC structures is beneficial for their operation as broadband gain medium. The most common approaches to achieve broadly tunable single-mode emission rely on the realization of external cavity (EC) configurations. Through the use of a grating as a tuning element, EC-QCLs can achieve broadband single-mode tuning [33]. A mid-infrared record tuning range of 40% around the central wavelength of 9.5 μm (7.6-11.4 μm wavelength range) has been demonstrated [34]. Commercially available for a number of years already, Daylight Solutions products, use EC gratings as the wavelength selective element (Fig. 1.5a). High-speed spectral scanning in a Littrow-type resonator is realized by employing a micro-opto-electro-mechanical-system (MOEMS) grating to select the wavelength [37]. The system configuration is shown in Fig. 1.7. Both macroscopic external gratings and MOEMS gratings are susceptible to misalignment. The wavelength shift due to misalignment, measured on the Daylight laser in Mode Hop Free - CW regime, is plotted in Fig. 1.5b). We notice a significant shift (˜6.5 - 7.5 nm) dependent on the wavelength.

For hand-held applications, it is essential to integrate QCL sources. Since QCLs are semiconductor lasers, arrays of single wavelength lasers can be realized on a single chip [38]. A tunable laser array, on an InP substrate, with a sampled grating distributed feedback and a beam combiner has been demonstrated in the wavelength range of 6.1 to 9.2 μm [39]. An array of 24 QCL distributed feedback (DFB) lasers on a single chip operating in 8.0-9.8 μm wavelength range operating in pulsed mode was realized [40]. Besides the research on broadband monolithic laser sources mostly undertaken by academia, a number of companies started their work on the application of these lasers as gas sensors. A portable gas sensor with an integrated QCL array (6.5-11 μm) was demonstrated [41]. Recently, the company MirSense revealed a multi-gas sensing system based on QCL sources assembled with a multiplexer and a photoacoustic cell (Fig. 1.6b). Although promising

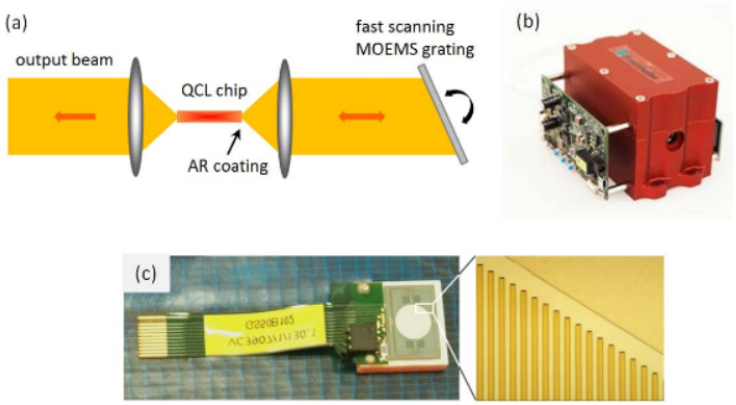


Figure 1.7: A MOEMS grating is used to tune the QCL chip (a). The package of the system (b) and the MOEMS scanner with etched grating (c) [37].

implementations based on a laser arrays have already been realized, this solution demands a multiplexer component that induces additional losses in the system. Since each laser operates in a narrow wavelength range, that differs from one laser to another in a laser array, this approach does not exploit the full potential of the gain of an individual laser. Also, due to maturity of CMOS technology, it makes sense to integrate the light source with a silicon-based platform. The first QCL that was heterogeneously integrated on a Si PIC, was demonstrated at 4.8 µm wavelength [42]. The device is based on molecular direct bonding technology and adiabatic coupling. The III-V epitaxial layers are bonded on top of a Silicon-on-Nitride-on-Insulator (SONOI) chip. However, since the SONOI platform has Si waveguides and nitride under-cladding, the operational range is limited to 6.7 µm. It is worth mentioning that a commonly used adhesive in the bonding technique starts to absorb heavily at wavelengths beyond 2 µm and makes for a poor heat sink [44], which gives advantage to flip-chip integration of QCLs where heat sinking is crucial to maintain operation.

The hybrid integration of a broadband III-V gain medium with CMOS-compatible, Si-based waveguide platforms could be used to implement chip-size laser modules without any moving parts, making it low-cost, compact and robust. Furthermore, the miniaturization and cost reduction of mid-infrared sensors could be extended to the implementation of the complete mid-infrared spectroscopic system on the same chip, where the gain chip is placed on the carrier chip, and the wavelength selective module, together with the sensing module, is implemented on the carrier platform. In the next section, we will discuss advantages and disadvantages of several attractive candidates for the carrier platform.

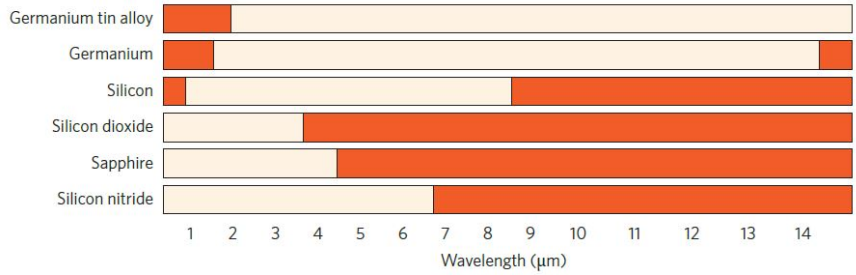


Figure 1.8: Optical transparency window of different candidate materials for mid-infrared integrated photonics platforms [43].

1.3 Silicon-based Waveguide Platforms for the Mid-infrared

In recent years, the wavelength range over which integrated photonics finds its applications has been extended to the mid-infrared region. Although the established and traditional waveguide platform for the telecom and datacom wavelength range, Silicon-on-insulator (SOI), found its way in mid-infrared photonics, it will not be suitable for covering the entire mid-infrared wavelength range. The reason lies in its optical transparency, which is graphically displayed in Fig. 1.8, together with that of other common materials in integrated photonics platforms. The SOI platform is limited to operation up to 3.8 μm due to the high absorption of the SiO_2 layer in the mid-infrared [45]. Hence, multiple silicon-based platforms, with clever solutions for the problem of SiO_2 absorption, have been explored for the implementation of mid-infrared photonic integrated circuits (PICs) beyond 3.8 μm, some of which will be discussed in this section.

1.3.1 SOI platforms for the mid-infrared

Due to its CMOS compatibility and maturity, the SOI platform has been widely explored in the mid-infrared wavelength region (Table 1.1), up to 3.8 μm [48] - a limitation imposed by the optical transparency window of silica. Another advantage is the compact circuit footprint and small bending radius, due to the large index contrast (n_{Si} = 3.42, n_{SiO_2} = 1.42). Apart from absorption, a source of loss in integrated waveguides is the leakage of the waveguide mode from the device layer, where the waveguides are implemented, to the Si substrate. A thick buried oxide (BOX) layer is required to prevent this leakage. A simulation of substrate leakage loss for SOI wafers used in integrated photonics (400 nm thick device Si layer, 2 μm thick BOX) as a function of wavelength [44] shows elevated losses beyond 3.5 μm. Besides the 400 nm thick device layer, other SOI platforms are

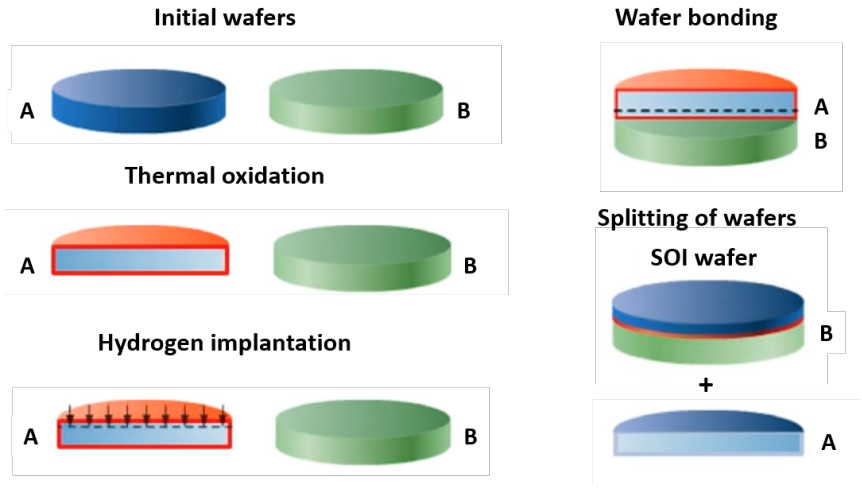


Figure 1.9: Fabrication process for the high device-layer-thickness-control of SOI wafers [52]. High-energy protons are implanted in the previously thermally oxidized wafer A. By controlling the proton kinetic energy, the thickness of the device layer is precisely and uniformly determined. Wafer A is then bonded to wafer B. After splitting over the line where the protons have been implanted, the SOI wafer is formed.

in use [45, 50]. The SOI wafers used in this application are made using SmartCut technology, which is explained in Fig. 1.9. The waveguide circuit is commonly formed by e-beam/deep UV (DUV) lithography followed by a dry etching process. One of the many advantages of the SOI platforms is that the techniques for heterogeneous integration with III-V materials are well established. This enables for example the implementation of light sources [3] and photodiodes [49, 51], enabling fully integrated spectroscopic sensing systems. Integrated mid-infrared spectroscopy has attracted the interest of the sensing industry, due to the possibility of developing low-cost and miniaturized devices, enabling their integration in existing equipment for on-line and in-situ monitoring of chemical species. These devices allow real-time and selective detection of several chemical compounds of interest [53].

1.3.2 Suspended Si Platform

While SiO_2 has a high absorption beyond 3.8 μm, bulk Si is considered to be transparent up to 8 μm. By locally removing the underlying SiO_2 layer to avoid high propagation losses, the standard SOI platform's wavelength operation range can therefore be extended. A number of functional devices has been demonstrated on the suspended Si-membrane platform (Table 1.2). The waveguide circuit is defined by e-beam/DUV lithography and dry etching. The removal of the SiO_2

Device	Wavelength [μm]	Characteristics
Waveguides [46]	2.1	Propagation loss $<$ 0.6 dB/cm
Waveguides [47]	3.39	Propagation loss of 0.6-0.7 dB/cm
Waveguides [48]	3.8	Propagation loss of 1.8 $\pm$ 0.2 dB/cm
MMI [48]	3.74	Insertion loss of 3.6 $\pm$ 0.2 dB
Add-drop ring resonator [48]	3.74	Q factor of 8200
MZI-based thermo-optic modulator [49]	2.3	π-shift of 50 mW
Add-drop ring resonator [48]	3.74	Q factor of 8200
TE grating coupler [46]	2.1	Coupling efficiency of 3.8 dB
TE grating coupler [50]	3.8	Coupling efficiency of -5 dB and 3 dB bandwidth 180 nm
TE AWG [51]	2 - 2.25	Insertion loss of 2.15 - 4 dB
TE AWG [50]	3.8	Insertion loss of 1.5 - 2.5 dB
TE PCG [51]	2.05 - 2.3	Insertion loss of 5 - 7 dB
TE PCG [50]	3.8	Insertion loss of 1.5 - 2.5 dB

Table 1.1: Silicon-on-Insulator: Demonstrated Devices

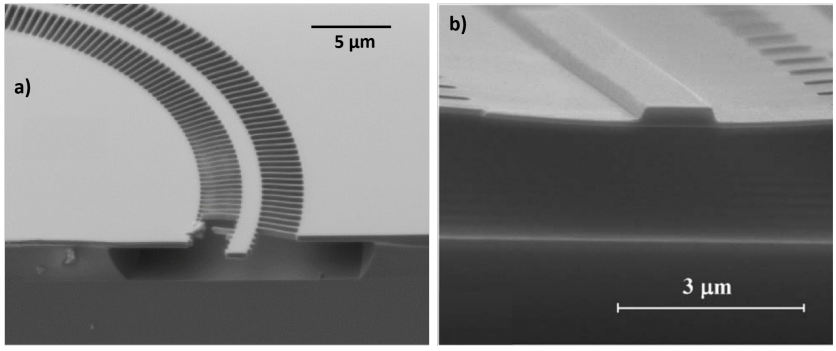


Figure 1.10: Fully-etched suspended waveguide [55] (a), and suspended ridge waveguide [57] (b).

layer is done by HF etching of the buried oxide (BOX) layer through holes in the Si device layer. The holes in the device layer are formed either at the same time as the waveguides [55], or after the circuit formation [57]. In the former case, the silicon strips used to suspend the waveguides are in direct contact with the guiding waveguide and hence their width has to be optimized to prevent the light from leaking into these structures (Fig. 1.10a). In the latter case the authors used ridge waveguides (Fig. 1.10b). The platform benefits from the possibility of small bend radii with low radiation losses [55] due to the high mode confinement as it is air-clad. One of the disadvantages of this platform is the difficulty to implement large-footprint devices such as arrayed waveguide gratings (AWGs) and planar concave gratings (PCGs). Another difficulty lies in fabrication as the free standing waveguides are prone to collapsing during the HF wet etch for the oxide removal. A possible solution could be to use vapor phase HF or critical point drying. Still, the platform remains theoretically transparent up to a wavelength of only 8 µm, and up to now - to our knowledge- no devices have been experimentally demonstrated beyond the wavelength of 5.2 µm.

1.3.3 Si-on-Sapphire

The Silicon-on-Sapphire (SOS) waveguide platform (Table 1.3) is another mid-infrared waveguide platform suitable for applications up to 5.6 µm wavelength [61]. This layer stack is sometimes used in the radio-frequency electronics industry to replace SOI. E-beam lithography and dry etching is used to define the waveguide circuit. SOS has the advantage of a low index substrate, which eliminates the issue of substrate leakage and enables compact circuits: a bend radius of 10 µm was used at 5.18 µm wavelength [59]. The biggest limitation of the SOS waveguide platform is its operational wavelength range which is limited by the transparency of the sapphire substrate: sapphire starts absorbing beyond 5.6 µm. Moreover,

Device	Wavelength [μm]	Characteristics
Ridge waveguides [54]	2.75	Propagation loss of 3.3 $\pm$ 0.6 dB/cm,
Waveguides and bends [55]	3.8	Propagation loss of 0.82 dB/cm and 0.014 dB/bend for 15.7 μm bend radius
2x2 MMI and MZI [55]	3.8	Insertion loss of 1.6 dB for the MMI and extinction ratio 15 dB for the MZI
All pass ring resonators [54]	2.75	Q-factor of 8100
All pass ring resonators [56]	3.4	Q-factor of 11000
All pass ring resonators [56]	5.2	Q-factor of 6800
TE [57] and TM grating coupler [58]	2.75	Coupling efficiency of -5.5 dB for TE; Coupling efficiency of -3 dB and 3 dB bandwidth of 50 nm for TM

Table 1.2: Suspended Si Platform: Demonstrated Devices

Device	Wavelength [μm]	Characteristics
Waveguides [59]	2.08	Propagation loss of 1.4 dB/cm
Waveguides [60]	4.5	Propagation loss of 4.3 ± 0.6 dB/cm
Waveguides [59]	5.18	Propagation loss of <2 dB/cm, 10 μm bend radius
Waveguides [61]	5.4 - 5.6	Propagation loss of 4.0 ± 0.7 dB/cm
TE slot waveguide [62]	3.4	Propagation loss of 11 dB/cm
Two-stage taper strip-to-slot waveguide mode converter [62]	3.4	Insertion loss of 0.13 dB
Add-drop ring resonator [63]	2.75	Q-factor of 11400 ± 800
All pass ring resonator [64]	4.3 - 4.6	Q-factor of 151000
Add-drop ring resonator [61]	5.45	Q-factor of 3000
Grating couplers [65]	2.75	Coupling efficiency of -4.9 dB for TE and -9.3 dB for TM
TE grating couplers [62]	3.4	Coupling efficiency of -5 dB

Table 1.3: Silicon-on-Sapphire Platform: Demonstrated Devices

typical Si device layers on SOS wafers have more defects and wafers are more expensive than the commercial SOI. Another challenge could be the realization of efficient thermo-optic modulators in this waveguide platform due to the high thermal conductivity of sapphire [63].

1.3.4 Germanium-on-Si and Germanium-on-SOI

Germanium (Ge) has low losses in the 2-14 μm wavelength range [43], which - together with its compatibility with standard CMOS/MEMS processes - makes it suitable for the implementation of mid-infrared PICs. Complementary to the SOI platform, Germanium-on-Silicon (Ge-on-Si) and Germanium-on-Silicon-on-Insulator (Ge-on-SOI) have emerged as platforms for sensing applications in mid-infrared, beyond the wavelength of 3.8 μm (Table. 1.4). Low losses (2.5 dB/cm) for single-mode waveguides on Ge-on-Si have been measured up to a wavelength of 7.5 μm but the platform became very lossy beyond 8 μm (>15 dB/cm) [70]. Another study showed losses <10 dB/cm for single-mode TE propagation between 9 - 11 μm wavelength, and from 9 - 10.5 μm wavelength for single-mode TM propa-

gation [71], which represents a current record in mid-infrared integrated photonics.

The Ge-on-Si platform benefits from a simple fabrication process and should provide a wider transparency window compared to the other silicon-based mid-IR platforms. Due to the width of the single-mode waveguide, it is possible to fabricate circuits by contact lithography, as well as e-beam. The details of fabrication will be elaborated in the next chapter. Unlike the Ge-on-Si platform, the Ge-on-SOI stack has an additional SiO_2 layer, which allows for more efficient integrated thermo-optic phase shifters [75]. The Si device layer in the SOI substrate of the Ge-on-SOI platform is thick enough to prevent overlap of the Ge waveguide mode with the underlaying oxide, hence the mode does not incur losses from the highly absorptive oxide above 3.8 μm wavelength. The fabrication of devices on this platform can also take advantage of the additional SiO_2 layer to under-etch parts of the PIC, such as to further improve the efficiency of the thermo-optic phase shifters.

1.3.5 Graded-index Silicon-Germanium Platform

Up to date, a number of devices has been demonstrated on the graded index Silicon-Germanium (SiGe) platform (Table. 1.5), including several basic devices for optical guiding such as S-Bend waveguides, Y-junctions, waveguide crossings, and symmetric and asymmetric evanescent couplers [76]. The waveguide circuits are defined by e-beam/contact lithography and dry etching. Due to the graded index nature of the platform, the waveguide profile could be optimized to provide single-mode propagation for a wide range of wavelengths, from 3 - 8 μm, which is at the same time the transparency window of the platform [77]. The graded-index SiGe buffer is optimized to minimize defects caused by the difference in lattice constants of Si and Ge. Low index contrast between guiding media and the substrate results in a large bending radius ($>$500 μm) and difficulty to achieve high efficiency grating couplers. To increase the compactness of the circuits, a similar platform based on step index SiGe has been developed [80]. An efficient locally free-standing TM grating coupler design together with a taper transitioning from the free-standing section to the standard SiGe platform has been proposed in [81].

1.3.6 This work

In this work, we primarily focus on showing 'proof of principle' QC gain chip tuning by an EC implemented on a Ge-on-Si chip (Fig. 1.11). The III-V gain chip integration is envisaged through flip-chip integration, which places the active layers upside down in a trench defined on the Ge-on-Si chip. The light from the gain chip is coupled to the wavelength-selective Ge-on-Si circuit which provides feedback to the gain chip. To ease the coupling between the two chips, AR coatings are applied on the facets of the chips. The light is then extracted from the Ge-on-Si chip and collected in an optical fiber. In the following chapters, the details of the

Device	Wavelength [μm]	Characteristics
Waveguides [66]	1.9 - 3.8	Propagation loss of 6 dB/cm at 1.9 μm, 3.5 dB/cm above 2.25 μm wavelength
Waveguides [67]	3.8	Propagation loss of 0.6 dB/cm
Partially-etched waveguides [68]	4.7	Propagation loss of 1 dB/cm,
TE and TM Waveguides [44]	5.15 - 5.45	Propagation loss of 3 dB/cm
TM waveguides [69]	5.8	Propagation loss 2.5 dB/cm,
TE partially-etched waveguides [70]	7.5-8.1	Propagation loss of 2.5 - 10 dB/cm,
TE waveguides [71]	9-11	Propagation loss $<$ 10 dB/cm,
TM waveguides [71]	9-10.5	Propagation loss $<$ 10 dB/cm,
MZI modulator [72]	1.95	Modulation efficiency ($V_\pi L_\pi$) of 2.68 V cm and 4 V DC reverse bias
MMI [67]	3.8	Insertion loss of 0.21 dB for 1x2 MMI and 0.31 for 2x2 MMI
MZI [44]	5.2 - 5.4	Insertion loss of 0.5 dB
MMI [70]	7.9	Insertion loss of 0.23 dB
Add-drop ring resonator and Vernier rings cascade [73]	3.8	Insertion loss of -1 dB and Q-factor of 1700 for th ring resonator. Q-factor of 5000 and insertion loss of -5 dB for Vernier rings cascade
AWG [68]	4.7	Insertion loss of 1.52 dB
TE and TM PCG [74]	5.2	Insertion loss of 4.9 dB for TE and 4.2 dB for TM

Table 1.4: Germanium-on-Si/SOI Platform: Demonstrated Devices

Device	Wavelength [μm]	Characteristics
Waveguides [76]	4.5	Propagation loss <1 dB/cm
Waveguides [76]	7.4	Propagation loss <1.5 dB/cm
Waveguides [76]	9.5	Propagation loss <2 dB/cm
Waveguides [77]	9.5	Propagation loss 3.5 dB/cm
AWG [78]	4.5	Insertion loss 5 dB
AWG [77]	8 - 9.5	Insertion loss >3 dB
Integrated FTIR [79]	5 - 8.5	

Table 1.5: Graded Index Silicon-Germanium Platform: Demonstrated Devices

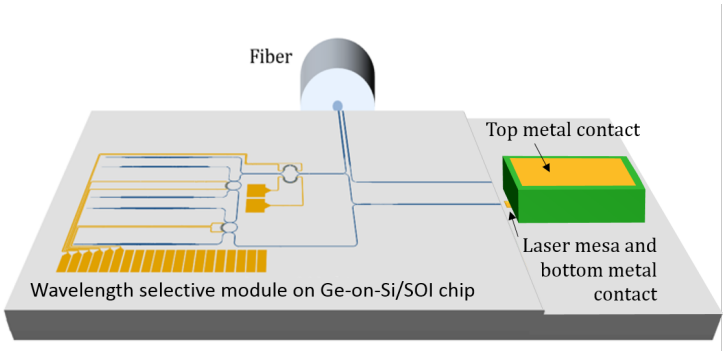


Figure 1.11: Flip-chip integration of the III-V gain chip with a Ge-on-Si EC chip.

proposed solution for the integration of a widely tunable, single-mode QCL on a CMOS-compatible platform without any moving parts, will be discussed.

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2

Development of Germanium-based Waveguide Platforms

2.1 Introduction

Over the course of this thesis, we worked on the development of Ge-on-Si and Ge-on-SOI waveguide platforms (Fig. 2.1). Germanium has a higher refractive index than Silicon and thus a waveguide can be constructed using these two materials, with Ge as the guiding medium. This chapter will elaborate on each step of the fabrication process, starting with the epitaxial growth of the Ge layer on Si and SOI substrates. Secondly, different options for the waveguide circuit definition (contact, deep ultraviolet (DUV) and e-beam lithography combined with matching wet/dry etching steps) are compared. Additionally, the top cladding is considered, together with different approaches for the implementation of heaters. Finally, anti-reflection (AR) coatings for efficient edge-coupling to and from the chips are discussed.

2.2 Epitaxial Growth of Germanium on Silicon and SOI

Germanium layers can be epitaxially grown on 200 mm Si/SOI (Silicon-on-Insulator) wafers. The quality of the epitaxial growth is determined by the defect density in the grown material. The defects start at the interface, predominantly caused by the

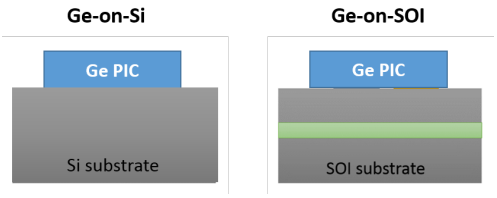

Figure 2.1: Germanium-on-Silicon and Germanium-on-Silicon-on-Insulator layer stack used as mid-infrared waveguide platforms.

lattice constant mismatch of the two materials. The difference in lattice constants of Ge and Si is 4.2 %. As a starting point of the process development, the quality of epitaxially grown Ge from imec and IQE was assessed. By comparing the propagation losses, it could be concluded that the quality of the epitaxial process from both suppliers is similar. Since the details of IQE's growth process were not disclosed, only the growth process of wafers grown by imec will be described in the following part.

2.2.1 Germanium-on-Silicon Wafers

For an integrated photonics platform, it is essential to reduce the light propagation losses as much as possible. Aside from optimization of the waveguide cross-section, it is also important to minimize intrinsic material losses. One of the contributors of intrinsic losses is free carrier absorption which is dependent on the doping level. Therefore, to ensure that the free carrier absorption losses are minimal, Si wafers with a low background n-type doping of 5x10^{14} cm^{-3} are chosen as substrates. The Germanium growth is carried out on these substrates at 450 °C by atmospheric chemical vapor deposition. GeH_4 is used as a Ge precursor gas. No intentional doping of the Ge layer was done. The lattice mismatch between Si and Ge introduces threading dislocations (TD) at the Si-Ge interface [2] which will cause absorption of light and hence increase waveguide loss. To reduce the number of defects, the wafers are annealed at 850 °C in a N_2 ambient for 3 minutes. At the high annealing temperatures, the atoms in the crystal lattice can start migrating. This migration is a thermally activated process and thus annealing reduces the density of dislocations in the lattice. The grown Ge film has a threading dislocation density (TDD) of 2 x 10^{10} cm^{-2} while the annealed film has TDD of 4 x 10^7 cm^{-2} [3].

Ge films with two different thicknesses (2 µm and 4 µm), grown on 200 mm Si wafers, were ordered from IQE. Ge films with a thickness of 2 µm on Si wafers were received from imec.

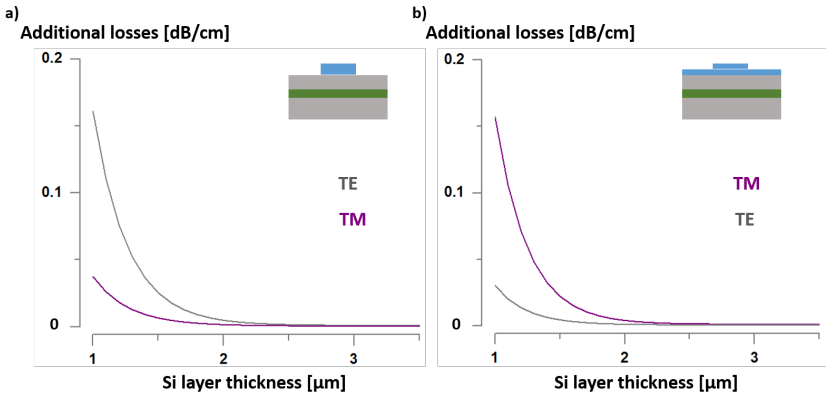

Figure 2.2: Simulation of the additional losses caused by the BOX layer in the substrate for fully (a) and partially etched Ge waveguides (b).

2.2.2 Ge-on-SOI Wafers

For the process development on the Ge-on-SOI platform, SmartCut SOI wafers from SOITEC were used. The high precision control of the device layer thickness, enabled by SmartCut technology is essential to achieve efficient grating couplers, which depend on the interference in the SOI substrate layers.

The Ge-on-SOI platform always had a 2 µm thick Ge layer. Given that SiO_2 absorbs heavily in the mid-infrared wavelength range, a thick Si layer is needed to prevent absorption losses caused by proximity of the BOX layer. From the beginning, we worked with a 3.2 µm thick silicon layer. Simulations show however that a 1.5 µm thick Si layer is also sufficient to avoid these losses for 2.2 µm wide fully etched and 3.25 µm wide 1 µm partially etched single-mode waveguides (Fig. 2.2). Simulation parameters for the SiO_2 layer are taken from [4]. As we will show later, loss measurements for the Ge waveguides are similar for both 1.5 µm and 3.2 µm silicon device layer SOI substrates.

Again, we had wafers prepared by two sources - imec and IQE. The IQE wafers started from 200 mm SOI wafers from Soitec with a 1.5 µm Si device layer thickness and 2 µm BOX. On some of them, 2 µm of Ge was directly grown (Ge-on-1.5 µm SOI). On the other wafers, 1.7 µm of Si was first grown, followed by 2 µm of Ge (Ge-on-3.2 µm SOI).

At the cleanrooms of imec, a Ge-on-3.2 µm SOI was fabricated. We began with 200 mm SOI wafers with 220 nm Si thickness on which an additional 3 µm of Si was then grown in a horizontal, cold wall, load lock reactor (ASMEpsilon 2000). The in-situ bake at 1050 °C removed all traces of oxygen. The Si layer was grown using dichlorosilane as Si precursor and H_2 as carrier gas.

Both IQE and imec used the same parameters to grow the Ge film on the SOI

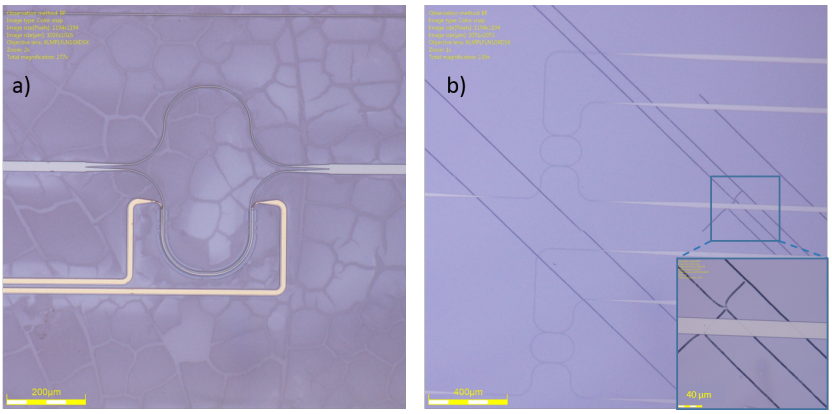

Figure 2.3: Cracks appearing in the SOI substrate of the Ge-on-SOI platform after a long HF etch to release structures (a) and to remove the metal mask after dry etching (b).

wafers as in the case of the Si substrate - the Ge epitaxy was not optimized further to adapt to our SOI substrate. Likely because of the Si growth on top of the SOI wafers and the unoptimized Ge growth for the Ge-on-SOI platform, these wafers are experiencing issues due to stress in the grown films when subjected to processing. In rare cases, after etching the Ge layer or after submerging in HF for more than 15 min (e.g. to release structures or to remove a remaining metal mask after etching), cracks would appear (Fig. 2.3).

2.3 Waveguide Circuit Definition

The fabrication flow of the Ge-on-Si/SOI waveguide circuit starts with the waveguide formation. The circuit can be defined by means of positive or negative lithography - where the defined pattern in the resist is transferred into the underlying layers during an etch step - or by means of inverse lithography to define a negative slope resist profile on which we deposit metal which then acts as a mask for etching. In the latter case, a lift-off process is needed to selectively remove the metal deposited on the resist pattern. Although the metal mask could be potentially used to etch thick layers, it is better to avoid the lift-off process, as it complicates the processing with an additional metal deposition step and it is not reliable for defining a waveguide circuit. The waveguide width is dependent on the resist development time, as underdeveloping will not open the resist effectively, while overdeveloping will make the waveguide wider. Also, there is risk of metal flakes redepositing on top of the waveguides and disturbing the waveguide pattern. In this section, three approaches to define the waveguides will be described: contact, e-beam and DUV lithography, each with its corresponding etching processes.

Contact lithography is a low-cost process that benefits from a resist thickness sufficient to etch the 2 μm Ge layer, but it is limited in the size of features that can be precisely defined. The theoretical resolution limit is estimated to $\sim$700 nm. However, the final structure dimensions will also depend on the resist thickness and the subsequent etching step. It can be used to fabricate waveguides, Mach-Zehnder interferometers (MZIs), arrayed waveguide gratings (AWGs) and flat-facet planar concave gratings (PCGs). Nevertheless, for low fabrication-tolerance components and components with smaller feature sizes, such as ring/racetrack resonators and gratings, e-beam and DUV are needed. Both of these high-resolution lithography techniques are used in combination with a metal mask, as their resists are too thin to support 2 μm deep etching. E-beam can be used to demonstrate devices and circuits, while DUV is commonly used in wafer-scale production. After the pattern definition step, a wet or dry etching step is used to transfer the pattern defined in the resist into the Ge layer.

2.3.1 Contact lithography and Wet/Dry Etching

Contact lithography is a process used to transfer patterns onto a sample in a 1:1 ratio. The process flow comprises three main steps: the spin-coating of a thin layer of a photo-resist, the UV illumination (i-line, 365 nm) through a glass mask with transparent/opaque chromium (Cr) patterns, and the developing. Sometimes, a primer layer (TI Prime) might be spin-coated on the sample prior to the spin-coating of the resist, to improve the resist's adhesion to the sample. We usually did not use the primer layer. The photo-resist is a type of polymer and is typically provided mixed with solvent to achieve a desired viscosity. The thickness of the resist is related to the spinning speed, while the acceleration influences the flatness of the polymer film (the right acceleration should reduce the accumulation of resist at the edges of the sample). To define waveguide circuits we use positive MIR 701 photo-resist, spin-coated in two steps to get a flat resist film: 2500 rpm for 30 s, followed by 3000 rpm spinning for another 30 s, all with 1000 rpm/s acceleration. The spinning at lower speed serves to spread the resist over the sample, while the second spinning step at higher speed defines the resist thickness. The resulting resist thickness is around 1040 nm. The spin-coated layer requires a baking step in order to evaporate the solvents and harden the resist. The temperature and baking time also have an influence on the final properties of the polymer layer and its behaviour under illumination. We used parameters recommended by the supplier here, 70 s at 100 °C. After the baking step, the polymer layer reabsorbs water molecules from the air. This is necessary for the chemical reaction taking place during illumination. For thin resist films ($\sim$1 μm) the water re-absorption takes 30-60 s. Upon illumination with UV light (the exposure), chemical reactions take place in the polymer layer causing the illuminated and non-illuminated parts

to have different behavior when in contact with the developing agent. The exposure time depends on the layer stack under the resist, as there is no anti-reflection coating applied. For our Ge platforms the optimal exposure time is 90 s. After illumination, the polymer layer contains high amounts of nitrogen gas (N_2), which is why it is necessary to wait some time for the gasses to evaporate. For a thin polymer layer ($\sim$1 μm) 1-2 min is enough to proceed to the subsequent baking step. Next, the sample is baked in order for the resist to cross-link. The UV dose and baking parameters will influence side-wall roughness of the waveguides after dry etching. The development of the sample is done using the appropriate solvent, in our case this is a solution of MIF 726 and water mixed in a 2:1 ratio, which will remove the non-cross-linked regions of the exposed MIR 701 resist. For a correct sample development, a continuous flow of the liquid has to be provided e.g. by slowly moving the sample. After the optimized developing time, which is around 80 s in our process, the chemical reaction has to be interrupted by cleaning the sample with the appropriated liquid e.g. de-ionized water. This step also helps to completely remove the non-cross-linked areas. The development time will strongly influence the pattern size, as well as the side-walls of the resist mask. Depending on the photo-resist and the goal of the lithography, a last baking step may be desirable to ensure complete solvent removal and to further improve the adhesion. If the lithography is used to define waveguides, this step is normally skipped, because it might cause resist shrinking and deteriorate the straightness of the resist side-walls.

To transfer the pattern from the resist mask to the sample, wet or dry etching can be used. Ge can be etched by KOH, piranha, SC_1, SC_2 and solutions containing peroxide (H_2O_2) and water (H_2O). Peroxide oxidizes Ge and turns it into GeO_x, an oxide soluble in water. The oxidation cannot progress unless there is a sufficient percentage of water in the solution - for lower etching rates the peroxide concentration has to be increased. For a 30$\%$ peroxide concentration in a peroxide-water solution, the etching rate of the Ge layer on the Ge-on-Si platform is 60 nm/min, while on the Ge-on-3.2 SOI platform the rate is 100 nm/min. The etching rate is constant over time, in both cases. The difference is etch rate is attributed to the lower quality of the Ge layer in the Ge-on-3.2 μm SOI platform. Fig. 2.4 shows a waveguide fully etched in CF_4/O_2 RIE plasma using a 10 nm Ti / 100 nm Cr metal mask [2], dipped in an HF solution, and wet etched in a 30$\%$ H_2O_2 solution for 30 - 300 s. Etching longer in peroxide solution improves sidewall roughness with the drawback of narrowing the structures. A cross-section of the 300 s etched sample shows a step in the Si substrate (Fig. 2.4h) - Ge wet etching by H_2O_2 is highly selective with respect to Si due to a thin layer of SiO_2 which forms on top of it. The peroxide etching forms clusters of GeO_x on the top Ge surface. To get a smooth Ge surface after the wet etching and remove these clusters, either a dip in an HF or buffered HF (BHF) solution or an annealing step

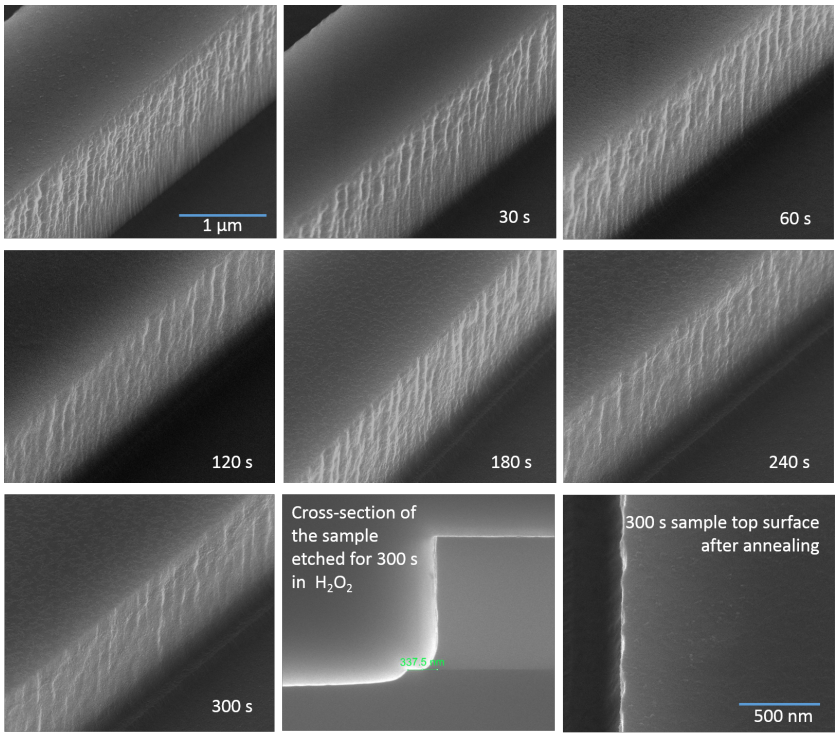

Figure 2.4: A Ge waveguide fully dry etched in CF_4/O_2 plasma using image reversal AZ5214 lithography, Ti/Cr metal mask and a lift-off process. The sample is etched in 30% H_2O_2 solution, for 30 - 300 s. The peroxide etching leaves clusters of GeO_x on the waveguide surface. Annealing at 350 - 550 °C evaporates residual oxide clusters and smoothens the waveguide surfaces.

can be done. We performed an annealing step by ramping the annealing temperature from 350 - 550 °C during 45 min in N_2 rich environment which made the Ge surface smooth - Fig. 2.4i). The side-wall roughness improves significantly after the 300s etch. However, the peroxide wet etching of Ge is highly isotropic, so parts of the Ge that were covered by the mask are still removed. This limits the circuit design, e.g the minimal gap in an evanescent coupler.

For transferring the pattern with minimal size offset from the resist mask to the target layer and to achieve 90°waveguide side-walls, it is best to apply a dry etching technique. Using dry etching, plasma removes the substrate materials. The parts of the layer we want to keep are protected by a mask. Usually, the polymer resist we used in lithography is thick enough to withstand the full etch of the target layer. This keeps the process flow more simple. Sometimes, the target layer - polymer etching ratio (the etch selectivity) is not high enough to allow to etch

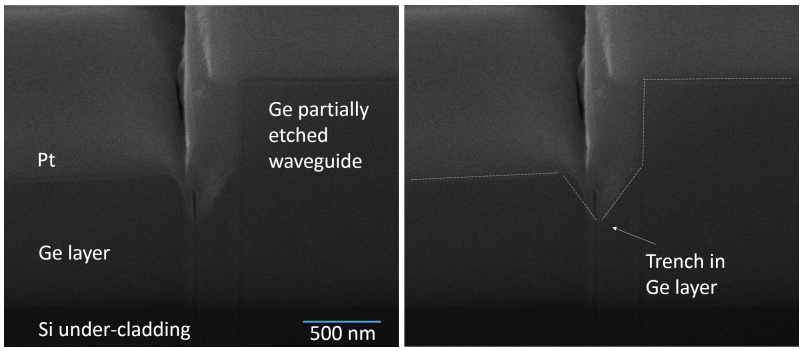

Figure 2.5: Trench effect formed in the high RF power RIE process, at 520 V, demonstrated on a partially etched Ge-on-Si chip. Platinum (Pt) is used to protect the top Ge surface during milling. On the left, the cross-section of the partially etched waveguide is shown. On the right a white dashed line is used to point out to the interface of Ge and Pt.

deep enough - the mask is completely etched away before the end of the etching process. In this case, we have to introduce more layers in the mask, such as silica or nitride masks, that are more resistant to the gases/plasma used to etch the target layer. The resist is then used to etch the first silica/nitride layer, which is used as a mask to etch deeper. Using more than two layers for the mask system may complicate the process flow and increase the cost of production. Additionally, using a complicated mask system can make the waveguide side-wall roughness worse, and can induce an offset in size of structures defined on the glass mask versus the target layer. Since we were not getting values of the Ge - oxide/nitride dry etching ratio higher than 0.5, we have focused on the search for an etching recipe using a 1 μm thick MIR 701 photo-resist mask.

Generally, dry-etching techniques are categorized as physical dry etching, chemical dry etching, or physicalchemical etching. In physical dry etching, high-energy particles (e.g. argon atoms) knock out substrates atoms from its surface which immediately evaporate after leaving the substrate surface. The main drawbacks are low etch rates, low selectivity, and trench effects (Fig. 2.5). The trench effect is visible around the edges of waveguides. It is caused by high-energy ions (high DC), reflected from vertical sides of the waveguides bombarding the horizontal surface next to them. Chemical dry etching uses a chemical reaction between the etchant gases and the substrate material to attack the substrate material. Gaseous reaction products are needed conditions for this etching concept because deposition of solid reaction products would protect the surface and stop the etching process. Chemical dry etching in plasma created in an RF field can be anisotropic and exhibits relatively high selectivity. Chemical dry etching is often used for cleaning wafers. For instance, photo-resist and other organic layers can be removed with

Parameter	s0	s1	s2	s3	s4	s5	s6	s7	s8	s9
CF_4 flow [sccm]	80	80	80	80	80	80	90	90	100	100
SF_6 flow [sccm]	3	3	3	3	3	3	3	3	3	3
H_2 flow [sccm]	12	12	12	7	7	7	7	12	7	12
DC bias [V]	520	420	320	520	420	320	420	420	420	420
pressure [mTorr]	20	20	20	20	20	20	20	20	20	20
Ge etch rate [nm/min]	42	27	13	115	97	78	115	31	115	37
resist etch rate [nm/min]	40	24	14	59	36	25	43	24	45	25
Ge - resist etch rate ratio	1.05	1.13	0.93	1.95	2.7	3.12	2.67	1.29	2.55	1.48

Table 2.1: Ge etching properties in $CF_4/SF_6/H_2$ plasma for small samples (0.5 x 0.5 cm)

oxygen (O_2) plasma.

Typically used physicalchemical etching mechanisms are reactive ion etching (RIE) and inductively coupled plasma (ICP) etching. Reactant gases are excited to ions in the RF field. Under low pressures and a strong electrical field, ions are directed to the substrate surface almost perpendicularly. Therefore, this method can achieve relatively high aspect ratios. The common problems of physicalchemical dry etching are mask erosion where the edges of the mask get damaged, undercutting where ions reflected from the bottom of the trench dig out the material under the mask, and the trenching effect where high-energy particles reflected from the vertical walls of the etched trench cause roughness in the bottom of the trench. During the dry-etching process , the trench side-walls should be protected to keep them parallel and to achieve high aspect ratios - the sidewall inhibitor deposition effect. Fluorine-containing molecules such as CF_4, SF_6, NF_3, and CHF_3 are normally employed for plasma-based dry etching of materials similar to silicon. Other gases such as O_2, Ar, and He can be added, e.g., for heat transfer, plasma stabilization, and enhanced ionization. Ar has a mechanical etching effect, which can induce more roughness on the side-walls. When used in combination with a resist mask, O_2 can burn the resist mask which is then hard to remove from the waveguides. Due to the reasons we mentioned, and the availability of gasses in our lab, we found that a $CF_4/SF_6/H_2$ combination works best for Ge waveguide platforms.

A parametric sweep of Ge layer etching in $CF_4/SF_6/H_2$ RIE plasma is shown in Table 2.1. Since the resist mask thickness is limited to 1 μm, we need to achieve Ge - resist etching ratios higher than 2. The etching rates for Ge and polymer

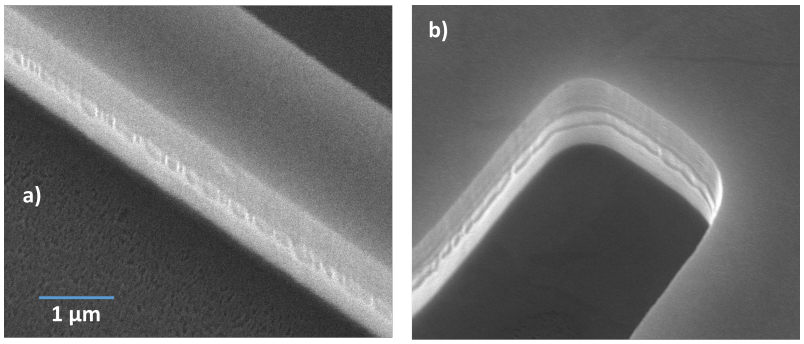

Figure 2.6: A waveguide etched in $CF_4/SF_6/H_2$ plasma using resist mask (a) and a 2 µm wide trench etched in the Ge layer (b). Etching in trenches usually looks worse than etching stand-alone structures.

depend strongly on the sample size - smaller samples have higher etching rates, but the trends remain the same. From samples s_0, s_1 and s_2 we can conclude that increasing the H_2 ratio in the gas mixture, slows down Ge etching. Although increasing the voltage bias makes the waveguide walls more straight, it can also cause the trenching effect (Fig. 2.5) and reduce the Ge - resist etching ratio (samples s_3 and s_5). SF_6 is a well known etching agent of group IV elements and has strong isotropic behavior even under high bias. To diminish this effect, we should reduce the portion of SF_6 flow in the total gas flow in the chamber. As we cannot increase the H_2 flow, another option is to increase the CF_4 flow. The best recipe to etch 2 µm Ge using 1 µm of resist is the recipe listed under s_8. After etching, we used acetone/isopropylalcohol (IPA)/water rinse, followed by 2 min in RIE O_2 plasma to get rid of the polymer residues.

Using contact lithography to pattern 1 µm of MIR 701 positive resist and a $CF_4/SF_6/H_2$ RIE process to define waveguides in a 2 µm Ge layer (Fig. 2.6), we achieve reasonable losses, from 2.5 - 5.5 dB/cm for 2.2 µm wide fully etched waveguides, and 2.5 - 4.5 dB/cm for 3.25 µm wide 1 µm partially etched waveguides, measured in the 5.2 - 5.45 µm wavelength range. The same processing was used to make 4 µm wide 2 µm partially etched waveguides in a 4 µm thick Ge film on a Si substrate. The losses measured at 5.3 µm are 2.5 dB/cm.

The losses can be further improved by combining the optimal dry etching recipe and wet etching of the sample in a H_2O_2 - water solution. However, due to the isotropic behavior of the peroxide wet etching, the Ge film thickness will change. To prevent the Ge waveguide from being etched from the top, it is enough to deposit 100 nm of SiO_2 on the Ge layer (Fig. 2.7a,b). A 1100 nm thick MIR 701 resist mask is used to dry etch through both the SiO_2 and Ge (Fig. 2.7c,d). The resist mask is then stripped in O_2 plasma (Fig. 2.7e). After the dry etching step, the sides of the Ge waveguides are passivated by fluoride (Ge-F bonds) and

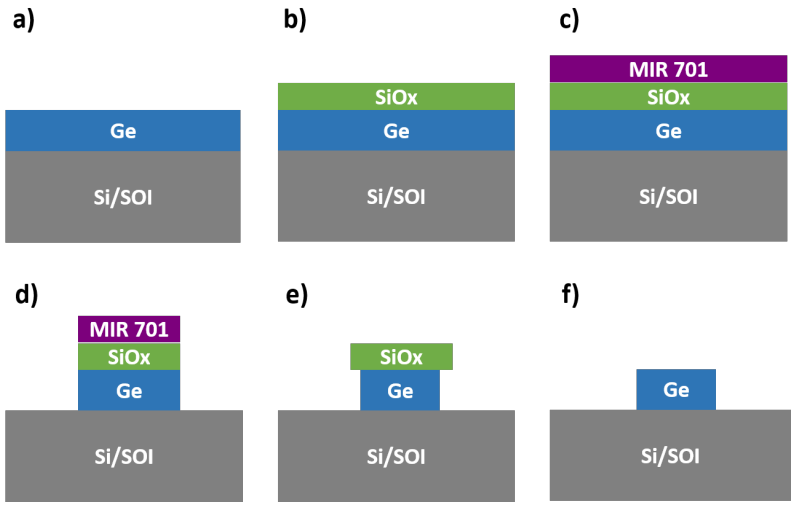

Figure 2.7: An idea for a process flow combining dry etching using resist mask and wet etching, to achieve smooth waveguide side walls: we deposit a thin layer of SiO_2 on top of the Ge layer to protect the top surface Ge waveguide surface from being etched in peroxide solution.

oxygen (Ge-O bonds) [6], which prevents further oxidation of the Ge layer. For example, it would not be possible to wet etch the Ge surface in peroxide solution without previously removing this passivation. To remove the passivation, it is necessary to perform a BHF dip (Fig. 2.7f). The etch rate of SiO_2 in BHF is around 200 nm/min, so the BHF dip should be shorter than 15 s, because we need a layer of silica to protect the top Ge surface. The silica layer is etched laterally as well, but this is negligible compared to the width of the Ge waveguide. Next, a peroxide wet etching is used to etch the Ge waveguide sides (Fig. 2.7g). At the end, a 1 min BHF dip removes the top SiO_2 layer, as well as the GeO_x residues from the peroxide etching.

2.3.2 DUV Lithography and Dry Etching

The advantage of DUV over contact lithography is its resolution, gained by the shorter wavelength used (193 nm) and de-magnifying the pattern (4:1 ratio in our case), from the glass mask to the resist. The scanner moves the wafer in such manner that the entire wafer surface gets exposed by the same chip design, providing a number of chips in one processing step. The exposure is done using a small slit of light. This way only a portion of the lens is used which reduces the influence of the optical aberrations, and improves the resolution comparing to regular stepper lithography where the whole reticle is exposed in one shot. After development,

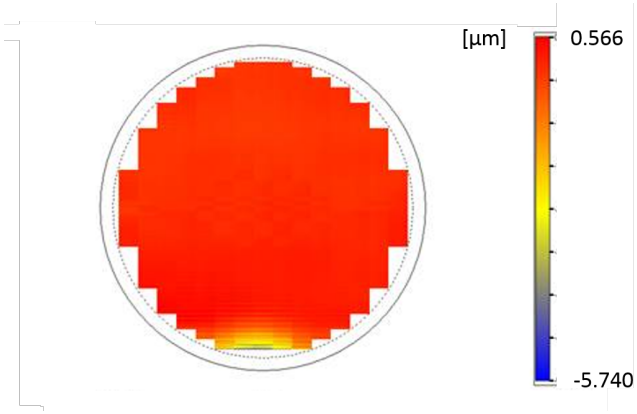

Figure 2.8: Wafer flatness is an important parameter for DUV exposure. Our wafers showed 6 µm *flatness variation across the entire wafer, while most of the wafer has flatness variation within 1* µm.

the defined pattern is then transferred into the guiding layer by dry etching. To test the process feasibility for the Ge-on-Si platform, we performed two experiments: the first experiment refers to the focus-and-expose matrix (FEM) experiment and etching mask definition (stack: 200 nm DUV resist + 50 nm bottom anti-reflective coating (BARC) + 50 nm Cr + 50nm SiN_x + 2 µm Ge), while the other experiment shows that with the thickness limitation of the SiN_x mask layer, a 2 µm thick Ge layer can be etched (stack: 1 µm MIR 701 resist + 600 nm SiN_x + 2 µm Ge).

We used a scanner tool operating at 193 nm at Eindhoven University of Technology. The FEM experiment allows to select the optimal exposure dose and focus, for the chosen critical dimension. The repeatability of the experiment depends strongly on the flatness of the wafer, which should not vary for more than 500 nm for a 3" wafer. In order to avoid focus variations across the wafer caused by wafer flatness, double sided polishing is preferred.

Since we had 200 mm single-side-polished Ge-on-Si wafers, the wafers were sent for laser dicing to cut out 3 wafers with a 3" diameter. The wafers had labels inscribed by a laser, which caused the wafer to bow around the inscribed label (Fig. 2.8). The labeling is done by a laser, which heats up the wafer locally. The wafer flatness, excluding the labeled area, was estimated to be within 1 µm. The wafers had 50 nm of Cr (used to etch up to 600 nm of SiN_x) and 50 nm of SiN_x (needed to protect the Cr etching tool from possible Ge contamination) deposited. To avoid influence of the layers beneath the resist, a BARC layer was spin-coated before the resist. The FEM optimization was done for a 100 nm gap on these wafers. With this experiment we made sure that a 100 nm gap (e.g. a coupler gap) could be defined by means of 193 nm DUV on our platform. The result of the FEM experiment is shown in Fig. 2.9. After testing the DUV system capabilities on the

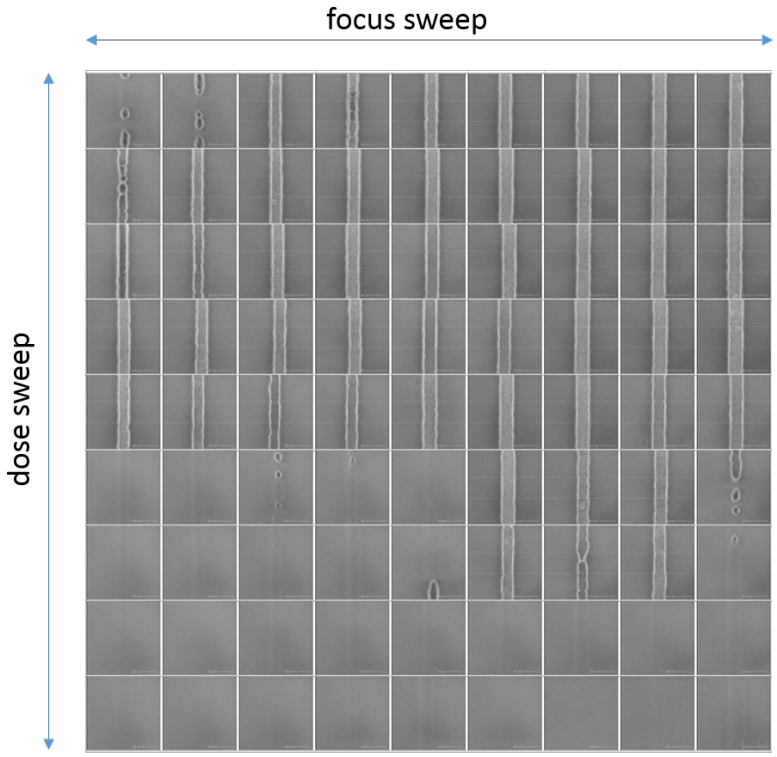

Figure 2.9: An example of a focus-and-expose matrix. Based on this experiment, the optimal focus and exposure dose is chosen. These parameters will depend on the critical dimension we want to achieve.

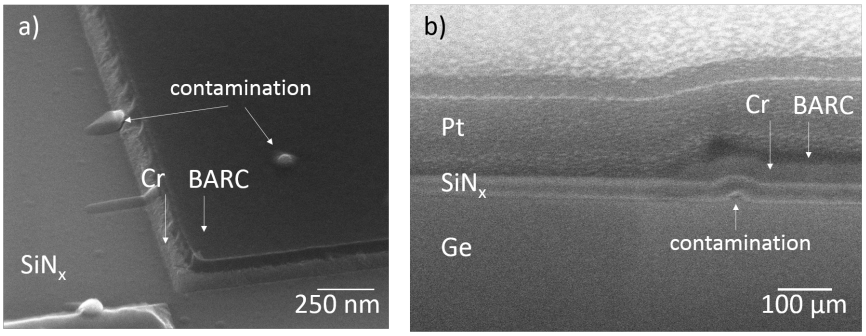

Figure 2.10: The BARC and Cr layers are etched at the same time in an ICP system. Unfortunately, the samples got contaminated before the SiN_x deposition. The contamination did not influence our FEM experiment however. The top view of the etched layers after the resist stripping (a) and the cross-section of the same (b). 50 nm of BARC and 50 nm of Cr are isotropically etched with selectivity towards the underlying 50 nm thick SiN_x layer.

Ge-on-Si platform, we started looking for an appropriate dry etching recipe. Due to the resist thickness (fixed for the DUV system in use), up to 50 nm of BARC layer and 50 nm of Cr mask can be etched. The BARC and Cr mask are etched for 90 s in a 15 sccm Cl_2, 15 sccm O_2 gas mixture. The etching recipe results in isotropic etching of the Cr mask, selective towards the underlying nitride layer (Fig. 2.10). In this experiment, the nitride layer serves to prevent contamination of the ICP etching chamber by Ge particles. Next, the resist is removed by an acetone/IPA rinse. The BARC and Cr layer serve as an etching mask for the nitride layer, which in turn serves as an etching mask for the Ge etching. With 50 nm of Cr we can etch up to 600 nm of SiN_x. In this paragraph we have described the experiment in which we show that the Eindhoven DUV stepper system can be used to define 100 nm features for the stack resist-Cr-BARC-Ge. In the next paragraph, we will talk about an experiment in which we test etching capabilities into the 2 μm thick Ge layer using 600 nm nitride mask.

The nitride mask is etched through RIE in a gas mixture of 80 sccm CF_4, 3 sccm SF_6 and 7 sccm H_2, at a pressure of 20 mTorr and with a 420 V DC bias, using 1 μm thick MIR 701 resist. After the nitride etching, the resist mask is removed by O_2 plasma followed by an acetone/IPA rinse. The sample is then loaded into the ICP system, where the Ge layer is etched. The used etching parameters for partial etching are (possible to etch up to 1.5 μm): 15 sccm Cl_2, 6 sccm H_2, 8 sccm CH_4, an inductive power of 250 W, an RF power of 200 W, at 15 mTorr, a temperature of 110 °C in the inductive chamber, and a 40 °C chuck temperature. In order to fully etch a 2 μm thick Ge layer, the etching recipe is modified from the partial-etching recipe, such to exclude CH_4 gas (0 sccm gas flow). This

modification allows us to etch deeper into the Ge layer with the same nitride mask thickness, but results in a higher propagation loss. The Ge layer is partially/fully etched, after which the remaining nitride mask is removed with HF.

We measured 3 dB/cm propagation losses on the partially etched sample for 3.25 μm wide waveguides and 8.5 dB/cm for fully etched 2.2 μm wide waveguides. With the two experiments we described in this section (the FEM and the dry etching using nitride mask experiments) we showed that we can achieve reasonable losses using high-volume, CMOS compatible fabrication tools such as a DUV stepper. This can result in high volume production of devices implemented on this waveguide platform.

2.3.3 Electron-beam Lithography and Dry Etching

Electron-beam (E-beam) lithography is a high-resolution (sub-10 nm) lithography tool that can draw custom patterns using a shaped beam, which can be deflected to preset positions within a writing field. The electron beam changes the properties of the e-beam-resist locally, resulting in a different solubility in the developing agent. For a positive resist, the exposed parts dissolve in the developing agent, while for the negative resist, the unexposed parts dissolve. In our cleanroom, we have a Raith Voyager system with a 50 kV electron beam and a maximum writing field size of 500 μm by 500 μm. To expose patterns that exceed the maximum writing field size, the system splits the design into multiple writing fields, whose writing is done in sequence: after exposing the first writing field the stage moves to center the electron beam above the next writing field, etc. The result is the exposed circuit design consisting of multiple writing fields stitched together. When moving the stage, stitching errors occur due to non-ideal behavior of the stage. Using larger writing fields can cause larger stitching misalignment errors, but smaller writing field sizes result in more stitching boundaries in the same circuit. The writing field size is, hence, chosen according to the application. The single-mode waveguide that we use, is 2.2 μm wide in the wavelength range (4.75-5.45) μm and the minimal lossless bend radius is 75 μm. The 500 μm by 500 μm writing field size allows e.g. accommodating a racetrack resonator with a radius of 100-120 μm or up to 750 periods of a first order grating with a period of 660 nm, in a single write field and hence avoid degradation of the Q-factor or phase errors in gratings by stitching effects. On other places where stitching cannot be avoided, the waveguides are expanded to a width of 5 μm as they incur less losses at stitching boundaries. This enabled the definition of complete circuits using e-beam lithography. The demonstration of the operation of these circuits will be discussed in later chapters.

We have developed a recipe for a positive e-beam lithography with an outcome of a negative slope, that we combined with metal deposition and a lift-off process to define a metal mask. This metal mask is then used to dry etch the waveguide

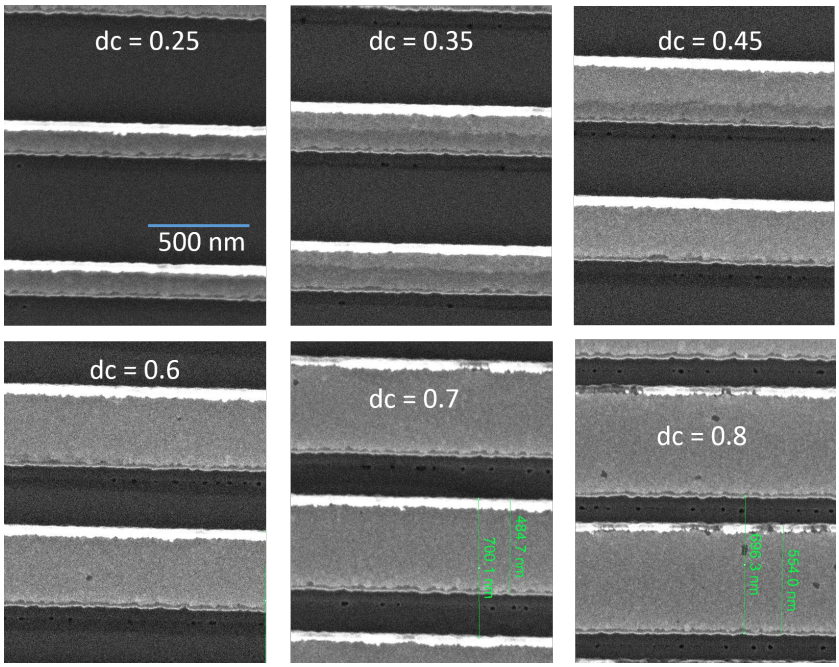

Figure 2.11: Top view of 5 nm Ti/50 nm Cr metal mask for a grating with a period of 0.7 µm *and different duty cycles (dc), from 0.3 - 0.8. All samples had a dose of 115* $\mu C/cm^2$ *and 2 min development in n-Amyl acetate.*

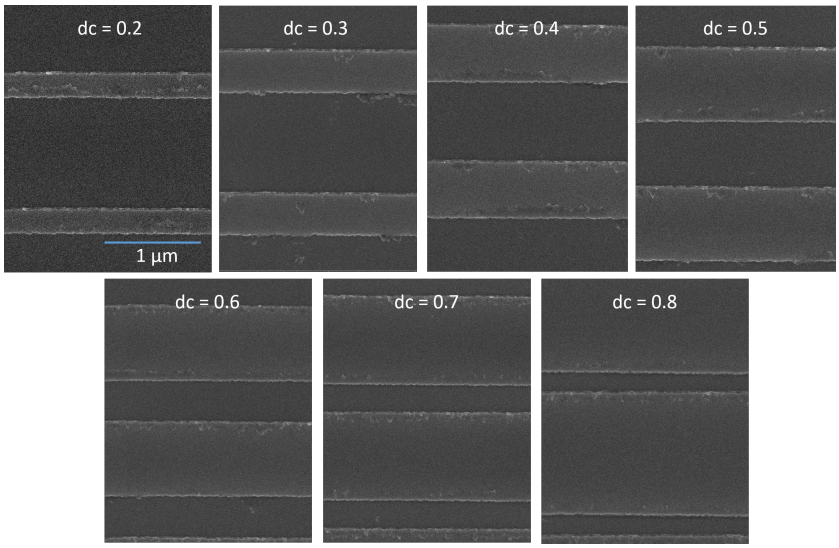

Figure 2.12: Top view of 5 nm Ti/50 nm Cr metal mask for a grating with a period of 1.45 µm *and different duty cycles (dc), from 0.2 - 0.8. All samples had a dose of 125* µ*C/cm*^{2} *and 2 min development in n-Amyl acetate.*

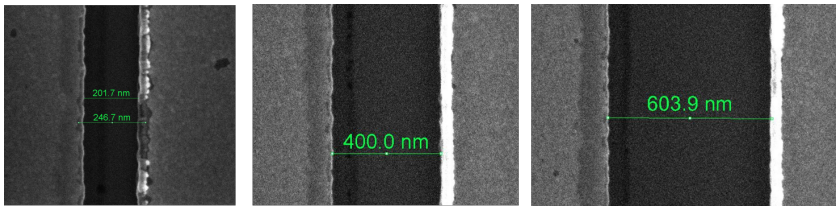

Figure 2.13: Top view of 5 nm Ti/50 nm Cr metal mask for coupler gaps of 200, 400 and 600 nm between two 2.2 µm *wide waveguides. All samples had a dose of 125* µ*C/cm*^{2} *and 2 min development in n-Amyl acetate.*

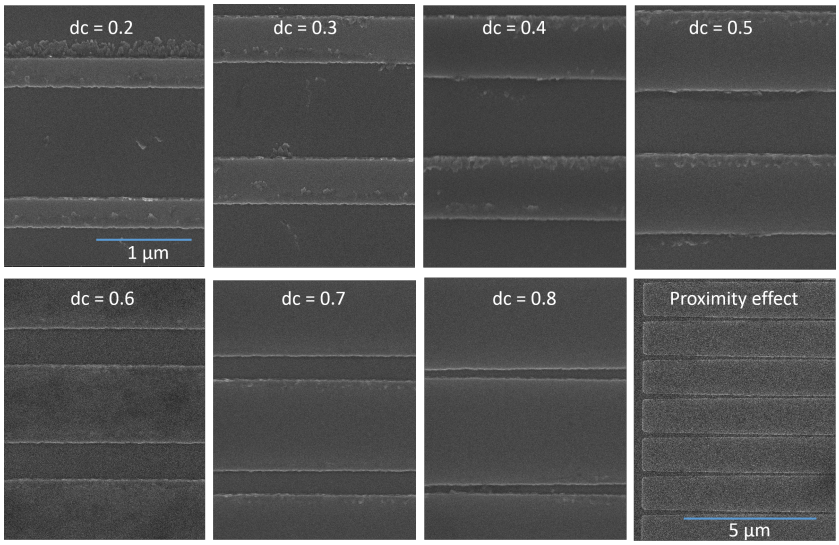

Figure 2.14: Top view of 5 nm Ti/50 nm Cr metal mask for a grating with a period of 1.45 µm and different duty cycles (dc), from 0.2 - 0.8. All samples had a dose of 145 µC/cm^2 and 2 min development in n-Amyl acetate. An example picture of the proximity effect for a grating with duty cycle of 0.8 is displayed in the bottom right picture.

circuit. The thickness of the metal should be adjusted to the depth (and thus the duration) of the subsequent dry etching step and therefore the resist should as well be sufficiently thick to enable the lift-off process. To achieve a wide range of possible etch depths, we used two e-beam resists: for etching less than 1 µm, we used the AR-P 6200.09 positive resist spin-coated at 2500 rpm to get 245 nm thickness, while for etch depths ranging from 1-2 µm we used AR-P 6200.13, spin-coated at 3000 rpm to get 475 nm resist thickness. For both resists, after the spin-coating, the solvents are evaporated and the resist is hardened by baking at 150 °C for 60s.

There are two ways of achieving a good resist profile for a lift-off process: combining a higher dose with an average development time, or an average dose with a higher development time. The recommended parameters from the resist supplier are a dose around 150 µC/cm^2 and a development time of 1 min in n-Amyl acetate, followed by 30s in IPA which is used as development stopper. Since even for doses as high as 220 µC/cm^2 the lift-off process was not working well for our platforms when performing the recommended 1 min development in n-Amyl acetate, based on preliminary results from a development time sweep experiment, we have focused on the second approach by fixing the development time to 2 min.

Based on simulations and the project goals, we have worked on the optimal dose for three different types of structures: a first order grating with a period of

700 nm and duty cycle around 0.5, a second order grating with a period of 1.45 μm and a duty cycle around 0.8, and a coupler gap of 400-500 nm between 2.2 μm wide waveguides. For very thin lines, such as a period of 700 nm and 0.2-0.5 duty cycle, the best results were obtained when exposing with a dose of 115 $\mu C/cm^2$ (Fig. 2.11). The lift-off process is not perfect for such thin lines, as on one side the metal along the sidewall which is standing upwards from the Ge surface after the metal deposition, does not break well, and so called "ears" are formed. This metal then folds on top of the wanted metal structure and creates a white shiny stripe in the SEM images. In most of the cases, the folding of the metal mask is within the boundaries of the wanted metal pattern and the sample can proceed with the fabrication, but there is a risk that the metal "ears" fold outside of the metal pattern we aimed to deposit, and create an unwanted shape in the Ge layer. For higher duty cycles it is also suitable to use a dose of 125 $\mu C/cm^2$. The latter dose also gives good results for second order gratings (Fig. 2.12), and the "ears" effect does not occur here, although for lower duty cycles such as 0.2-0.3 the edges of the metal mask are less straight than for higher duty cycles (0.4-0.8). Also coupler gaps between 200-600 nm (Fig. 2.13) can be accurately patterned using a dose of 125 $\mu C/cm^2$. Even though it seems that a slightly higher dose of 145 $\mu C/cm^2$ gives better results for the second order grating with a duty cycle of 0.8, it shows significant issues with the proximity effect. This issue is absent when using the dose of 125 $\mu C/cm^2$, which is why we choose the latter for our experiments. To summarize, a lower dose of 115 $\mu C/cm^2$ is better for narrow periodic lines ($<$300 nm grating tooth width), while for lines with widths ranging from 300-2200 nm (here we include the coupler gap of 200-600 nm between two waveguides 2.2 μm wide), a dose of 125 $\mu C/cm^2$ is more appropriate. Due to the low exposure dose, we use a 30 μm electron beam aperture with a 10nm step. This parameter is kept constant for both straight and curved elements.

After the exposure, the sample is submerged for 2 minutes in n-Amyl acetate for the development, followed immediately by a dip in IPA, which acts as a stopper agent, for 1 min. This results in a negative slope on the sidewalls of the resist. If the exposed pattern does not contain resist stripes narrower than 400 nm it is safe for the sample to be subjected to a few short turns in an ultrasonic bath in IPA environment. This will interrupt the delicate bridges in the resist created by the stitching errors. To further remove the resist residues from the bottom of the resist trenches, the sample is dry-etched for 10 s in a low pressure O_2 plasma to prepare the sample for metal deposition. The plasma removes the resist from all surfaces, which is why we lose about 25 nm of resist thickness in this step. O_2 plasma also activates dangling bonds on the Ge surface which helps with the adhesion of the metal to Ge. The metal deposition is done by electron beam evaporation. The combination of metals we use is 5 nm of titanium (Ti) and 50 nm of chromium (Cr) if the e-beam resist is 220 nm thick, or 5 nm of Ti and 90 nm of Cr if the

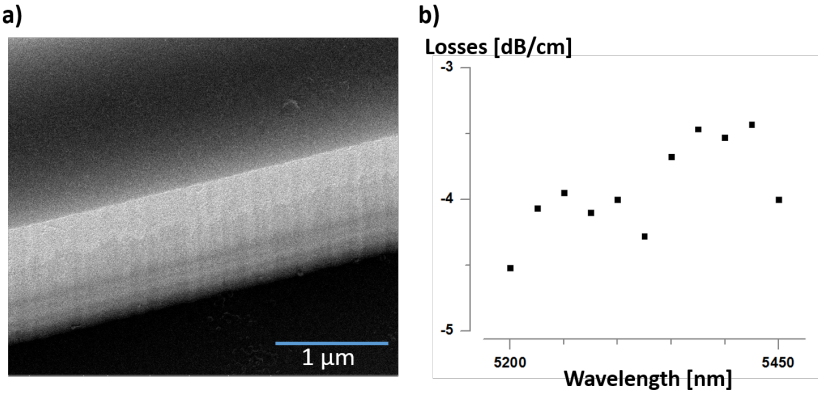

Figure 2.15: Fully etched waveguide using a 5nm Ti/90 nm Cr metal mask and a CF_4/H_2 etching recipe (a). Measured losses for partially etched waveguides (b).

resist thickness is 450 nm after the O_2 treatment. The lift-off process is done using the solvent anisole. As anisole is less volatile under atmospheric pressure than acetone, the risk of metal redeposition is lower than in the case of a lift-off using acetone.

After the metal mask is defined, the fabrication can proceed. If the entire circuit is defined in one e-beam exposure step, the pattern can be etched. However, if the circuit definition is not completed (e.g. some parts of the circuit still need to be defined through contact lithography, or in a second e-beam step), then those parts of the chip should be protected from the etching. Since with a positive e-beam resist and the lift-off technique, the originally exposed parts remain after etching, it is necessary to protect the rest of the sample, e.g. with a photo-resist (AZ9260). The etching step is done in the RIE system with a CF_4/H_2 dry-etching recipe, which we developed from our $CF_4/SF_6/H_2$ etching recipe used to etch waveguides with a thick photo-resist mask, as described in the previous subsection. SF_6 is a gas with isotropic etching behavior, which becomes more pronounced when the etching mask is thinner. Although etching Ge with CF_4 as a source gas, without the aggressive SF_6, makes the etch rate drop to only 22 nm/min, the sidewalls obtained with the slower recipe have a smoother texture (Fig. 2.15). After dry etching, it is necessary to remove the metal mask by leaving the sample in a 50% HF solution for 10 min. HF dissolves the thin Ti layer. The measured losses are estimated to be around 3.5-4.5 dB/cm for 3.25 µm wide, 1 µm partially etched waveguides in the wavelength range 5.2-5.45 µm.

2.3.4 E-beam Overlay

Some of the designed Ge-on-SOI waveguide circuits comprise shallowly etched (0.5 - 1 µm) grating couplers and a 2 µm deep etch for the rest of the circuit. The two etch depths call for a process with two separate etch steps (Fig. 2.16). The e-beam resist used in the first step gives better resolution (important for grating couplers) but it is limited to thicknesses below ∼250 nm. This resist thickness is sufficient to perform lift-off of a 50 nm Cr mask needed to etch up to 1 µm of Ge. Etching 2 µm of Ge necessitates 100 nm of Cr mask, which is why we opted for a less viscous version of the resist with which we can achieve ∼450 nm thick layer. However, this resist thickness is insufficient to effectively cover the 0.5 - 1 µm step in the partially etched gratings. For this reason, a combination of e-beam lithography and optical lithography is used. In the next paragraph, the overlay process is described in detail.

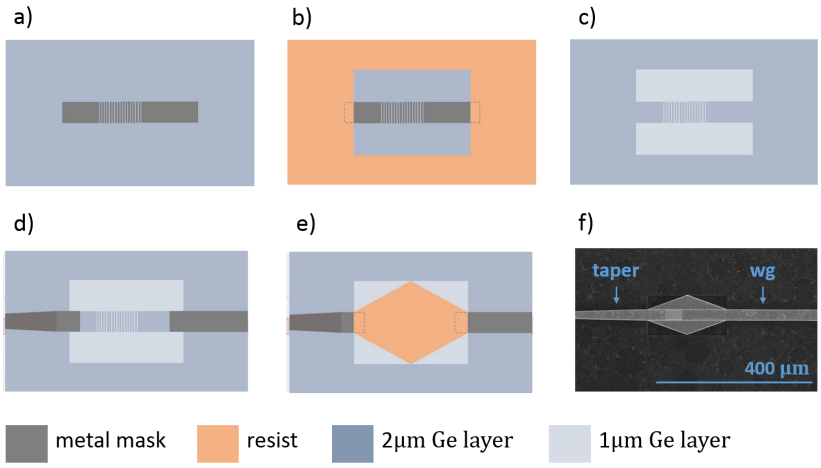

Figure 2.16: Top view of the fabrication scheme for combining partially etched gratings and a fully etched waveguide circuit, by combining electron beam and optical lithography.

In the first step we use a positive e-beam resist (AR-P 6200.09) to define a Ti/Cr (5 nm and 50 nm thick respectively) metal mask through a lift-off process for the partial etching of the gratings (Fig. 2.16a). Since we only define the gratings with the positive e-beam resist, it is necessary to protect the rest of the sample (Fig. 2.16b), for which we use a photo-resist (AZ9260). CF_4/H_2 reactive ion etching is then used to do the partial etch (Fig. 2.16c). After etching, the remaining photo-resist is removed using acetone and IPA, followed by the removal of the metal mask with HF. A second e-beam lithography step is then performed to define the rest of the circuit, which may include fabrication-sensitive components, e.g. racetrack

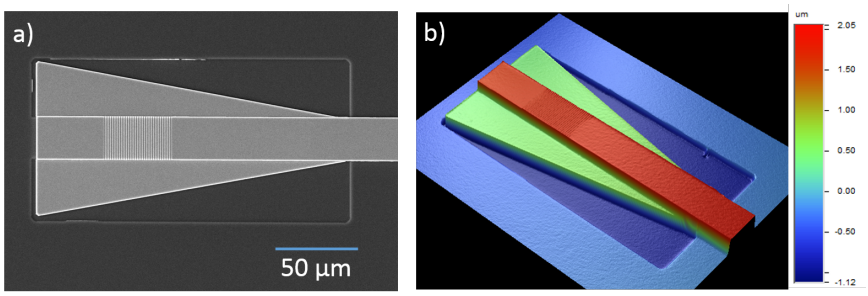

Figure 2.17: A SEM image (a) and a white light interferogram of a partially etched grating on a fully etched waveguide (b).

resonators (Fig. 2.16d). For the overlay resist, we use AR-P 6200.13 resist, which is by its chemical composition the same as AR-P 6200.09, with a difference in viscosity. More dense resist allows to achieve a thickness of 450 nm when spin-coated at 3000 rpm. This resist thickness is enough to define a 5 nm Ti / 90 nm Cr hard mask through lift-off. Here we again use AZ9260 photo-resist to protect the gratings from eroding during dry etching, in the points where the metal mask is not sufficiently covering them (Fig. 2.16e).

The protective structures defined in the AZ9260 photo-resist have a tapered shape such that there is a smooth transition from the grating to the fully etched waveguide. In order to reduce the influence of fabrication imperfections on the circuit performance we make sure that the two e-beam lithography patterns overlap on the slab section of the grating before tapering down to the single-mode waveguide. The second etching step is done in the same CF_4/H_2 plasma until the Ge-Si interface is reached (Fig. 2.16f), after which the photo-resist and the metal mask are stripped resulting in the structure shown in Fig. 2.17, where we can distinguish the partially etched grating, fully etched waveguide and the transitioning taper.

Alternative to the process flow we described here with two e-beam steps, we have tried to limit the processing to only one e-beam step, at expense of less efficient grating couplers due to the slightly worse resolution of AR-P 6200.13 photo-resist and thicker metal mask (10 nm Ti + 90 nm Cr). After patterning the entire circuit in one step, we first etch 1 µm for the gratings, then protect the gratings with AZ 9600 resist and continue etching until we reach the under-laying Si. However, we noticed that AZ 9600 resist is not entirely gone around the waveguide's side-walls after the development due to the topography of the sample. This residual resist creates a horizontal line on the waveguide's side-wall (Fig. 2.18), which in turn influences performance of components.

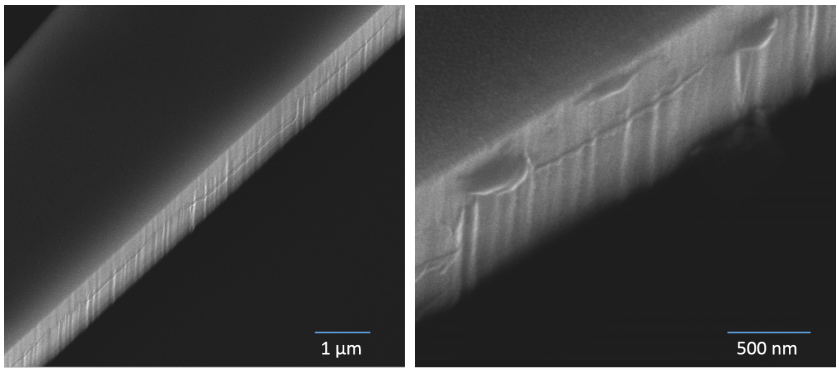

Figure 2.18: Alternative processing for the circuits with two etch depths that uses one e-beam step and results with a horizontal line over the waveguide's side-wall. This fabrication imperfection significantly reduces the Q-factor of racetrack resonators.

2.4 Anti-reflection Coating

Anti-reflection (AR) coatings are used whenever reflections from surfaces must be eliminated. Typical broadband ARs are made of multi-layer coatings, adapting the refractive index of the light-guiding medium to the refractive index of air. While an uncoated Ge surface causes a reflection of about 36% in the mid-infrared wavelength spectrum, a good AR coating can much reduce the reflections, according to simulations (Fig. 2.20). The reflection depends on the refractive index of the layer and the layer thickness (Fig. 2.20b). The optimal layer index is determined from:

$$n_{AR} = \sqrt{n_{Ge,TM_{00}} n_{air}} \tag{2.1}$$

Here, $n_{Ge,TM_{00}}$ is the effective index of the TM fundamental mode, TM_{00}, while n_{air} is the index of the air surrounding the waveguide. For our AR coating, we have used TiO_2. We have estimated the index of the TiO_2 layer, deposited in our e-gun chamber, to be 1.92 at 5200 nm. The estimation was obtained through ellipsometry at 1550 nm and fitting to a refractive index curve, found in literature [7].

The fabrication procedure is illustrated in Fig. 2.19. Since the sample is mounted under angle θ in the e-gun chamber, the real thickness of the AR coating will be $cos(\theta)$ times smaller than the deposited thickness. The optimal thickness for an AR coating in the 5 μm wavelength range with a refractive index of 1.92, is 750 nm.

Parasitic reflections play an important role in circuit behavior. One demonstration of the AR coating quality is shown in Fig. 2.21, where the transmission through two MZI circuits with and without AR coating is plotted. Our AR coating effectively suppresses unwanted secondary reflections which produce the Fabry-

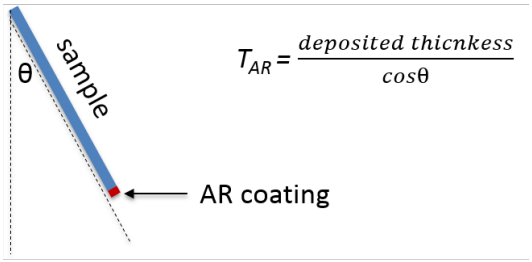

Figure 2.19: Fabrication of AR coating: the sample facing up is mounted under an angle which prevents unintentional deposition on the top of the sample.

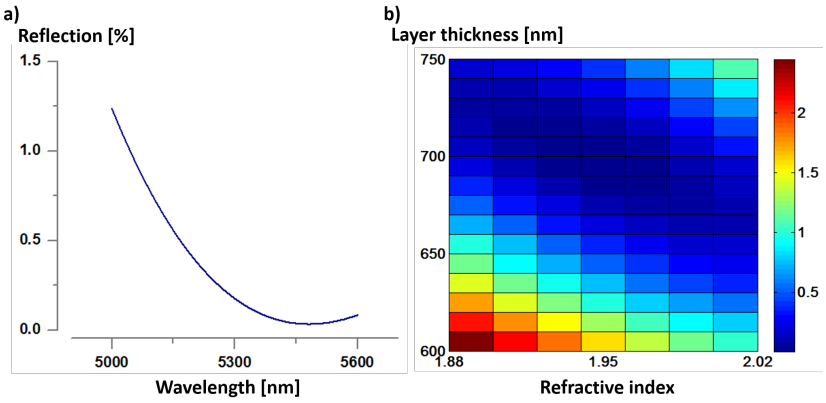

Figure 2.20: A 2D simulation of reflection from a 750 nm thick AR coating layer with an index of 1.92, deposited on the facet of a 2 µm *thick Ge slab on SOI waveguide (a) and a simulation of the reflection of the AR layer as a function of the refractive index and thickness of the layer at 5.2* μm *(b).*

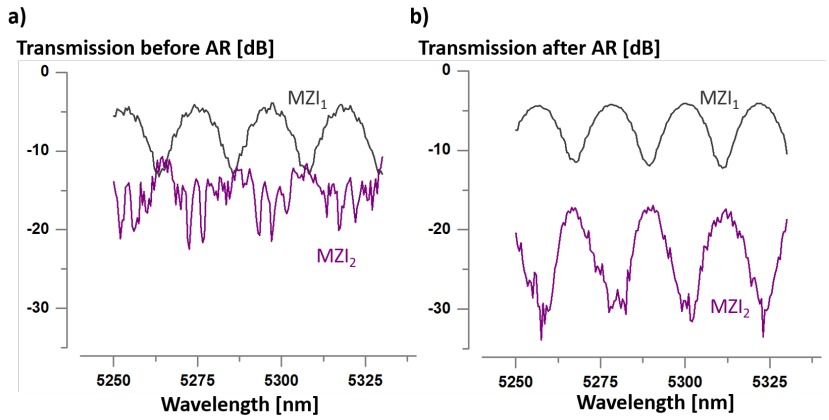

Figure 2.21: Transmission through two MZI circuits before applying AR coating (a) and after depositing the AR coating on all facets (b).

Perot wavelength-dependent ripples in transmission. In the case of the MZI_2 circuit, the intensity of the reflections before depositing the AR coating (Fig. 2.21a) is comparable with the insertion loss of the MZI circuit, and is masking the useful signal. After depositing the AR coating, the reflections are suppressed by around 15 dB, which resulted in the characteristic MZI transmission (Fig. 2.21b).

2.5 Top Cladding

In integrated photonics, cladded waveguides are often used to reduce the losses due to interaction of light with the side-wall roughness and to passivate the dangling bonds on the exposed parts of the waveguide. Besides passivation which provides chemical stability, another benefit is mechanical stability - using hard materials as waveguide cladding can prevent damage. A typical cladding used for the SOI platform in the telecom wavelength range is silica. This provides also vertical symmetry of the propagating mode. A lot of common cladding materials for applications in the telecom wavelength range are highly absorbing in the mid-infrared beyond 4 μm wavelength. We have measured the losses for a couple of materials whose bulk absorption does not show elevated values in the mid-infrared [8]: hafnium-dioxide (HfO_2), titanium-dioxide (TiO_2) and a type of fluoride glass (IR-F625).

HfO_2 is used for anti-reflection and multilayer coatings for high precision optics and laser coatings in the visible and infrared range. Its refractive index is close to 2. When deposited on an unheated substrate the layer has tensile stress. The deposition is done in our electron beam evaporation system in an O_2-rich atmosphere at a pressure of $4x10^{-5}$ mbar. We have measured that depositing 300 nm of

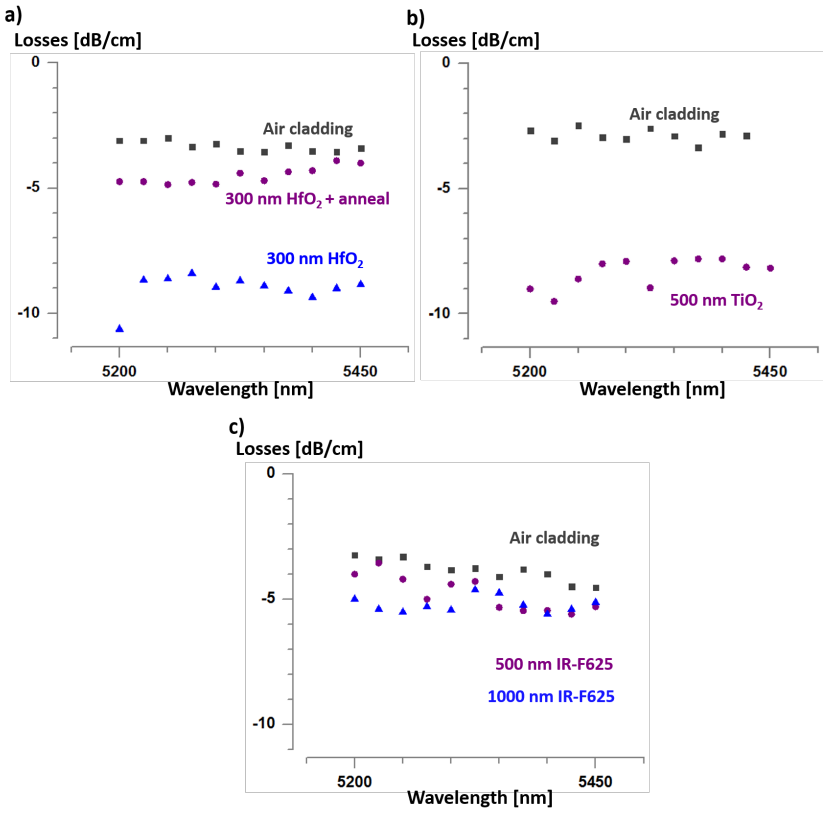

Figure 2.22: An estimation of additional losses caused by top coating deposition of HfO_2 (a), TiO_2 (b) and IR-F625 (c).

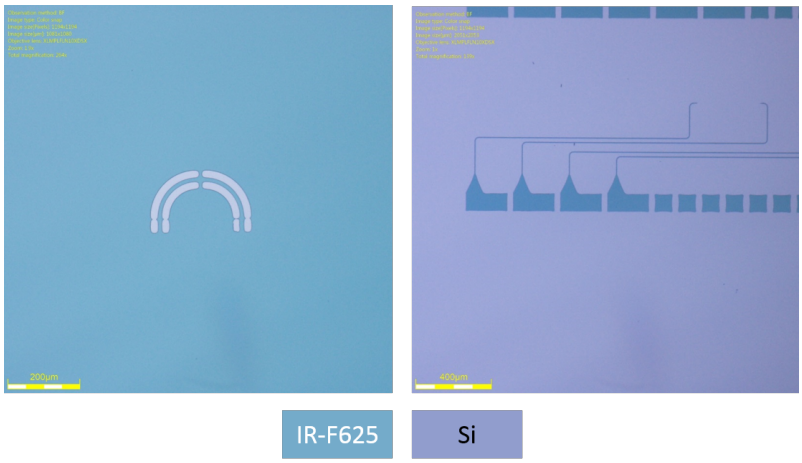

Figure 2.23: IR-F625 thin film etched in 37% HCl using AZ9260 photo-resist mask.

HfO_2 on 1 µm partially etched Ge-on-Si waveguides, cause an additional loss of 6 dB/cm in the wavelength range from 5.2 - 5.45 µm (Fig. 2.22a). Although losses dramatically increase after deposition, we have noticed that after annealing at 450 °C for 30 min in a N_2 atmosphere, the excess losses decrease to a reasonable value of additional 0.5-2 dB/cm. Annealing at temperatures above 450 °C led to damage in the HfO_2 layer.

TiO_2 is typically used in UV protection (as it absorbs in the UV), anti-reflection and multilayer coatings for lasers and free-space optics in the visible and infrared wavelength range. It melts around 1750 °C and is expected to give tensile stress on unheated substrates during deposition. We deposited TiO_2 in the electron beam evaporation tool in an O_2 atmosphere at pressure of $4x10^{-5}$ mbar. A wide range of refractive indices can be achieved with this material due to its structure that can vary from amorphous to crystalline depending on the deposition conditions, especially temperature. As mentioned previously, we have estimated that the refractive index of a thin film deposited in our e-gun chamber is around 1.92. We tested this cladding on Ge-on-Si partially etched waveguides on which we deposited 500 nm and 780 nm of TiO_2 and measured that it increases the waveguide losses by 5-6 dB/cm in the wavelength range from 5.2 - 5.45 µm (Fig. 2.22b).

IR-F625 is a material optimized by Umicore for low tensile stress and absorption, to replace radioactive ThF_4 and high-stress YF_3 films, also used as AR coating in the infrared. It has a refractive index of 1.5 and its melting point is at 1200 °C. We tested claddings of 500 nm and 1000 nm of IR-F625 on Ge-on-Si partially etched waveguides. The measured additional losses are up to 2dB/cm in the wavelength range 5.2 - 5.45 µm (Fig. 2.22c). Another advantage of this material is its resistance to HF wet etching, as deposited in our e-gun tool, while it can

be etched by hydrochloric acid (HCl). An example of the result of wet etching a 1 μm thick IR-F625 film with 37% HCl solution is shown in Fig. 2.23. The etch rate is 75 nm/min. This way, it is possible to use HCl to open gratings or create vias to access the heaters under the top cladding, without affecting the AR coating. The IR-F625 thin films, deposited in our e-gun tool, can survive up to 15 min in a HF 50% solution, after which cracks start to appear in the layer. However, if annealed at 250 °C for 30 min in a N_2 environment, the IR-F625 can be etched by HF. Annealing at this temperature can also reduce the losses by 1-1.5 dB/cm (tested at 5310 nm). Annealing at temperatures above 250 °C causes damage in the top-cladding layer.

In this section, we assessed three top-cladding layers with respect to the additional losses caused by these layers and processing limitation they impose. Both, IR-F625 and HfO_2 layers annealed at 450 °C in N_2 atmosphere are good candidates for the top-cladding of Ge waveguide platforms, while TiO_2 causes higher additional propagation losses, for the wavelength range 5.2 - 5.4 μm. IR-F625 offers better chemical stability but higher stress comparing to the HfO_2 layer. For fabrication of most of the circuits we will describe in later chapters we opted for air cladding to minimize the number of processing steps. Top cladding is beneficial for production of chips which will be used outside of laboratory environment as it provides mechanical protection and isolation from humidity and other environmental conditions.

2.6 Heater Definition

We use heaters to thermally change the effective index of selected components. Metal heaters deposited on top of a Ge post defined by a 100 nm thick metal mask and a dry etch step in a CH_4/H_2 gas mixture, are demonstrated in [9]. The distance between the Ge post and the Ge waveguide is set to be 3 μm, and both waveguides and Ge posts are defined at the same time in the Ge film. However, circuit formation by 1 μm photoresist mask and a dry etch process as we have described earlier, is affected by the etch lag effect (Fig. 2.24). When the standalone structures are etched 2 μm deep, only about 1.65 μm is etched in the 3 μm narrow trenches. For this reason, and because of heater efficiency, we have developed heaters where the metal is deposited directly on the SOI substrate (Fig. 2.25a). As the heat spreads directly from the heaters into the Si layer which has a higher thermal conductivity than Ge, these heaters show slightly better efficiency.

The thermal conductivity of SiO_2 is 1.4 W/mK, while the thermal conductivity of Si is 130 W/mK. The buried oxide layer in the SOI prevents efficient heat sinking into the Si substrate, which enhances the efficiency of the heaters. To better thermally isolate the heaters laterally and thereby improve their efficiency, we additionally etch through the top Si layer to prevent lateral heat spreading. As

an additional processing step, it is possible to remove the oxide layer underneath the heated waveguide.

2.6.1 Standard Heater Definition Process

The standard fabrication scheme for the heaters is displayed in Fig. 2.25c)-e). The heaters are defined by image reversal lithography with 3 μm thick Ti35E photo-resist. After development, 30s of O_2 plasma treatment in the RIE system is applied to remove any polymer residue off the bottom of the resist trenches (the Si surface). O_2 plasma can oxidize the Si top surface, which is why this step is followed up by a 5s BHF dip to remove the thin oxide layer. Next, a layer of Chromium (Cr) / Gold (Au) is deposited by e-gun evaporation, followed by an acetone assisted lift-off (Fig. 2.25c). The same process is then repeated to make the 700 nm thick Au metal pads to land probe needles. An SEM image of the heater structure, around a racetrack resonator, with labeled parts, can be seen in Fig. 2.25b). As we have mentioned before, the Si layer has very low doping, and as such it does not conduct the current well. In order to localize the heat produced by the heaters around the waveguide, trenches are etched in the Si layer (Fig. 2.25d). The trenches are formed by AZ9260 contact lithography, followed by dry etching in $CHF_3/SF_6/H_2$ plasma. Additionally it is possible to under-etch the heated part or the circuit with HF, to prevent any heat sinking into the Si substrate ((Fig. 2.25e). This could make the heating structures up to 5x more efficient compared to heaters on SOI with unetched BOX [9]. Cr and Au are typically resistant to HF etching, and previously we have mentioned that there is a 5s BHF step to ensure that there is no oxide on top of the Si surface before depositing metal. Still, in some occasions when exposed to HF the heaters exhibit problems with adhesion. This could be due to a non-negligible amount of SiO_2 forming again quickly before the metal deposition, possible O_2 leak into the deposition chamber or stress in the substrate layers which gets enhanced when additional metal layers are deposited on the already strained multi-layer stack. Because of the instabilities in this process we have described here, we have developed another way to make locally free-standing heaters, which will be explained in the next section.

2.6.2 Inverse Heater Definition Process

To avoid damage to the heaters by HF etching, it is possible to invert the process such that the metal heaters do not get exposed to the wet etchants. This is schematically explained in Fig. 2.26a)-c). First, the trenches in the Si layer are formed by AZ9260 positive photo-resist and dry etching by plasma. A 20 min HF wet etching step is performed to locally release the heated part of the circuit from the substrate, after which the metal heaters and contacts are deposited. Since the top surface of the chip already has topography (5 μm from the top surface of the Ge waveguide

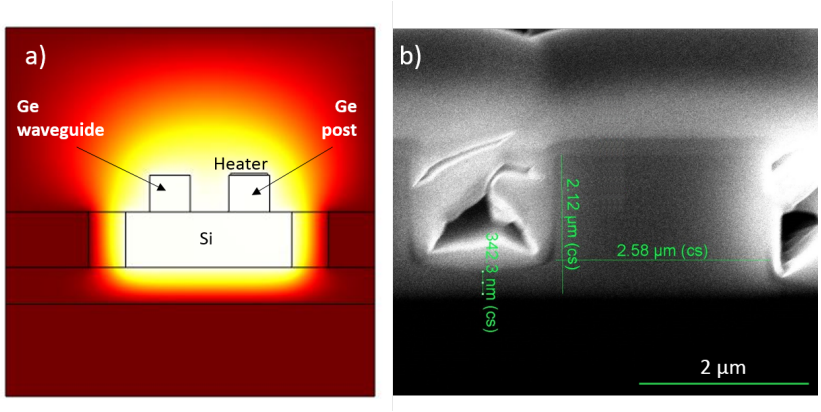

Figure 2.24: Design of heaters on top of a Ge post as described in [9] (a). Cross-section of the heater on Ge defined by contact lithography (b). The etch lag effect forms a bridge in the narrow gap between the waveguide and the heater post.

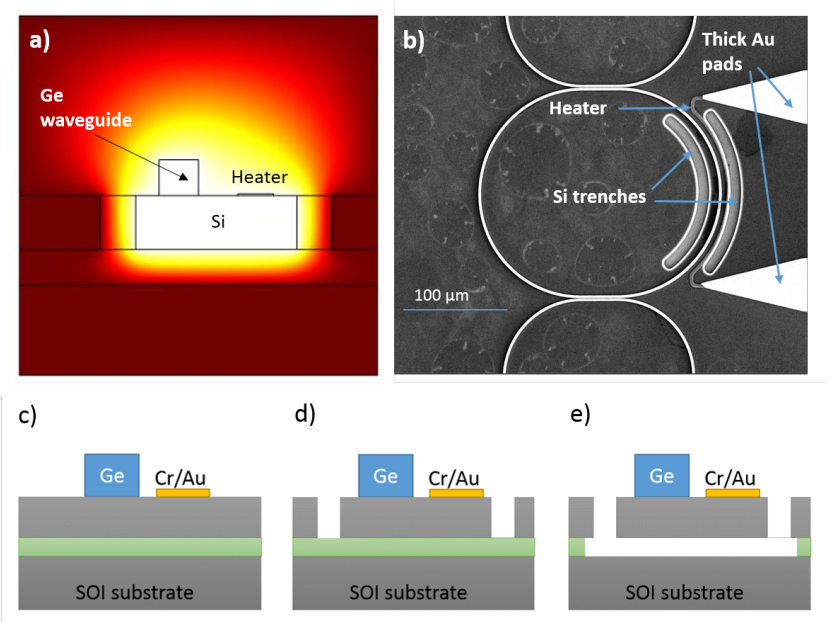

Figure 2.25: Design of heaters on the SOI substrate (a). Parts of the heating structure include the heater itself, thick metal contact pads and the trenches in the Si substrate layer (b). Fabrication process: heaters are deposited directly on the substrate (c), trenches are etched in the Si layer to access the BOX (d) which is then etched by HF (e).

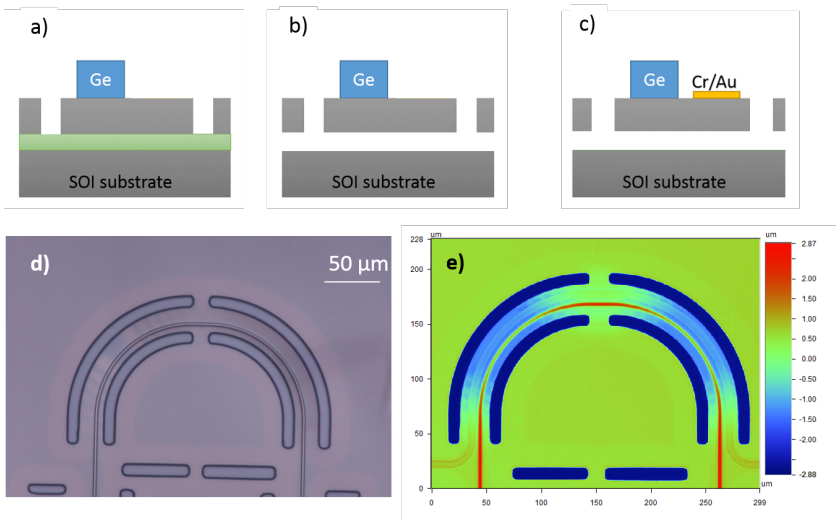

Figure 2.26: Fabrication process for inverse heater definition: trenches are etched in the Si layer to access the BOX (a), which is then etched by HF (b). In the last step metal heaters are deposited (c). Image of the structure after HF - before metallization (d) and white-light interferogram of the device after metallization (e). Already after HF wet etching, the released parts of the circuit start to bow.

till the bottom of the trenches in Si), 4 µm of Ti35E resist is used. After 30s in O_2 plasma and 5 s in BHF, Cr/Au heaters are deposited by e-gun. The same lithography and O_2/BHF resist cleaning steps are used to define metal contacts. A 700 nm thick Au layer is deposited in a Univex evaporation tool. After the processing, the released part of the circuit is bending towards the Si substrate . The heater efficiency is not reduced however ($\sim$ 60 mW for 2π shift).

2.7 Conclusion

In this chapter we discussed waveguide circuit definition by lithography and dry/wet etching. The Ge circuits can be defined by contact and e-beam lithography and dry etching. By demonstrating compatibility with DUV fabrication large-scale manufacturing is within reach. Additionally, we described other processing steps for Ge-on-Si/SOI waveguide circuit fabrication such as different techniques for heater definition, several top-cladding layers and an AR coating. In the following chapters, we will present devices and circuits fabricated using combinations of these processing steps.

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3

Laser-chip and Fiber-chip Interfaces

3.1 Introduction

Packaging, as well as wafer-level testing of integrated optical devices requires the implementation of efficient fiber-to-chip grating couplers. However, grating couplers limit the wavelength range of operation. In this chapter we will discuss fiber-to-chip grating couplers for circuit testing and the edge couplers used for the tunable laser outcoupling, by butt-coupling with optical fiber. At the end, we will discuss III-V gain chip to Ge waveguide butt-coupling approach.

3.2 Fiber-chip measurement setup

For the grating coupler / edge coupler characterization we used a setup schematically shown in Fig. 3.1. Light from the free-space emitting QCL operating in continuous wave is coupled to an InF single mode fiber. The laser operates in three regimes that are of interest to us: in pulsed regime from 5.15 - 5.45 μm and a repetition rate of up to 100 kHz and 5$\%$ duty cycle; continuous wave (CW) from 5.2 - 5.4 μm; and continuous wave - mode hop free (CW-MHF) from 5.25 - 5.4 μm. Between the QCL and the fiber coupler, there is a Babinet-Soleil polarization control element and a chopper. The chopper turns the CW and CW-MHF light into 50$\%$ duty cycle pulses and hence, allows us to detect the signal using a pre-amplified InSb detector and a lock-in amplifier. With the polarization controller element the input polarization state is set. The fibers are not polarization main-

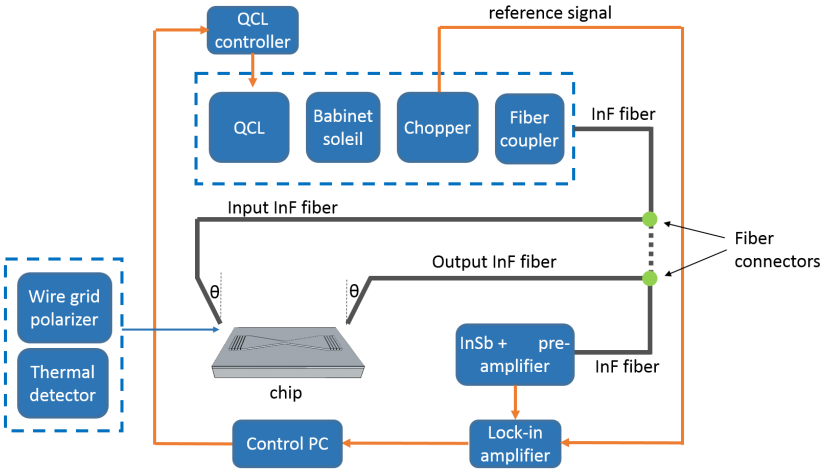

Figure 3.1: The measurement setup. A control PC sets the wavelength of the QCL in CW or pulsed mode through the QCL controller. The light from the laser goes through the Babinet-Soleil polarization control element and the chopper that turns the CW light of the QCL into a 50% pulsed signal which is then coupled to the single mode InF fiber by a chalcogenide objective lens. The device transmission is measured by a pre-amplified InSb detector and a lock-in amplifier that receives the reference from the chopper and sends the detected signal back to the control PC. A wire grid polarizer and a thermal detector are used to determine the fraction of light in a particular linear polarization at the input of the grating. The QCL power is measured on the InSb detector, by connecting directly the two fiber connectors - dashed grey line on the diagram

taining and the polarization rotation in the fiber is wavelength dependent, hence a wire grid polarizer and a thermal detector are used to determine the polarization at the output of the input fiber. The setup can be used in a vertical or in a horizontal configuration, depending whether the fibers are fixed on goniometer stages or on horizontal holders.

To estimate grating coupler efficiency, the Daylight Solutions QCL operating in CW mode in combination with the chopper is used. The laser light is coupled to an InF single mode fiber with a mode field diameter of 17 μm at 5.2 μm wavelength. With the polarization control element, we maximize the transmission through the device at the central wavelength. This way we ensure that most of the light is TM polarized at the output facet of the fiber, as the gratings are optimized for TM polarization. Since the fibers are not polarization maintaining we measured the TM fraction of light R_{TM} as a function of wavelength at the output facet of the input fiber by placing a wire grid polarizer and a thermal detector under the fiber facet. The fact that the light is not perfectly linearly polarized across the wavelength range of interest is taken into account in the calculation of the coupling

efficiency. The loss caused by the difference in fiber length when measuring the transmission through the chip (full grey line in Fig. 3.1) and when measuring the QCL power P_{QCL} directly (dashed grey line in Fig. 3.1) is not negligible in the wavelength range of interest and is evaluated from [1]. The fiber loss ranges from 1-2.5 dB/m over the considered wavelength range. Taking all of this into account, the efficiency $\eta(\lambda)$ of a single fiber-to-chip grating coupler is given by

$$2\eta(\lambda)[dB] = 10log_{10}\frac{P_{trans}(\lambda)}{P_{QCL}(\lambda)R_{TM}(\lambda)} + A_{fiber}(\lambda)[dB] \tag{3.1}$$

$P_{trans}(\lambda)$ is the power received by the detector when coupled through the chip, $A_{fiber}(\lambda)$ is the attenuation caused by the difference in fiber length mentioned earlier, and the 2 on the left side of equation comes from the fact that we measure the transmission through two couplers.

3.3 TM Fiber-to-Chip Grating Couplers

The efficiency of a grating coupler is limited by its directionality (power diffracted towards the fiber with respect to power in the waveguide) and the overlap between the fiber mode and the field diffracted by the grating towards the fiber. Many approaches have been suggested to improve the directionality, especially at the telecommunication wavelength range, such as slanted gratings [2], a substrate mirror [3] or a silicon overlay [4]. Other designs yielded similar efficient grating couplers due to optimization of the overlap between the fiber mode and scattered field of the grating [5–7]. However, experimentally characterized grating couplers in the mid-IR have shown lower efficiency then the couplers at telecom wavelengths [8–10].

As the PICs considered in this work will be butt-coupled to a QCL emitting TM polarized light with grating couplers used as test ports, our couplers are optimized for TM polarization. The schematic cross-sections of the grating structures designed on the Ge-on-Si and Ge-on-SOI platform are shown in Fig. 3.2a) and b), respectively. For the Ge-on-Si platform we use a standard second order grating structure with a uniform grating period and duty cycle. For the Ge-on-SOI platform we have designed a more complex grating structure to optimize the coupling efficiency. In fact, a fourth order grating is used, comprising a uniform and apodized grating section. Using larger period that corresponds to the fourth order grating allowed for more complex design (features defined by e-beam vary from 0.5 - 1.5 nm). Secondly, the SiO_2 layer is locally removed to enhance the coupling efficiency further, as the reflectivity of the Si/air interface is larger than the reflectivity of the Si/SiO_2 interface because of larger index contrast. This ensures that almost no light is scattered towards the substrate.

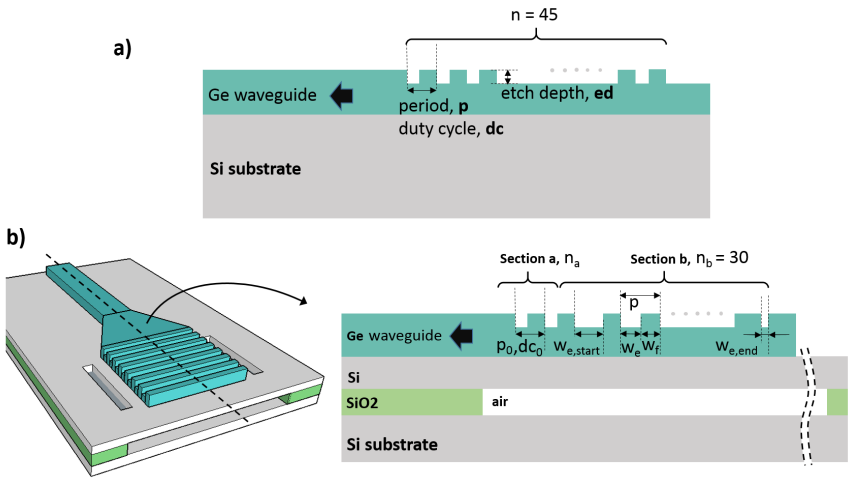

Figure 3.2: Schematic of the grating structures designed on the Ge-on-Si (a) and Ge-on-SOI (b) waveguide platform.

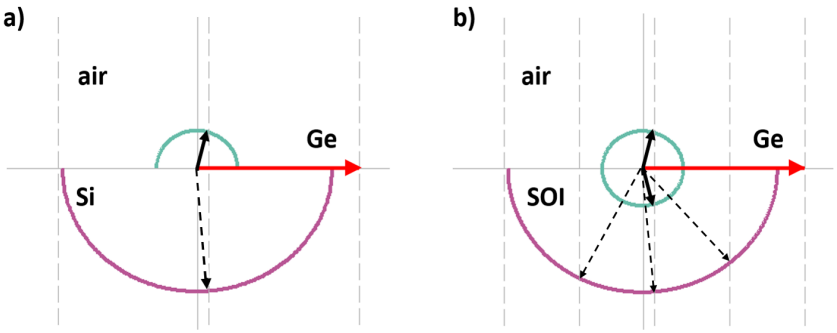

Figure 3.3: Vector diagram of a second order Ge-on-Si grating (a) and a fourth order Ge-on-SOI grating (b) with the buried oxide layer locally removed. The allowed diffraction orders in air (solid arrows) and Si under-cladding (dashed arrows) are also indicated.

The wave-vector diagrams for both cases assuming a uniform grating are shown in Fig. 3.3. The Si bottom cladding supports the propagation of several diffraction orders for the fourth order grating. Generally, for the same layer stack, it is expected that second order gratings exhibit higher coupling efficiency than fourth order gratings due to the larger number of diffraction orders in the latter case. However, at the Si/air interface these higher diffraction orders undergo total internal reflection - as indicated in Fig. 3.3b) by the green circle representing the length of the k-vectors in air - whereby they are 'recycled' in the structure. This results

in only a single diffraction order propagating in the air gap towards the silicon substrate. By properly optimizing the layer structure the power in this downwards diffracted field can be minimized, thereby maximizing the directionality of the grating structure towards the optical fiber. Note that the total reflectivity of the substrate comprises the coherent addition of a reflection at the Si-air and air-Si substrate interface, therefore the buried oxide layer thickness also has an impact in the case of the Ge-on-SOI coupler. To further increase the fiber coupling efficiency we implemented an apodization where the etched feature w_e changes linearly from $w_{e,start}$ to $w_{e,end}$ and where w_f is determined by:

$$p(n_e + n_f)/2 = w_e n_e + w_f n_f \tag{3.2}$$

p is the period of the corresponding grating coupler with the same etch depth when the duty cycle is constant and equal to 0.5, optimized for a given fiber angle. w_e and n_e are the width of the slit and the effective index of the fundamental TM mode in the slit respectively, while w_f and n_f are the width of the unetched part and effective index of the fundamental TM mode of the unetched part of the grating respectively. Another feature of the grating is that it has n_a grooves at the entrance of the grating coupler structure with uniform duty cycle dc_0 and period p_0, which makes the perturbation of the waveguide caused by the grating less abrupt and reduces reflection in the waveguide when coupling from the PIC to the fiber. This section is marked as Section a in Fig. 3.2. The Sections a and b are designed with the same etch depth. The proposed design is a trade-off between the complexity of the grating structure, both in terms of device optimization and fabrication, and the fiber-to-chip coupling efficiency. The parameters are optimized for maximal efficiency at a wavelength of 5.2 μm.

3.3.1 Grating coupler for the Ge-on-Si platform

When designing a uniform second order grating coupler for the Ge-on-Si platform, we optimized the period of the grating to ensure that maximal coupling is achieved at the central wavelength of interest. We additionally optimized the duty cycle and the etch depth of the gratings to achieve the best directionality of our structure and maximum overlap of the diffracted field profile with the fiber mode. Other parameters taken into consideration are the angle between the fiber and the vertical y-axis, and the position of the fiber on the x-axis parallel to the grating. The number of periods was set to 30. All simulations were performed using a 2D finite-difference-time-domain solver. The best simulated TM coupler for Ge-on-Si with 2 μm thick Ge device layer, has a period of 1.45 μm and an etch depth of 0.9 μm with a duty cycle of 0.8 (defined as the ratio of width of the unetched Ge grating teeth and the grating period). The optimal fiber angle for the coupler is 5°. A maximum coupling efficiency of 40% with a 3 dB bandwidth of 180 nm is

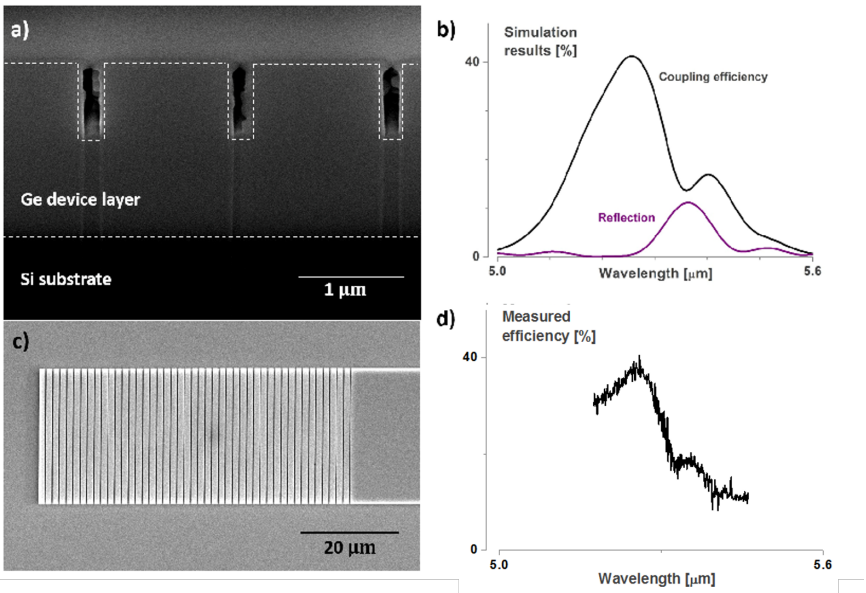

Figure 3.4: Cross-section (a) and top view of the optimized Ge-on-Si grating coupler (c). Simulation (b) and measured data of the same device (d).

obtained (see the top graph in Fig. 3.4b). The best lateral overlap of the fiber mode and the fundamental TM grating mode was achieved for a 27.5 µm wide grating.

A cross-section and top-view picture of the realized grating coupler structures is shown in Fig. 3.4a). The couplers, together with the waveguides, were etched in one step by a CF_4/H_2 plasma using a Ti/Cr mask. The mask was defined by e-beam lithography using a positive resist and lift-off process. After the etching process the metal mask was removed by HF wet etching.

Experimentally, a fiber-to-chip coupling efficiency of 40% and a 3dB bandwidth of about 200 nm is obtained (Fig. 3.4b). In Fig. 3.5 we show the impact of the grating etch depth and germanium waveguide layer thickness on the fiber coupling efficiency, as a function of the fiber-to-chip grating angle. By varying the etch depth or the Ge thickness within $\pm$100 nm of the optimal value we lose less than 5% in maximum coupling efficiency which means that our design has high tolerance to fabrication imperfections.

3.3.2 Grating coupler for the Ge-on-SOI platform

In our Ge-on-SOI design we have fixed the thicknesses of the Ge layer to 2 µm. The SiO_2 layer was also fixed to 2 µm, because of the commercial availability of such SOI wafers. The thickness of the Si layer is to be optimized such that

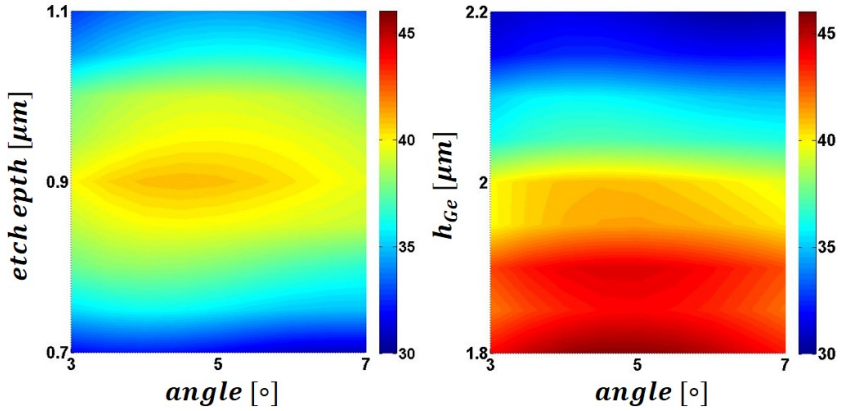

Figure 3.5: Maximum coupling efficiency in the 5-5.6 μm *wavelength range for the Ge-on-Si grating coupler as a function of the grating etch depth and fiber angle (a) and as a function of thickness of the Ge layer and fiber angle (b).*

we maximize the directionality of the grating, as discussed above. However, the Si layer has to be thicker than 3 μm so that the loss of the optical mode is not enhanced by the overlap with the SiO_2 layer, which is heavily absorbing in the wavelength range of interest. The optimized coupler has a period of $p = 2.88$ μm, an etch depth of $h = 0.5$ μm, with $w_{e,start}$ = 1.4 μm and $w_{e,end}$ = 0.5 μm. Section a has n_a = 2, a period of p_0 = 1.8 μm and a duty cycle of dc_0 = 0.5. The thickness of the Si layer in this case is 3.2 μm. The angle of the fiber is 10°. The Ge-on-SOI coupler with these parameters has a simulated coupling efficiency of about 70% and a 3dB bandwidth of 200 nm, as shown in the top graph of Fig. 3.6b).

A top-view image and schematic view of the fabricated grating coupler structure is shown in Fig. 3.6a). We have locally under-etched the grating by accessing the SiO_2 layer through narrow openings in the Si layer and by HF wet etching of the oxide layer. The rest of the SiO_2 layer serves as support such that the free-standing structures would not collapse. The couplers, together with the waveguides, were etched in one step by CF_4/H_2 plasma using a titanium/chromium mask. The mask was defined by e-beam lithography using a positive resist and lift-off process. After the etching process the mask was removed by HF wet etching.

The measured device has a maximum efficiency of 45% and a 3 dB bandwidth of 220 nm estimated by interpolation (Fig. 3.6c). In Fig. 3.7 we show the dependence of the maximum coupling efficiency on different parameters (the thickness of the silicon cladding h_{Si}, the thickness of the buried oxide layer h_{SiO_2}, the thickness of the Ge waveguide layer and the grating etch depth). Due to the interference mechanism in the layers under the grating, efficiency strongly depends

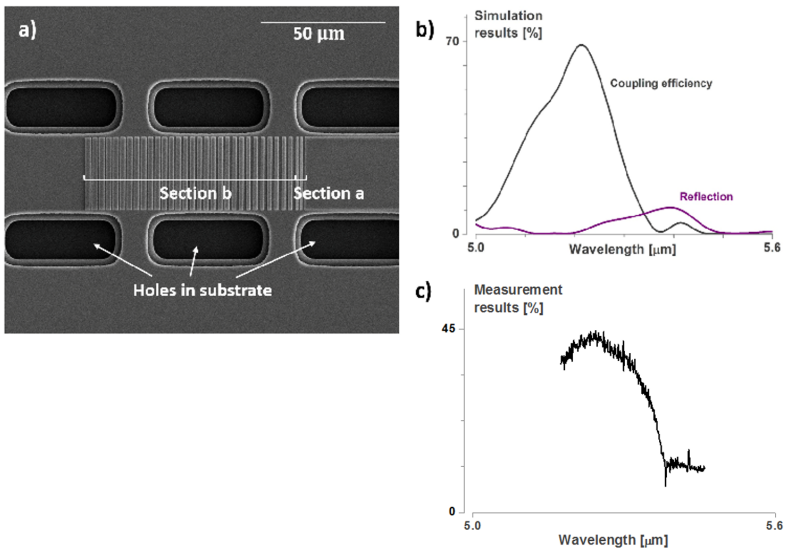

Figure 3.6: SEM image of the locally free-standing Ge-on-SOI grating coupler (a). Simulation (b) and measured data of the same device (c).

on the layer thicknesses in the substrate. Up to 10% can be lost in maximum coupling efficiency by varying the thicknesses of the Ge or Si layer within $\pm$50 nm of the optimal value. The insertion loss is dependent on the thickness of the SiO_2 layer - by changing the thickness of this layer by $\pm$100 nm we can lose up to 5% in maximum coupling efficiency. When the grating is released from the substrate (free-standing) it becomes subject to stress in the free-standing layers which causes the grating to bend and hence change the thickness of the air gap beneath it (h_{SiO_2}) from the optimal value that we got in our simulations. The difference in the maximum simulated and measured efficiency is attributed to these fabrication imperfections. Comparing to the Ge-on-Si design, this coupler is less tolerant to fabrication imperfections, as it has more parameters whose small variations can contribute to a decrease in the peak efficiency.

3.4 Ge waveguide-to-fiber butt-coupling

Commonly used materials in fiber manufacturing, such as SiO_2, have elevated absorption in the mid-infrared. For wavelengths beyond 2 µm, different materials are therefore used for fibers [11]. InF fibers have reasonable losses for wavelengths up to 5.6 µm. Its losses and mode field diameter depend on the wavelength (Fig. 3.8). The mode field diameter is significantly larger than the Ge layer thickness

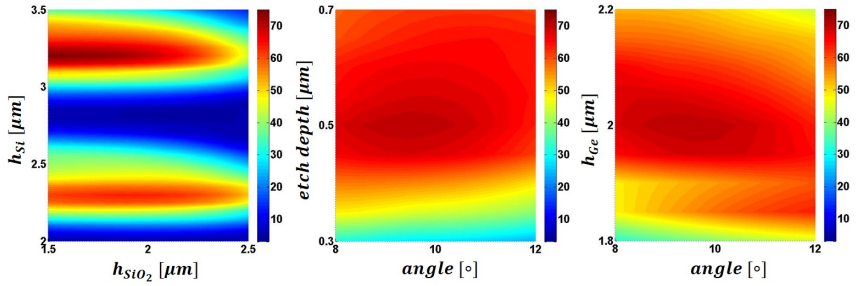

Figure 3.7: Maximum fiber-to-chip coupling efficiency in the 5 to 5.6 µm *wavelength range for the Ge-on-SOI grating coupler depending on different parameters: Si and SiO_2 layer thickness (a), grating etch depth and fiber angle (b) and the thickness of the Ge waveguide layer vs. fiber angle (c).*

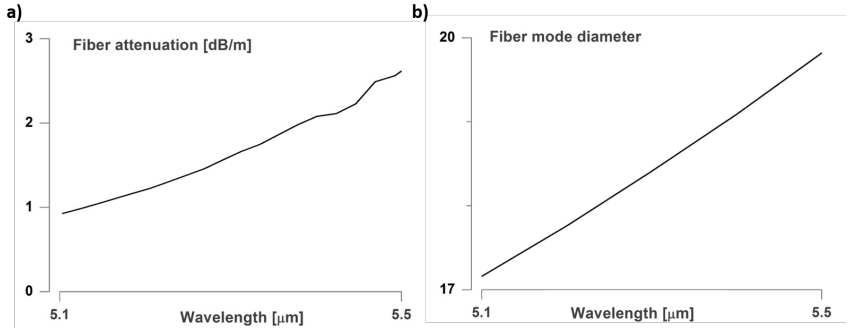

Figure 3.8: Wavelength dependent losses (a) and mode field diameter (b) of the InF fibers used in this work [1].

(∼18 µm vs. 2 µm), which leads to low coupling efficiency. In horizontal direction we can set the waveguide width to achieve better coupling. On Fig. 3.9a) we plotted the coupling efficiency as a function of the waveguide width at 5.3 µm wavelength fo a 10 µm gap between the fiber and the waveguide. In practice, it is difficult to achieve 0 µm gap, and our estimations are that the gap is around 10 µm. The coupling efficiency changes dependent on the gap between the waveguide and the fiber (Fig. 3.9b). In most of our circuits we fixed the waveguide width to 15 µm.

3.5 Laser-to-Ge waveguide butt-coupling

The active region of the QCL gain chip used in our work is based on a GaInAs/AlInAs lattice grown on a InP substrate [12]. The gain chip is designed for TM polarization. Therefore, our Ge-on-SOI chip is also designed for TM polarization. The

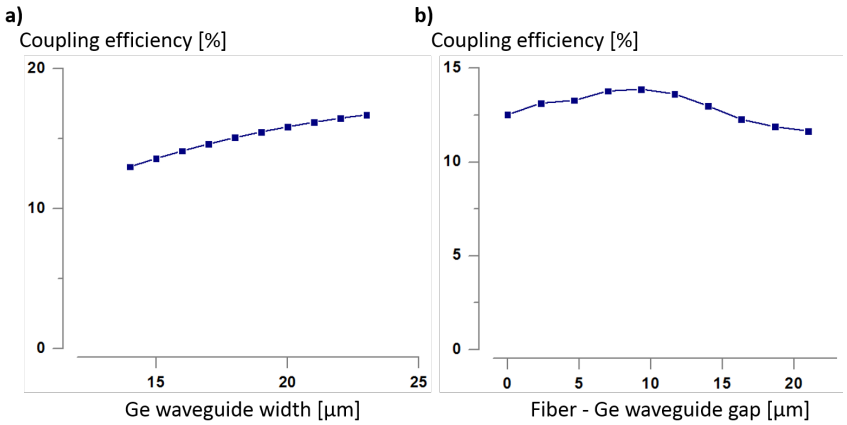

Figure 3.9: Butt-coupling efficiency vs. waveguide width for a 10 µm *gap between InF fiber and waveguide (a) and efficiency vs. gap for a 15* µm *wide Ge waveguide (b).*

Material	Index	Thickness [µm]
InP layer3	3.1	3
InP layer2	3.11	1
InGaAs layer3	3.27	0.1
InGaAs layer2	3.3	1.7
InGaAs layer1	3.27	0.1
InP layer1	3.11	2.2
InP substrate	2.81	$\sim$ 300

Table 3.1: Equivalent layer structure of the laser used in simulations

equivalent III-V stack, used to simulate the efficiency of the coupling of light from the III-V ridge waveguide to Ge waveguide, is displayed in Table 3.1.

While the width of the Ge input taper could be selected to profit from maximum overlap with the mode of the gain chip, and it is set to 10 μm, the thickness of the Ge waveguide layer is fixed to 2 µm which limits the maximum butt-coupling efficiency, as the $1/e^2$ width of the mode power profile along the fast axis (perpendicular to the III-V stack) is 3 µm. From Fig. 3.10a we can see that due to the geometry of the cross-sections of the two waveguides, the alignment along the fast axis is more sensitive than the alignment along the slow axis. Optimal overlap of the two mode field profiles is achieved for the center of the Ge waveguide 0.35 µm above the center of the active area ridge waveguide.

For the optimal horizontal alignment, we have simulated the butt-coupling ef-

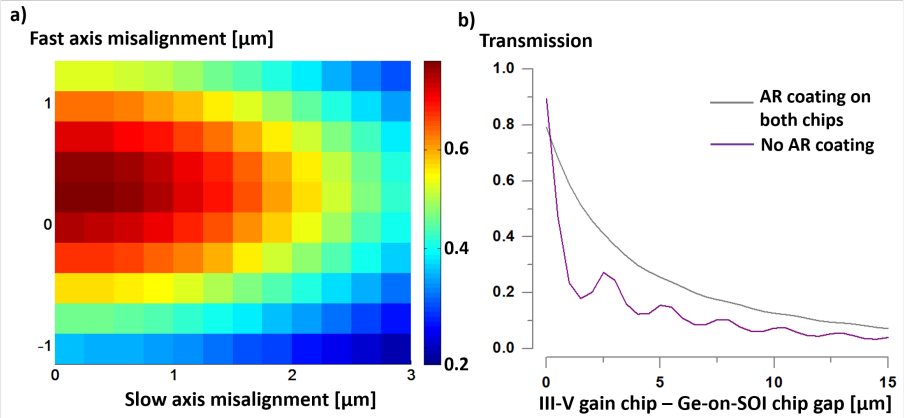

Figure 3.10: A simulation of horizontal alignment between the III-V active region ridge waveguide and the Ge-on-SOI input waveguide (a). For optimally aligned waveguides, we have performed a simulation of coupling efficiency depending on the gap between the waveguides (b).

ficiency between the gain chip and a Ge-on-SOI chip with and without AR coating on the two facing facets. The simulations are performed assuming perfect one-layer AR coatings for the two layer stacks at 5.1 µm wavelength. On Fig. 3.10b we see that while the maximum butt-coupling between the chips is higher in the case without AR coatings, the simulations show that butt-coupling is less sensitive to the gap between gain-chip and Ge waveguide when AR coatings are present. This is due to the Fabry-Perot effect caused by reflections of the interfaces in the case of no AR coatings present. The maximum butt-coupling of the chips with AR coatings is 80% with 3 dB less coupling for a gap of 2.5 µm between the two chips, while maximum coupling without AR coatings is 90% with already 3 dB less coupling for a gap of 0.5 µm.

3.6 Conclusion

Because of the small cross-section of on-chip waveguides, the coupling of light between a waveguide and an optical fiber is an important issue. Our simulations showed that fiber-chip endfire coupling efficiency remains low even after optimization of the waveguide cross-section. To solve the light coupling issue, we demonstrated efficient grating couplers for both Ge-on-Si and Ge-on-SOI platforms. Besides for high coupling efficiency, grating couplers are beneficial for wafer-level testing of integrated optical devices. Nevertheless, for broadband applications, grating couplers can limit the wavelength range of operation. In this chapter we presented efficient grating couplers for circuit testing and edge cou-

plers for the laser readout and coupling of light between the gain-chip and the Ge waveguide. In the next chapters, we will discuss the components and circuits characterized using these interfaces.

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4

Germanium Waveguide Filters in the 5 μm wavelength range

4.1 Introduction

To implement chip-based wavelength-selective optical feedback to a quantum cascade gain chip, we have considered several types of filters. Mach-Zehnder Interferometers (MZIs) in a cascaded formation make a continuously tunable filter, however with limited wavelength discrimination. An advantage of this filter is the straightforward fabrication with contact lithography. Another filter that benefits from relatively straightforward fabrication is an arrayed waveguide grating (AWG) combined with MZI switches used to select feedback from only one of the AWG ports. Due to the fact that the AWG itself is not tuned, this filter allows only for discrete tuning. Besides the filters fabricated by contact lithography, we also considered filters for whose fabrication DUV or e-beam lithography is needed. These filters are based on distributed Bragg reflectors (DBRs) or racetrack resonators. The DBR filters have a large FWHM and FSR, while the racetrack resonators have low values for both of these parameters. Due to low FSR of the racetrack resonator filters, we combined two racetrack resonators in a Vernier configuration to extend the wavelength tuning range of the external cavity quantum cascade laser formed with this filter. In this chapter we will discuss these passive photonic integrated filters in detail. The filter circuits were simulated, fabricated and measured for the purpose of this thesis, that is to use them to provide wavelength-selective feedback to a quantum cascade gain chip. The fabrication processes are explained in detail

in Chapter 3. The fabricated PICs were characterized on measurement setups that were assembled in the course of this thesis.

4.2 Measurement Setup with a Wavemeter

The setup used in measurements of MZI and AWG waveguide circuits is shown in Fig. 3.1 in Chapter 3. When measuring circuits which contain components whose characteristics change fast as a function of wavelength (e.g. racetrack resonators) we need to monitor the wavelength precisely due to the laser wavelength instability explained in the Introduction chapter. The measurement setup used for racetrack resonator measurements is an upgrade of the setup explained in Chapter 3. The setup schematic is shown in Fig. 4.1. For wavelength monitoring purposes we insert a CaF_2 beam splitter before the polarization controller and the chopper. The light reflected by the CaF_2 beam splitter is sent to an FTIR. The spectrum recorded on the FTIR is fitted with a Lorentzian curve for precisely determining the laser wavelength. This way, the FTIR works a wavemeter.

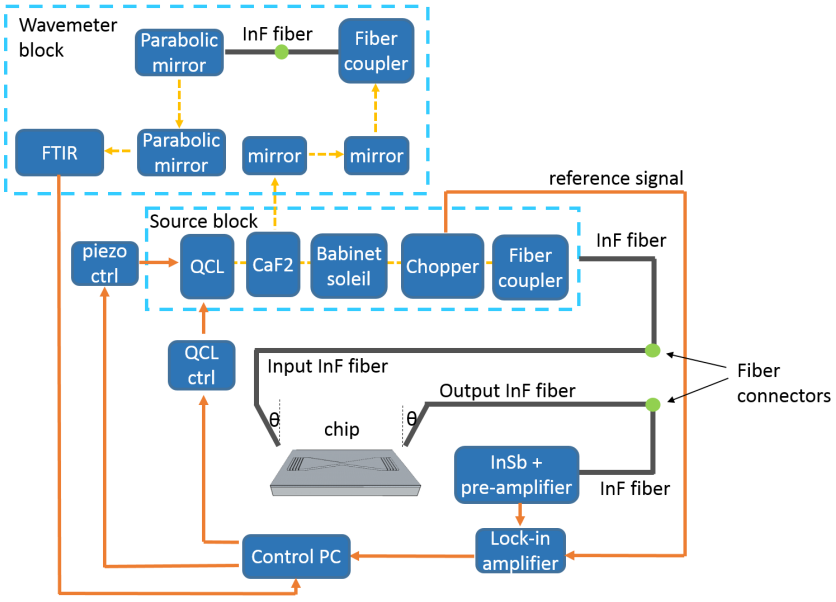

Figure 4.1: The measurement setup with a wavemeter.

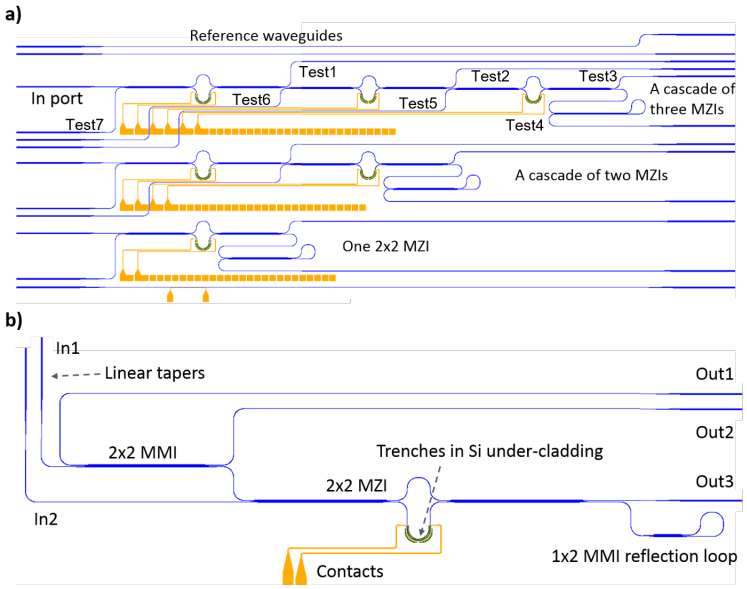

Figure 4.2: Cascades of MZIs (a) and a single MZI reflector circuit used to test the concept with labeled input and output ports (b).

4.3 Cascaded Mach-Zehnder Interferometer

4.3.1 Design

A Mach-Zehnder interferometer (MZI) can use directional couplers or multi-mode interferometers (MMIs) to split/combine power to/from the MZI arms. When one of the arms is longer than the other, this causes a wavelength dependent phase delay, resulting in a sinusoidal tranmission function as a function of wavelength. The FSR of a MZI is:

$$FSR = \frac{\lambda^2}{n_g \Delta L} \tag{4.1}$$

where ΔL is the difference in length of the MZI arms, n_g is the group index of the guided mode and λ is the center wavelength. The FSR is inversely dependent on ΔL - decreasing ΔL will increase the FSR. In the cascaded MZI configuration, every subsequent MZI in the chain has halve the path length difference of the previous MZI , which doubles its FSR compared to the previous one. By aligning the transmission peaks of the different MZIs at a certain wavelength, maximum transmission is obtained for this wavelength and transmission peaks at other wavelengths are suppressed. The simulations for three cascaded MZIs, where the first

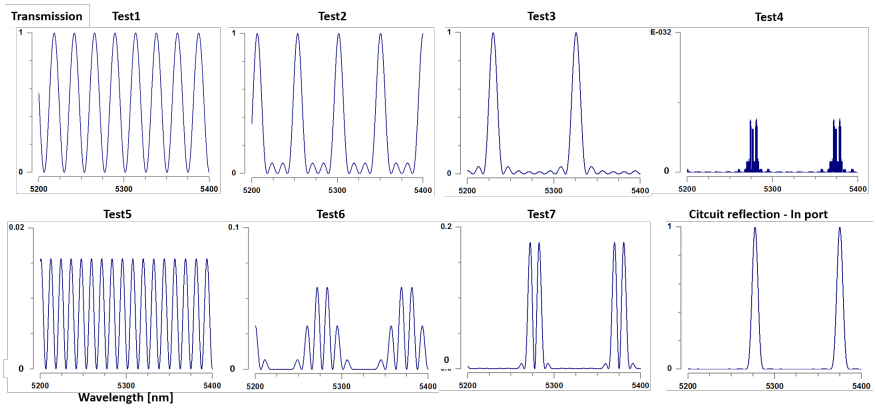

Figure 4.3: Simulation of three cascaded MZIs. The ports correspond to the schematic in Fig. 4.2a).

MZI's ΔL is 300 μm (FSR = 23.4 nm) is shown in Fig. 4.3. The simulations correspond to the input and test ports of three cascaded MZIs, labeled in Fig. 4.2a), when light with a normalized input power of 1 is coupled in the 'In port'. The test ports 'Test4', 'Test5', 'Test6' and 'Test7' are used to thermally align the three MZIs, by minimizing the signal on these ports for the wavelength we want to keep in the circuit. The FWHM of the light reflected back to the 'In port' is 8 nm. The idea is that the quantum cascade gain chip is butt-coupled to the port labeled 'In port', the light passes through the thermally tunable MZI cascade, gets reflected by the loop mirror, which reflects the light back towards the 'In port' (Fig. 4.2a).

We have worked on the MMI configuration to build 2x2 MZIs. 1x2 MMIs are 230 μm long while 2x2 MMIs are 930 μm long. The rest of the MMI parameters are the same: a 25 μm wide MMI region, using 11 μm wide access waveguides (with 100 μm long tapers) and a 3 μm space between them.

The circuit used to test the concept of the loop mirror is shown in Fig. 4.2b). Fibers are coupled to 15 μm wide waveguide facets which are tapered down to single mode waveguides (2.2 μm wide). The tapers are linear and 500 μm long. An input MMI is inserted before the MZI, to read out the reflection signal, that would finally be used for setting the wavelength of the gain chip. Since this component brings additional -6 dB of losses in a round trip, it should be excluded from the final design. In this case, we would rely on the ports 'Out2' and 'In1' to tune the MZI wavelength, and hence align MZIs in a cascaded configuration. Input and output waveguides are implemented at 90^0 to avoid cross-coupling between the fibers.

The circuit is fabricated on the Ge-on-3.2 μm SOI platform, by contact lithography and fully dry etched by $CF_4/SF_6/H_2$ plasma. We proceeded with inverse

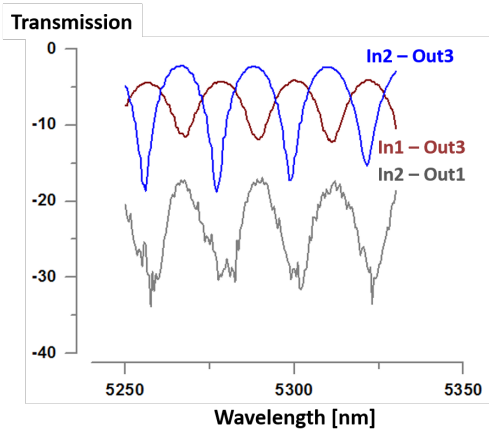

Figure 4.4: One MZI reflection circuit measurements.

heater definition, where we first define the trenches in the Si device layer and locally under-etch the circuit, and then we deposit the metal heaters and contacts. The sample is thinned down to 350 μm and cleaved. A TiO_2 AR coating is deposited on both facets. Finally, 300 nm of IR-F625 top cladding is evaporated by e-gun and annealed at 250^0C in a N_2 rich environment.

4.3.2 Measurement Results

The measurements are performed on the horizontal setup described earlier, where the light from the QCL is guided by fibers that are butt-coupled to the chip. The TM waveguide losses measured on the chip are 3.5 dB/cm at 5310 nm wavelength. The measurements are shown in Fig. 4.4. All measurements are shown relative to 'In1 - Out2' transmission (+ 3dB because the light passes through a 2x2 MMI). The total losses for a round trip ('In1 - Out1' measurement) in this reflector circuit, are ˜17 dB. The light is sent through the 'In1 port' and it passes twice through a 2x2 MMI which makes for 6 dB loss. From the 'In2 - Out3' measurement we estimate a 2x2 MZI insertion loss of 2 dB, which in a round trip makes 4 dB. The waveguide length from port 'In1' till 'Out2' is ˜1 cm, while the distance that the light travels from 'In1' till 'Out1' is three times longer, which brings another -7 dB due to propagation losses over additional 2 cm. So, the input 2x2 MMI, MZI insertion loss and the circuit length explain the losses plotted in Fig. 4.4. Although the input 2x2 MMI can be left out of the final circuit, a bigger issue is circuit size. Large MMIs are chosen to meet fabrication tolerances of the contact lithography [1].

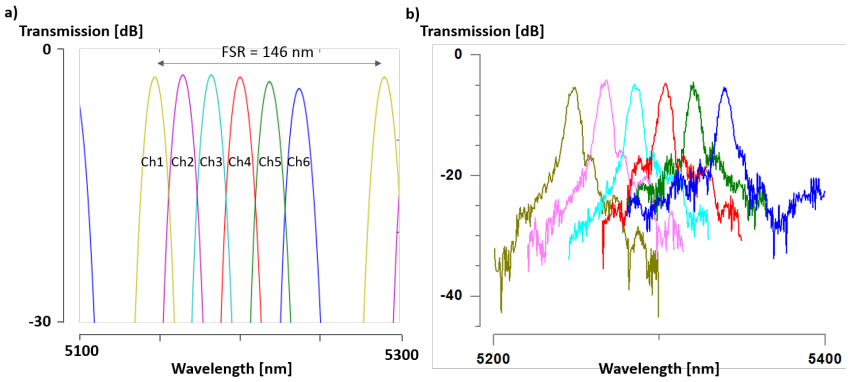

Figure 4.5: Simulation of the AWG response (a) and measured AWG transmission (b).

4.4 Arrayed Waveguide Grating with MZI switches

4.4.1 Design

An arrayed waveguide grating (AWG) is a component used for wavelength multiplexing and demultiplexing. An AWG consists of input and output waveguides, followed by two wide slab regions called free propagation regions or star couplers and an array of waveguides connecting these two star couplers. Light is launched from an input waveguide towards the input star coupler, where it diverges due to free propagation in the slab. After arriving on the waveguide array, the divergent beam couples in the array waveguides, which are designed to keep constant length difference (ΔL) between two consecutive arms of the array. After the output star coupler, depending on the phase difference between the different waveguide arms, the light will interfere constructively in different points. At this position we place the output waveguides. All waveguides from the array are in phase when λ_c = $n_{eff}\Delta$L/m, where n_{eff} is the effective index of the mode in the waveguide and m is the diffraction order. The FSR of the multiplexer is given by $\lambda^2/n_g\Delta$L, where n_g is the group index of the mode guided in the arrayed waveguides.

The AWG used in this work is designed with an aperture width of 4 µm and a linear 90 µm long taper connecting the aperture and the single-mode waveguide. The arrayed waveguides' aperture is also 4 µm wide with 1 µm space between two consecutive waveguides (5 µm pitch), and with 175 µm long tapers. From the waveguide aperture width - pitch ratio we estimate that insertion losses will be $>20\%$. To reduce losses caused by propagation, the 36 arrayed waveguides are expanded in straight sections to 4 µm wide multi-mode waveguides, using 25 µm long tapers. The bending radius of the arrayed waveguides is 75 µm. ΔL is 46 µm, which sets the channel spacing to ˜18 nm and the FSR to 146 nm. Simulations of

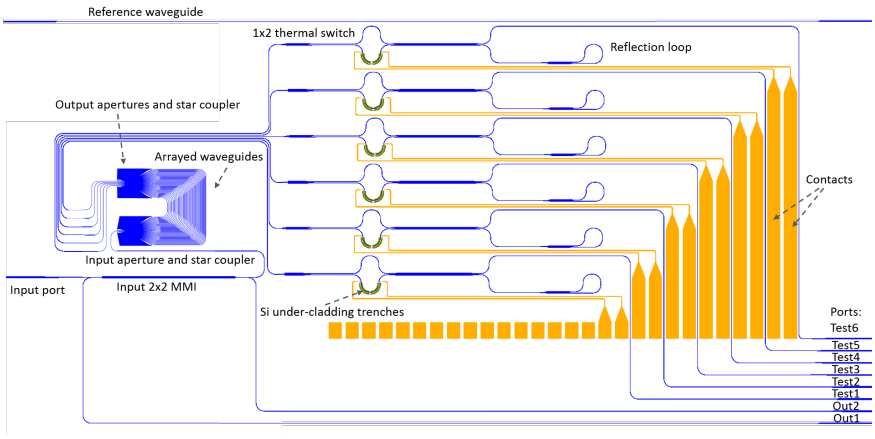

Figure 4.6: AWG with MZI switch circuit.

the AWG performance are shown in Fig. 4.5(a).

The circuit we are building to provide wavelength selective feedback for the gain chip, has to have the possibility to switch on and off individual AWG channels. Therefore each output waveguide of the AWG has a thermal 1x2 MZI switch with a ˜400 µm long heater. The MMIs used here are the same as in the case of the cascaded MZI circuits. After the switch, there is a 1x2 MMI with a loop that returns the light towards the input waveguide. An AWG channel can be switched 'ON'or 'OFF' by the MZI switches. By setting only one of the channels to the 'ON' state, we can build a discrete feedback for the gain chip.

To test this concept, we have first fabricated an AWG on the Ge-on-Si platform. Once we tested the fabrication on the Ge-on-Si platform, we have switched to the Ge-on-SOI platform to implement more complicated structures, including the thermo-optic switches. The complete circuit (Fig. 4.6) is fabricated on Ge-on-3.2 µm SOI. Fully etched waveguides are formed by contact lithography and $CF_4/SF_6/H_2$ plasma. For the Ge-on-SOI chip, the heaters are deposited on the Si under-cladding, and trenches in Si are etched around the heaters. The Ge-on-Si chip is without heaters. Finally, the chips are lapped to 350 µm and cleaved. An AR coating is deposited only on the facets of Ge-on-SOI chip.

4.4.2 Measurement Results

The measurement of five channels of the AWG implemented on the Ge-on-Si platform, is shown in Fig. 4.5b). The insertion loss is -5 dB, referenced to a straight waveguide. For the Ge-on-SOI chip, the AWG measurements are plotted relative to the 'Input' - 'Out2' transmission. The heaters on the Ge-on-SOI platform require 200 - 250 mW for a 2π-shift. An example of an AWG channel in 'ON' and

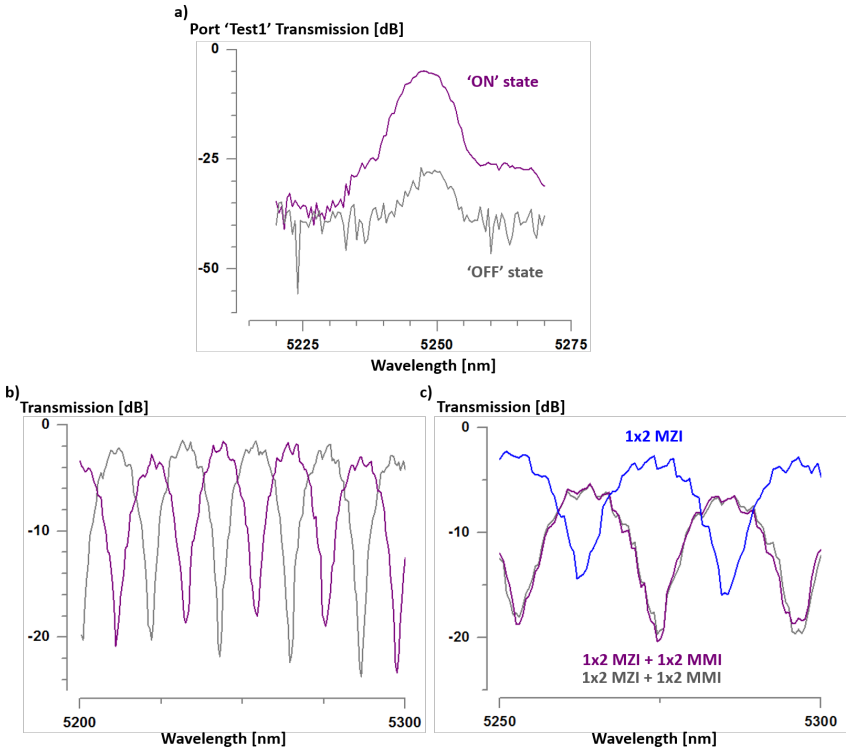

Figure 4.7: AWG channel in 'ON' and 'OFF' state (a). A 1x2 MZI transmission measurement (b) and transmission measurement of a structure consisting of a 1x2 MZI with a 1x2 MMI on one of its output waveguides.

'OFF' state is given in Fig. 4.7a). The FWHM of an AWG channel is 8 nm. The insertion loss in the 'ON' state is -5 dB. Switching off an AWG channel makes a difference of 20 dB in signal intensity. The transmission measurement of a 1x2 MZI and a 1x2 MZI followed by a 1x2 MMI on one of its output waveguides, relative to a straight waveguide, are shown on Fig. 4.7b) and c). However, due to high losses we were not able to test the circuit reflection. The circuit length is ˜1 cm, the AWG insertion loss is -5 dB, while the insertion loss of a 1x2 MZI is $<$ -0.5 dB (-3.5 dB on the graph, where -3 dB comes from the 1x2 power splitting), which means that the losses in a round trip are $>$17 dB, assuming 3 dB/cm propagation loss. In spite of high losses and high FWHM, AWG based filters for QCL wavelength selection could find their application in liquid sensing where absorption characteristic changes less abruptly comparing to a typical gas absorption characteristic.

4.5 Distributed Bragg Reflecting Grating

4.5.1 Design

A distributed Bragg Reflector comprises a periodic variation of the waveguide geometry (in our case the waveguide thickness), resulting in a periodic variation of the effective refractive index of modes. Each boundary between an unetched and etched part of the grating causes a partial reflection of light. The DBRs can be designed to have very high reflection, while maintaining relatively narrow bandwidth and high FSR, which makes them a good filter for liquid sensing. Normally, first order DBRs have maximal reflectivity, which limits fabrication to e-beam or DUV lithography.

The period of a first order grating in a Ge waveguide at 5.3 μm is ˜700 nm. We performed 2D FDTD transmission simulations of gratings with periods from 700 - 760 nm, a fixed duty cycle of 50% and an etch depth of 100 nm. 1500 periods are assumed in the simulation. The simulations are assuming TM polarization and the Ge-on-SOI platform, for which the waveguide supports higher order vertical modes besides TM_{00} (Fig. 4.8a), due to the vertically limited Si under-cladding. The presence of these higher order vertical modes are visible in the grating transmission spectrum (Fig. 4.8b).

The DBR is fabricated on a Ge-on-SOI waveguide platform consisting of a 2 μm thick germanium waveguide layer on a 3.2 μm silicon bottom cladding on top of a 2 μm thick SiO_2 layer. Next, the 10 μm wide multi-mode waveguide is tapered to a 2.2 μm wide single-mode waveguide on both ends. The single-mode waveguides are long enough to suppress multi-mode behavior in lateral direction. The single-mode waveguides are then tapered up to 18 μm to overlap better with the fiber mode. All tapers are linear and 350 μm long. The input and output facets

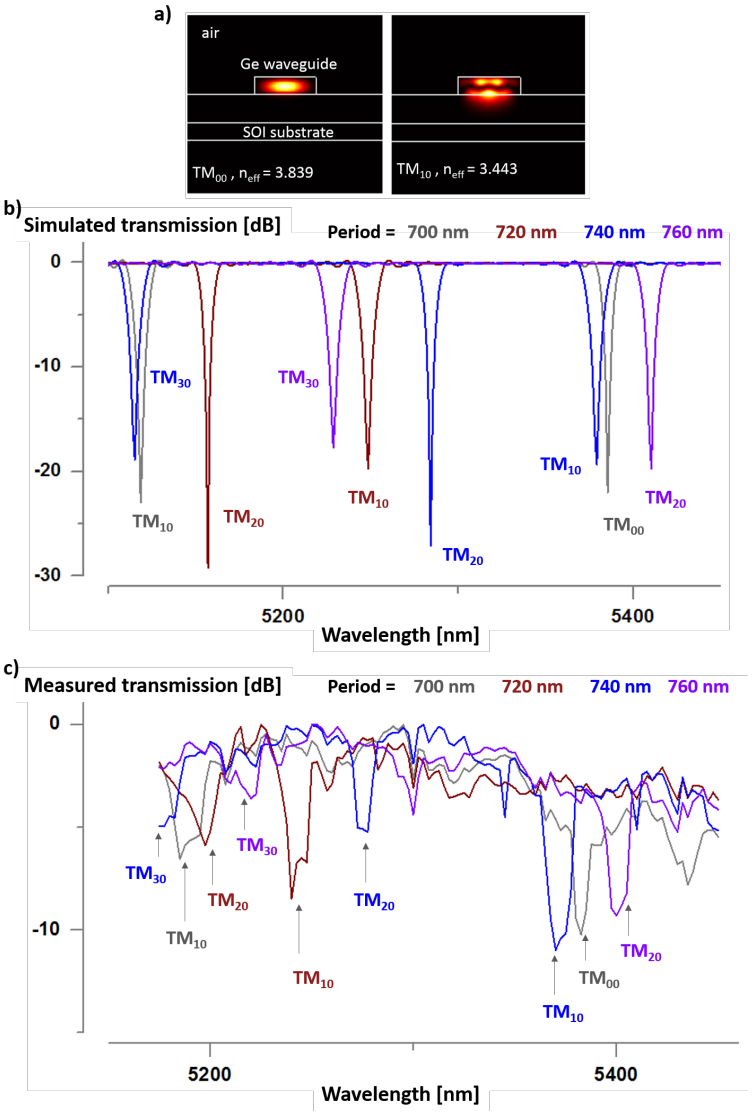

Figure 4.8: A 10 µm *wide Ge waveguide in which the DBR is implemented supports multiple modes in vertical direction (a). The simulation of the transmission of a uniform grating of 1500 periods (b) and the measurement results of a grating with 1500 periods (c).*

are implemented at 90^0 angle to avoid any cross-coupling between the fibers. The grating is patterned by e-beam lithography, 100 nm etched in a 10 μm wide Ge multimode waveguide. The rest of the circuit is defined by contact lithography and fully etched. Both facets are AR coated.

4.5.2 Measurement Results

The measurements are done in the horizontal setup we have described earlier. The DBRs are characterized in transmission. There is an absorption line of the fiber material at 5300 nm. While there is a reasonable match for the position of the dips (Fig. 4.8c), the extinction ratio is somewhat different. The AR coating on the facets keeps the reflections below 1 dB.

4.5.3 Sampled Gratings

Sampled gratings (SG) are used to implement widely tunable distributed Bragg reflector (DBR) [2] and distributed feedback (DFB) lasers [3]. A SG consists of multiple gratings with a period Λ (total length of the grating being Λ_g) repeating periodically with a sampling period Λ_s (Fig. 4.9a). A SG provides a comb-like reflection spectrum (Fig. 4.10), with the spectral interval between two neighboring reflection peaks $\Delta\lambda_s$ given by [4]:

$$\Delta\lambda_s = \frac{\lambda_B^2}{2n_g\Lambda_s} \tag{4.2}$$

, where $\lambda_B = 2n_{eff}\Lambda$ for the first order grating. n_g and n_{eff} are group and effective index of the grating. A larger sampling period Λ_s will result in a larger interval between two neighboring reflection peaks $\Delta\lambda_s$, and vice versa. Simulations show that it is possible to design a sampled grating with an FSR of 500 nm, which is enough to form a single mode thermally tuned distributed Bragg reflector laser with a broadband QCL we described in the introduction (Fig. 4.9b). However, in this case we would have to dissipate a lot of power to tune the Ge waveguide filter over 500 nm. Therefore, it is necessary to combine at least two SGs (Fig. 4.9c). In Fig. 4.10 we show simulation results of two SGs combined in a serial configuration. We used CAMFR software for the simulations. The sampling periods of the two SGs, are set to be slightly different, such that multiplying the spectra of the two SGs gives a combined FSR of 430 nm. Parameters of Grating1 are: Λ =680 nm, N_g =3, N_s =12 and Λ_s =39.7 μm. For Grating2 we have: Λ =670 nm, N_g =3, N_s =16, Λ_s =32.675 μm. Both gratings are etched 900 nm deep and have a 50% duty cycle. The individual FSRs of Grating1 and Grating2 are 75 nm and 95 nm at 5 μm wavelength. The lengths of these gratings are around 660 and 500 μm. Due to deep etching, which determines reflection strength, the FWHM of the filter is $>$10 nm.

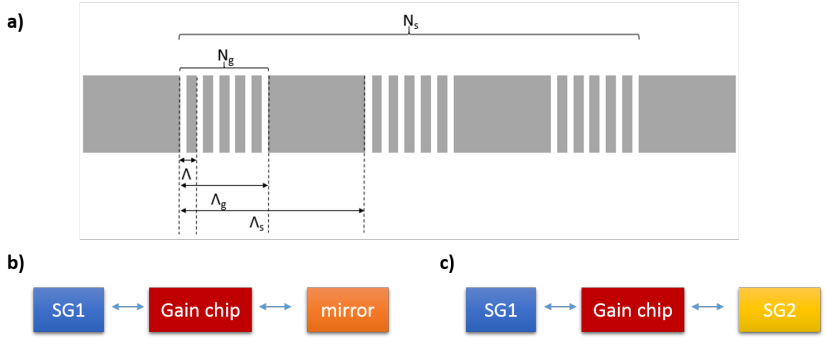

Figure 4.9: A SG (a) and SG-DBR configurations: one SG and a 100% reflecting mirror are providing the feedback to the laser (b) and two SGs in vernier configuration (c).

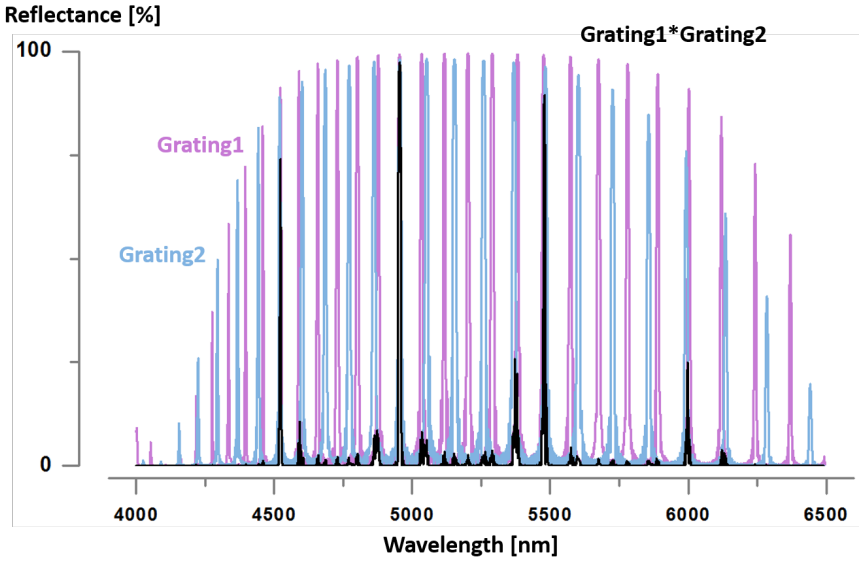

Figure 4.10: A simulation of the reflection of two sampled gratings combined in serial configuration.

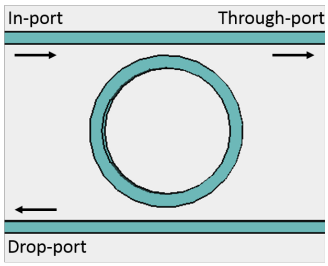

Figure 4.11: A ring/racetrack resonator with labeled ports.

4.6 Racetrack resonator

4.6.1 Design

A ring/racetrack resonator consists of a closed circular waveguide - a loop, and one or two waveguides coupled to it. It is an interferometric filter, which resonates for wavelengths whose phase change is an integer multiple of 2π after each trip around the loop. A ring resonator has a point coupler, while a racetrack resonator has a coupler of a finite length. Carefully designed resonators can have low FWHM, which makes these devices suitable for gas sensing application. However, FSR could be insufficient to form a single-mode QCL when deployed as a wavelength selecting element.

Resonant peaks can be observed in the drop port, while dips in transmission can be measured in the through port (Fig. 4.11). The racetrack resonators have a transmission to the through port T_p and the drop port T_d given by [6]:

$$T_p = \frac{t^2a^2 - 2t^2a\cos\phi + t^2}{1 - 2t^2a\cos\phi + t^4a^2} \tag{4.3}$$

$$T_d = \frac{(1-t^2)^2a}{1 - 2t^2a\cos\phi + t^4a^2} \tag{4.4}$$

where t is the self-coupling coefficient. It is related to the cross-coupling coefficient κ by $\kappa^2 + t^2 = 1$. a is the single-pass amplitude transmission of the racetrack resonator defined by $a = \sqrt{e^{-\alpha(2\pi r+2L)}}$, where r and L are the racetrack radius and the coupler length and α is the power attenuation coefficient. As light circulates inside the resonators while only small portion of it is coupled to the drop port, attenuation coefficient is crucial for high Q-factor. $\phi = \beta(2\pi r + 2L)$ is the single-pass phase shift, with β being the propagation constant of the circulating mode. The racetrack resonator free spectral range (FSR) is determined by $FSR = \frac{\lambda^2}{n_g(2\pi r+2L)}$, with n_g the group index. The FSR is limited by bend radius, which should be 75 μm for our platforms to avoid loses. Typical values for FSR of our racetracks is ∼10 nm.

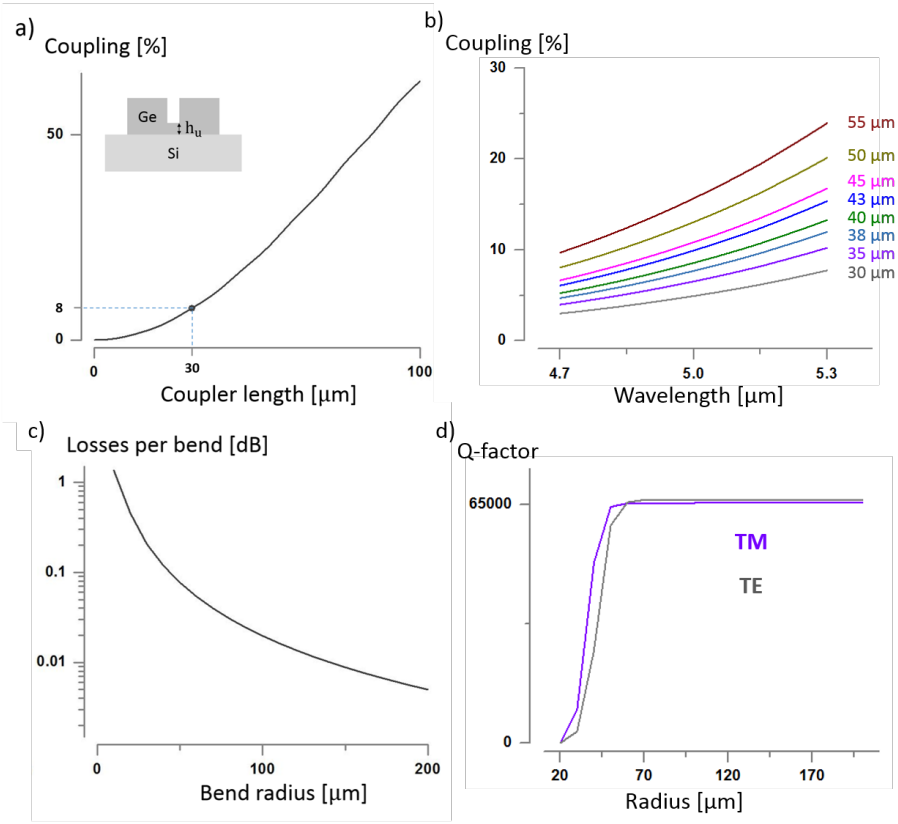

Figure 4.12: Coupling to the racetrack resonator as a function of the coupler length (a) and the radiative losses per 90^o bend (b). Theoretically calculated Q-factor assuming 3 dB/cm scattering losses (c).

The Ge-on-SOI single mode waveguide structures were chosen to be 2.2 µm wide and fully etched through the 2 µm thick Ge waveguide layer, while the gap between the racetrack resonator and bus waveguide was chosen to be 0.5 µm. The simulated power coupling efficiency as a function of coupler length (TM-polarization), calculated using a full-vectorial FDE tool is shown in Fig. 4.12a). Due to the etching process we used, the Ge layer is not fully etched in the coupler region, leaving a slab of h_u = 450 nm. The simulated coupling efficiency for a coupler length of 0 µm is $< 0.1\%$, which indicates that the coupling in the bends is negligible. This increases to 8% for a coupler length of 30 µm. However, coupling efficiency depends strongly on the wavelength. Coupling efficiency for different coupler lengths, and fixed coupler gap of 500 nm and h_u = 450 nm for the wavelength range from 4.7 - 5.3 µm is displayed on Fig. 4.12b.

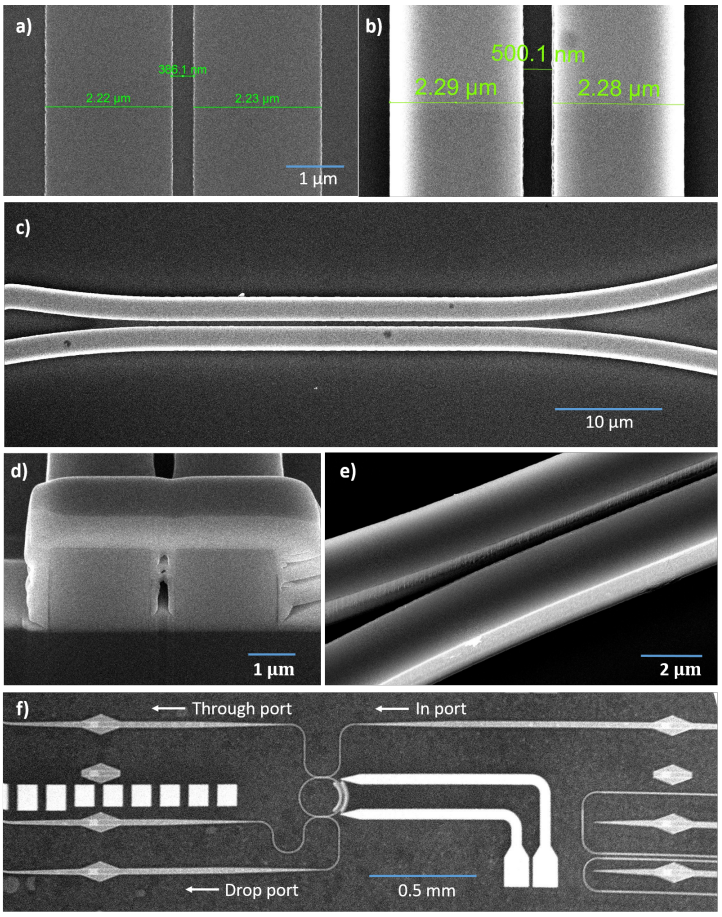

Figure 4.13: A racetrack coupler metal mask before etching (a) and after full etching and mask removal (b). The coupler gap was defined to be 450 nm, and after the etching it broadened to 500 nm. Top view of the etched coupler (c), the coupler side-walls (d) and the coupler cross-section in the straight part of the coupler (e). The cladding-like structure on the cross-section image is platinum that was deposited to protect the waveguides while making a focused ion beam cross-section of the waveguide. Full circuit (f).

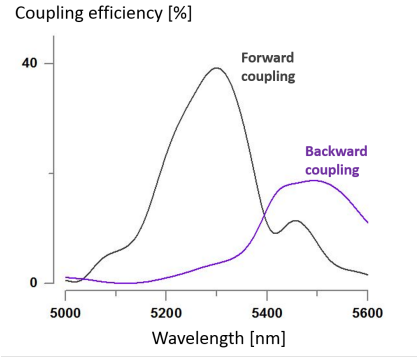

Figure 4.14: The simulations of forward and backward coupling to the waveguide by the grating coupler.

The bend radiation loss per 90 degree bend of the fully etched waveguide at a wavelength of 5.3 μm is shown in Fig. 4.12c) as a function of bending radius. The bend radiation loss consists of propagation losses and losses due to the interface between the straight waveguide and the bend, which are more dominant. Based on the simulated bend losses we can estimate a theoretical unloaded Q-factor of the resonator [6]:

$$Q = 4.3\frac{2\pi n_g}{\lambda}\frac{1}{Loss_B[dB/cm] + Loss_S[dB/cm]} \tag{4.5}$$

where Loss_B is the loss caused by the bends, which we can simulate, and Loss_S is the scattering loss. The Q-factor calculated assuming scattering losses of 3 dB/cm for TM and TE polarization is shown in Fig. 4.12d).

The racetrack resonators were fabricated using e-beam lithography as discussed earlier. SEM images of the fabricated device is shown on Fig. 4.13. Grating coupler structures were used to characterize the devices. The grating coupler structures interface with a single mode InF fiber [7] at 5.3 μm wavelength and are etched 1 μm deep, have a grating period of 1.45 μm and a grating duty cycle of 0.8 (duty cycle being the ratio of the width of the unetched part and the period). 30 periods were implemented to have a good coupling efficiency to the InF fiber with a mode field diameter of 18 μm. The fiber is tilted 5 degrees off-normal. The simulated coupling spectrum in both forward and backward direction, when launching the fiber mode, is shown in Fig. 4.14. The small fiber angle causes some coupling of light in the backward direction, which in case of an abrupt termination of the waveguide causes back-reflections and interference. Therefore, in order to reduce the reflections, the waveguide in the backward direction is tapered down, as can be seen from the SEM pictures.

4.6.2 Measurement Results

The transmission is measured using a vertical setup with a wavemeter, which we have described earlier in this chapter. An example of a racetrack resonator through port spectrum is shown in 4.15. The characterized racetrack has coupler length of 30 μm, coupler gap of 500 nm and h_u = 450 nm. The loaded Q-factor is 32000 at 5309.5 nm wavelength. Although the coupling between bus waveguide and racetrack resonator changes with wavelength, which influences the critical coupling, similar Q-factor (>30000) is measured at nearby resonances. The FSR of the resonator is ˜9 nm.

In Table 4.1 we list the parameters of the racetrack resonators we have tested, together with the loaded Q-factors measured. The best characterized racetrack with bend radius of 100 μm, 30 μm long coupler with a coupler gap of 400 nm has Q-factor of 32000 around 5.3 μm wavelength. In the next section we show racetracks with the same parameters that have Q-factors around 20000. This illustrates sensitivity of Q-factor on fabrication imperfections. The dry etching of the device leaves more side-wall roughness in the coupler gap comparing to the etching of stand-alone structures (Fig. 4.13e). This effect leads to higher losses and lower coupling coefficient. The etch lag effect in the coupler gap is not easily controlled which leads to changes in h_u value, which in return changes coupling coefficient and consequently the Q-factor itself.

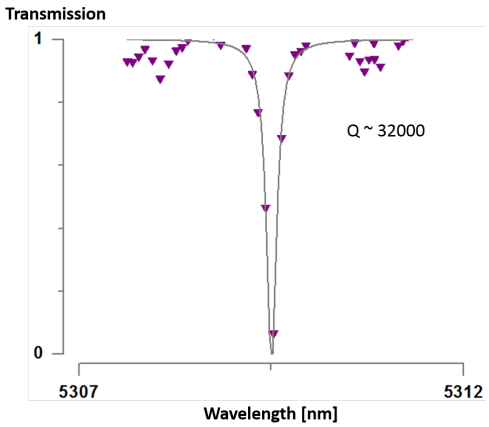

Figure 4.15: Racetrack resonator with a measured loaded Q-factor of 32000.

Radius [μm]	Coupler length [μm]	Coupler gap [nm]	Wavelength [nm]	Loaded Q-factor
100	30	400	5309.5	32000
100	40	400	5231	9000
100	40	400	5266	8000
100	43	400	5275	5000
75	35	400	5310	10000
75	45	400	5300	8000
75	55	400	5323	8000
50	50	400	5321	8000

Table 4.1: Characterized racetrack resonator resonances for Ge-on-3.2 μm SOI

4.7 Racetrack resonator Vernier filter

4.7.1 Design

In Fig. 4.16b) we show the device structure under study used to validate the functionality of a tunable Vernier filter on the Ge-on-SOI platform in the 5 μm wavelength range. Two racetrack resonators are implemented on the Ge-on-SOI waveguide platform with a 2 μm thick germanium waveguide layer on a 3.2 μm silicon bottom cladding and a 2 μm thick SiO_2 layer. Heaters are implemented on the side of the Ge waveguide. Fiber-to-chip grating couplers are used to interface with the PIC.

FSR_V, the free spectral range of the Vernier filter realized by cascading the

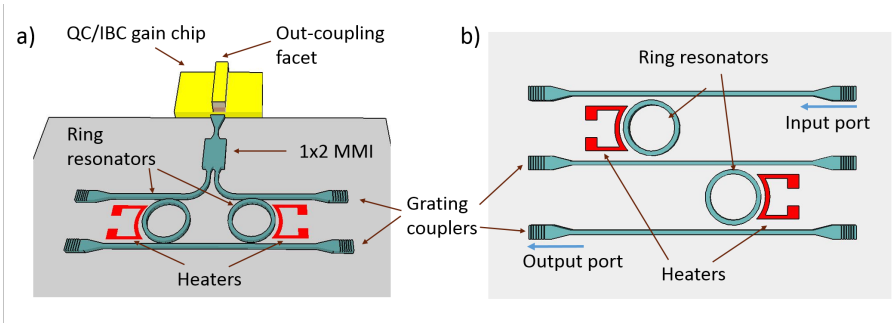

Figure 4.16: A widely tunable external cavity QCL/ICL without any moving parts: the rotating grating is replaced by a tunable reflector on a chip. The tunable filter consists of a beam combiner/splitter and a Vernier ring resonator filter in a loop configuration (a), a tunable Vernier filter based on racetrack resonators that was used in the experiment (b).

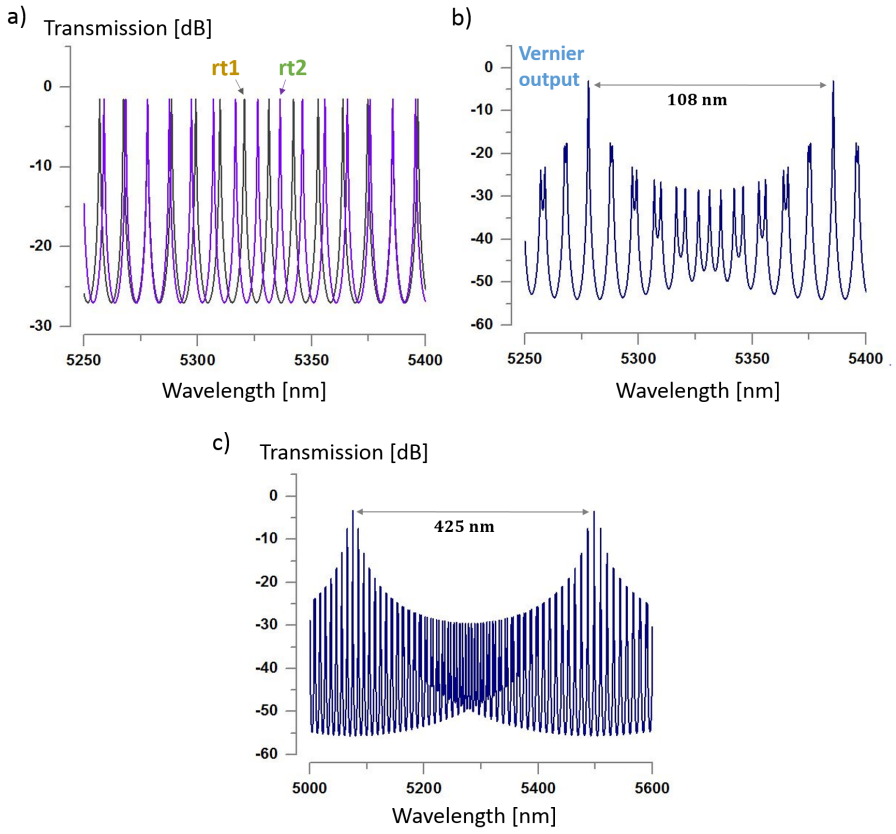

Figure 4.17: The simulated drop port spectra T_d of individual racetrack resonators (a) and the transmission of the Vernier filter built with these racetrack resonators (b). Simulation of a larger FSR_V Vernier filter (c).

individual resonators, depends on the individual FSRs of the racetrack resonators:

$$FSR_V = \frac{FSR_1 FSR_2}{FSR_1 - FSR_2} \tag{4.6}$$

The simulated drop port spectrum T_d of individual rings with a radius of 100 µm and 110 µm is shown in Fig. 4.17a, assuming a coupler length L = 30 µm, while in Fig. 4.17b the combined transmission of the Vernier filter is plotted. Here we assumed a group index $n_g = 4.2$, $t = 0.96$ and $a = 0.98$.

In this design, FSR_1 and FSR_2 are 9.7 nm and 8.9 nm respectively in the 5 µm wavelength range, leading to a combined FSR_V of 108 nm and the side-peak suppression is >15 dB. The transmission of the Vernier filter reaches a maximum where the resonant peaks of the individual racetrack resonators overlap, which

determines the lasing wavelength of the external cavity laser. By thermally adjusting the position of the overlapping transmission peaks the lasing wavelength can be tuned. The tuning range is limited by FSR_V. This free spectral range can be extended by reducing the difference in FSRs of the individual racetrack resonators. Using ring resonators with the same loaded Q-factor (˜20.000 in the example above), but with a radius of 100 µm and 102.5 µm respectively, a combined free spectral range FSR_V of 425 nm can be obtained at the expense of a reduced side-peak suppression of 4 dB (Fig. 4.17c).

A combination of electron-beam lithography and optical lithography is used to define the Ge-on-SOI waveguide circuit, comprising a 1 µm deep etch for the grating couplers and a 2 µm deep etch for the waveguide structures and racetrack resonators. The grating coupler design is the same as the one used in the previous section. The e-beam write field is 500 µm by 500 µm, which allows accommodating the racetracks in a single write field and hence avoid degradation of the Q-factor by stitching errors. On other places where we cannot avoid stitching, we are expanding the waveguides to a width of 5 µm as they incur less losses when stitching errors occur. A SEM general overview of the Vernier filter circuit is shown in Fig. 4.18.

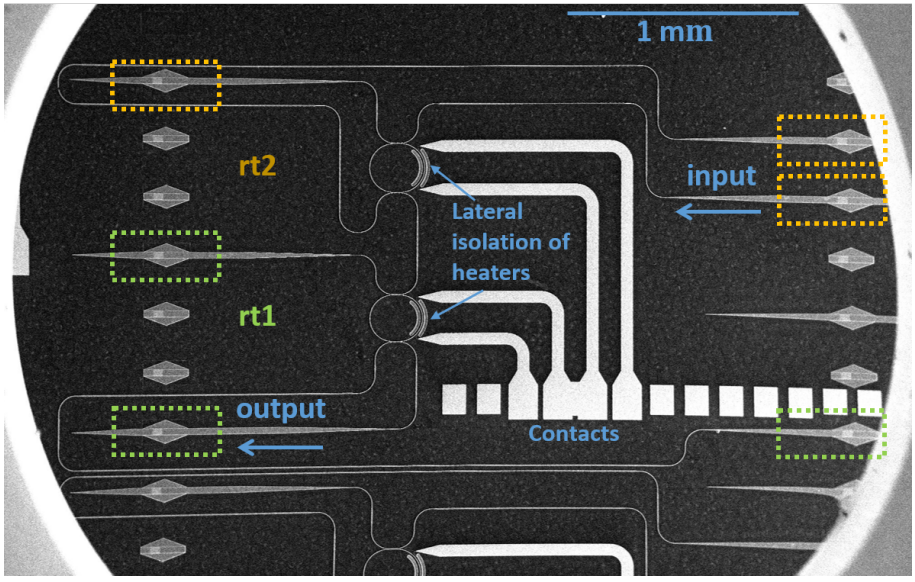

Figure 4.18: The chip layout: the two racetrack resonators in a Vernier configuration with ports that allow to measure the response of each individual resonator.

For the experiment, we have chosen to realize a Vernier racetrack resonator tunable filter based on resonators with a radius rt_1 and rt_2 of 100 µm and 110 µm

respectively, while the length of the coupler L was chosen to be 30 μm in both resonators. In this case the tunable filter could be characterized over an entire FSR_V of 108 nm with the available continuous wave QCL operating in the 5.25-5.4 μm wavelength range. The chip layout (Fig. 4.18) allows us to test the racetrack resonators used to build the Vernier filter individually using the grating coupler ports marked in green in case of racetrack 1 (rt_1 = 100 μm) and the grating coupler ports marked with orange squares for racetrack 2 (rt_2 = 110 μm), as well as the complete Vernier filter.

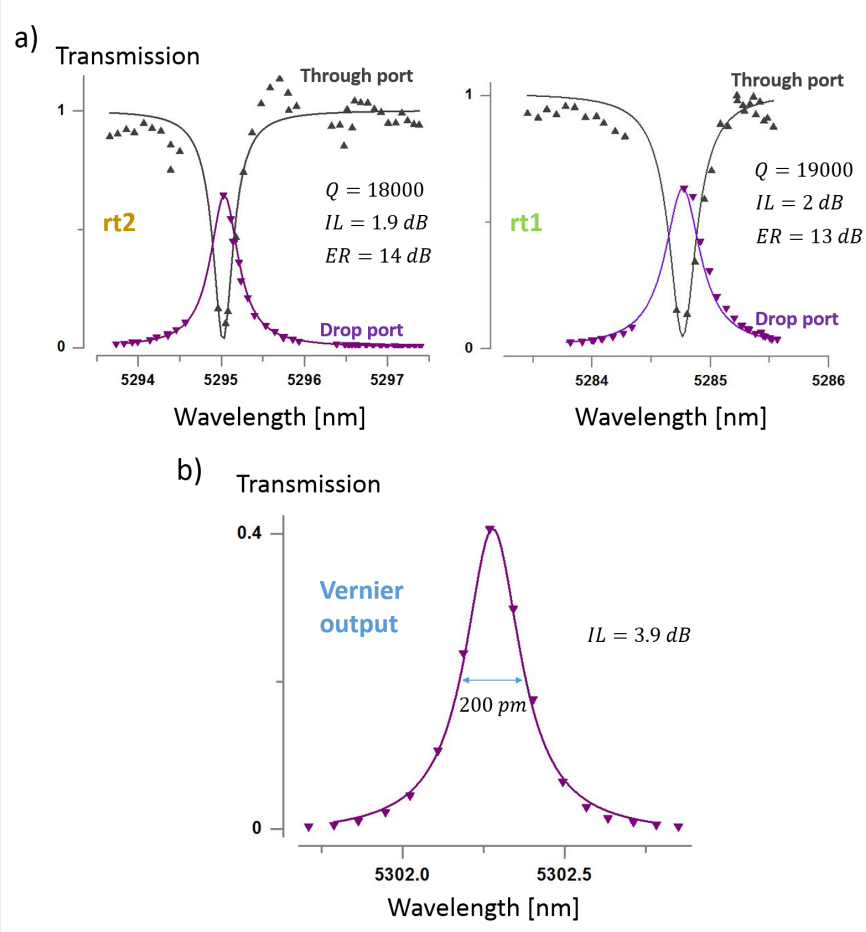

Figure 4.19: Measured and fitted transmission of the through and drop port of the individual racetrack resonators when not heated (a), and of the Vernier filter when aligned by heating one of the racetracks (b).

4.7.2 Measurement Results

The measured transmission spectra of the through and drop ports of the individual racetrack resonators are shown in Fig. 4.19a), showing a loaded Q-factor of 18000 and 19000 respectively. The measured extinction ratio (ER) is 14 dB and 13 dB, respectively, while the insertion loss (IL) is 1.9 dB and 2 dB. The full width at half maximum (FWHM) of the Vernier filter for a case where the resonance wavelengths of both racetrack resonators are aligned is 200 pm, while the IL is 3.9 dB.

For $r = 100\mu m$ and $L = 30\mu m$, the parameters we get from the fitting of the racetrack resonator spectra are $t = 0.96$ and $a = 0.98$ corresponding to waveguide loss of 2.5 dB/cm. An FSR_V of 108 nm is experimentally obtained.

By thermally tuning one of the racetrack resonators the position of the overlapping transmission peak can be tuned in steps of the FSR of the other resonator. This way, discrete tuning of the filter can be realized as shown in Fig. 4.20a). Accessing wavelengths in between resonances of the resonator that was not tuned, can be achieved by tuning both racetrack resonators at the same time. This is illustrated in Fig. 4.20b). To access any arbitrary wavelength within the FSR_V of the Vernier filter the total power dissipation of the filter is less than 500mW. The side-peak suppression of the filter transmission is more than 20 dB.

In order to assess the temperature dependence of the filter, transmission spectra of racetrack 2 were characterized at different stage temperatures. The resonant wavelength shift as a function of stage temperature, given by

$$\Delta\lambda = \frac{dn}{dT}\frac{\lambda}{n_g}\Delta T \tag{4.7}$$

is shown in Fig. 4.21a).

A thermo-optic coefficient of $501.3 \pm 12.5\frac{pm}{^oC}$ is measured, which is close to the calculated value of $520\frac{pm}{^oC}$, using the Ge thermo-optic coefficient of $\frac{dn}{dT} = 4.2 \times 10^{-4}K^{-1}$ at 5.2 μm wavelength [8].

The racetrack resonator response time to a step in the heater voltage is shown in Fig. 4.21b. For this experiment the laser wavelength was aligned with a resonance of the ring resonator, after which a step function in the heater current was applied which detunes the resonance from the laser wavelength and results in a drop in transmission at the drop port. Assuming a first order response of the resonator detuning and taking into account the Lorentzian line shape of the resonance with a full width at half maximum $FWHM$, we have:

$$I_N = \frac{1}{1 + (\frac{2*\Delta\lambda*(1-e^{-t/\tau})}{FWHM})^2} \tag{4.8}$$

where I_N is the normalized power transmission, $\Delta\lambda$ is the steady state change in the resonator wavelength from an ON-resonance state to an OFF-resonance state

and τ is the time constant. $\Delta\lambda$ is obtained by comparing the applied step in the heater power dissipation with the power needed to tune over the FSR of the resonator. By fitting, we get a time constant of 125 μs.

4.8 Conclusion

In this chapter we have considered several filters on the Ge-on-Si and Ge-on-SOI platforms. Some filters benefit from simple fabrication (cascaded MZIs and AWGs) while other need DUV or e-beam for the fabrication (grating and racetrack based filters). However, the e-beam fabricated filters offer narrower FWHM which is a critical criterion when choosing a filter for wavelength selection of a laser. Using racetracks or sampled gratings in Vernier configuration enables high FSR while reducing the thermal power needed for tuning. In the following chapter we will employ some of these filters to tune the wavelength fed back to a gain chip.

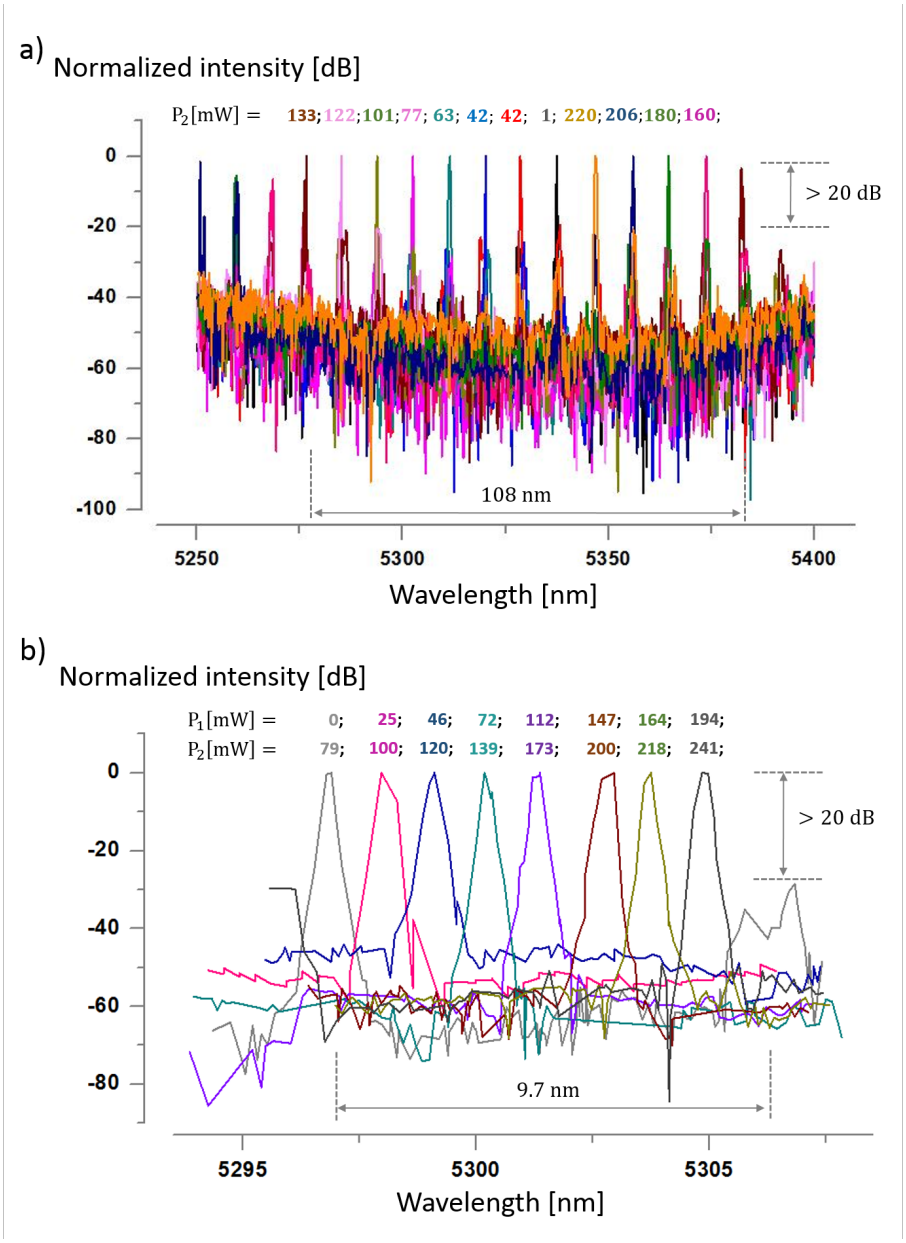

Figure 4.20: The discrete tuning of the Vernier filter. By thermally tuning resonator 2, one can tune the resonant wavelength of the filter in steps of the FSR of the resonator1 that is not tuned (a). The fine tuning of the Vernier filter by tuning both racetrack resonators together such that we have maximum transmission at the wavelength of choice. Here we show the fine tuning for a few wavelengths with a step of approximately $2FWHM$ over the FSR of the individual racetrack (b).

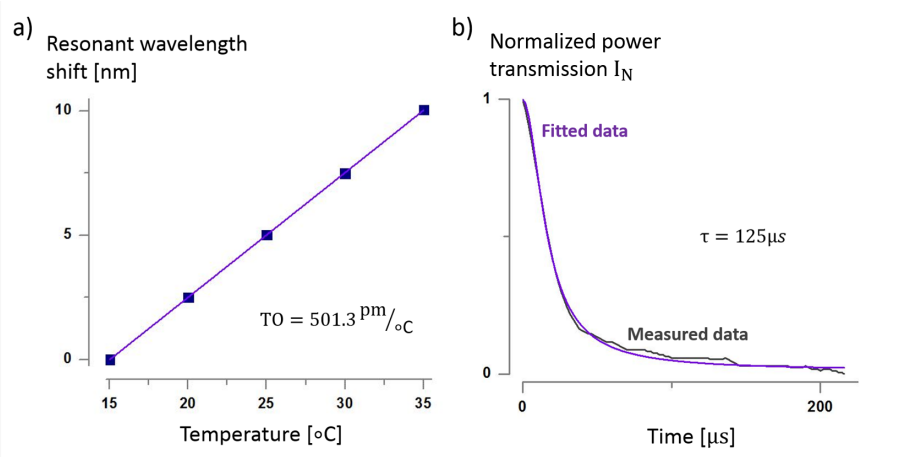

Figure 4.21: The resonant wavelength shift as a function of ambient temperature (a). Measurement data and fitting of the tuning speed of the resonator (b).

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5

External Cavity Quantum Cascade Laser Thermal Tuning

5.1 Introduction

The next step in QCL/ICL miniaturization is the implementation of the external cavity, used for wavelength selection and tuning, on a chip. Ideally, in an external cavity chip both the reflector and the phase of the feedback are tuned. For this purpose we implement heaters which enable thermal tuning. The coarse wavelength selection is done by a waveguide-based filter, while tuning the phase is used to adjust the cavity mode location (longitudinal mode position) allowing to fine tune the laser emission. Since in our setup it is not possible to resolve wavelengths with a resolution greater than 0.3 nm and the FSR of the longitudinal modes for a laser operating at 5 μm, with a 10 mm long cavity is $\sim$0.3 nm, we are only focusing on coarse wavelength tuning. In this chapter we will show different designs of the external cavity chip and describe their operation. We will start by presenting an external cavity tunable laser using a distributed Bragg reflector (DBR) on Ge-on-SOI. Later, results obtained by racetrack-resonator-based external cavity circuits are interpreted together with ideas for continuation of this work.

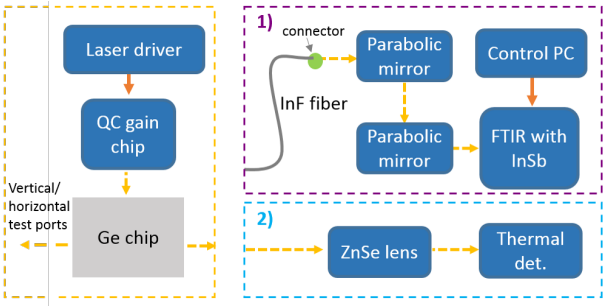

Figure 5.1: The measurement setup consists of a fixed block on the left - the light source - and two detection blocks that are interchangeable. Detection block 1) can determine the wavelength and estimate the power using an non-calibrated detector while block 2) has a calibrated thermal detector.

5.2 Measurement setup

The measurement setup is schematically shown in Fig. 5.1. Light from the QC gain chip operating in a quasi-continuous wave regime (100 kHz repetition rate, 1 µs pulse duration) is butt-coupled to the Ge-on-SOI chip. The gain chip is mounted on a cooling stage and the temperature is fixed at 20 °C. For detection we used two different schemes. The first option is to use an InF single mode fiber to take the signal of the Ge chip to an FTIR with an InSb detector, which allows to measure the emission spectrum and estimate the output power. The InSb detector is not calibrated, but the power can still be estimated by comparing the measured optical power of the Daylight QCL on both the InSb detector and a calibrated thermal detector. The second detection scheme comprises a ZnSe AR coated lens from 3-5 µm and a thermal detector.

Coarse mechanical alignment of the gain chip and the Ge chip is done with the help of a camera (Fig. 5.2), after which the alignment is optimized using the InSb detector readout.

5.2.1 Gain Chip Design

The active region of the QCL gain chip used in our work is based on a GaInAs/AlInAs lattice grown on a InP substrate [1], fabricated by Fraunhofer IAF. The maximum operation temperature, room-temperature maximum peak power per facet, and room-temperature slope efficiency of the QCL are improved by using a slightly-diagonal transition between the initial and the final electron state in the active region and the introduction of AlAs blocking barriers [2]. The gain material is confined in a ridge optical waveguide which is 10 µm wide and 3.5 mm long. Light is emitted from the cleaved front facet of the waveguide that has a broad-

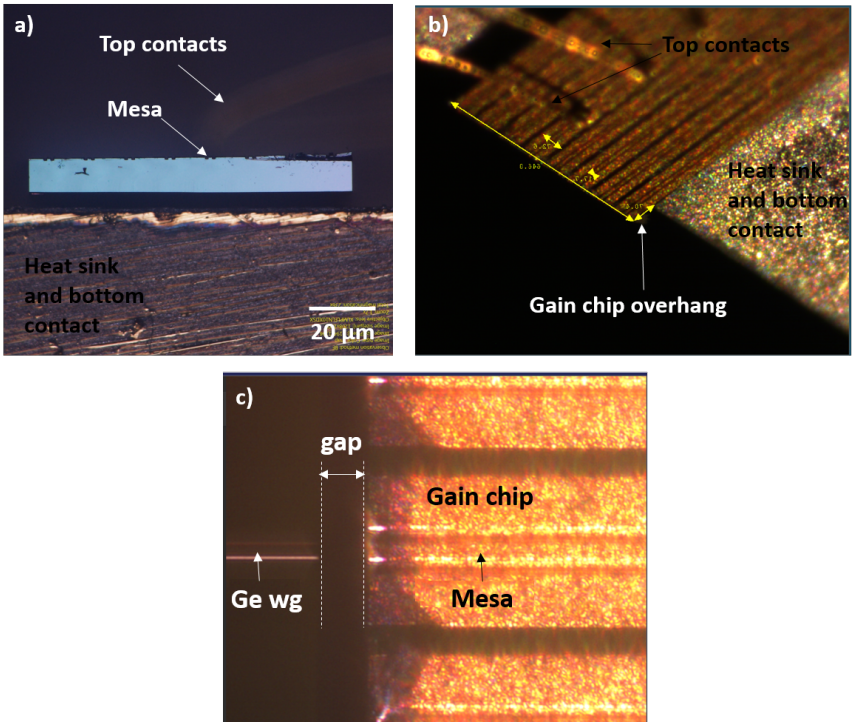

Figure 5.2: The III-V chip is mounted epi-up on a heat sink (a) with about 50 µm *overhang from the edge of the heat sink to ease the alignment with the Ge chip (b). Coarse horizontal alignment of the gain chip and the Ge chip is done visually, by positioning the III-V mesa and the Ge waveguide opposite to each other. In the vertical direction, both chips should be in the focus of the camera simultaneously (c).*

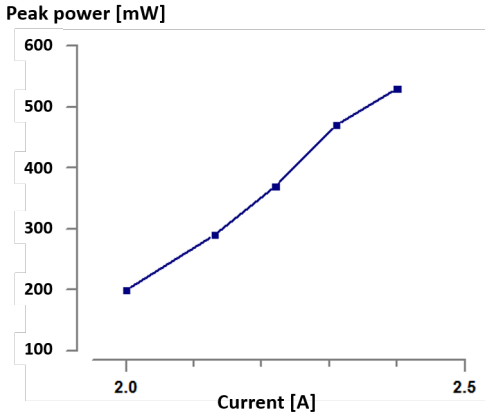

Figure 5.3: Current - peak power dependence of the gain chip lasing on parasitic reflection of its AR coated facet.

band AR coating which consists of a SiO_2/Si/SiO_2 layer stack. The laser structure is mounted on a heat sink. When operating in quasi-continuous mode at room temperature, the threshold current for lasing is 1.5 A, which is achieved by parasitic reflection of its AR coating with a reflectance estimated to be $< 3\%$. A current - peak power plot for the gain chip lasing on the AR parasitic reflectance is shown in Fig. 5.3. The laser is operating in pulsed mode at 100 kHz and 1 μs long current pulses. This laser power is detected by placing the thermal detector in front of the gain chip.

5.3 Gain chip with DBR thermal tuning

The DBR is implemented on a Ge-on-SOI waveguide platform consisting of a 2 µm thick Ge waveguide layer on a 3.2 µm Si bottom cladding on top of a 2 µm thick SiO_2 layer. In order to get a narrow reflection bandwidth and hence a single-mode emission, a shallow etched grating is needed. However, there are two limitations that come into play. On one hand, the shallower the grating, the longer the grating structure needs to be for a given reflectivity, which means that a longer grating section needs to be temperature tuned, increasing the power dissipation of the heater. On the other hand, there is the issue of the control of the etch depth. The etching rate of our dry etching recipe is around 25nm/min, including a dead-time in which no etching occurs. Therefore, shallow etched gratings are harder to control. We found that a 50 nm etched grating is a good compromise between grating strength and controlled fabrication. The waveguides were chosen 10 µm wide, in order to mimic a slab waveguide, allowing the optimization of the grating

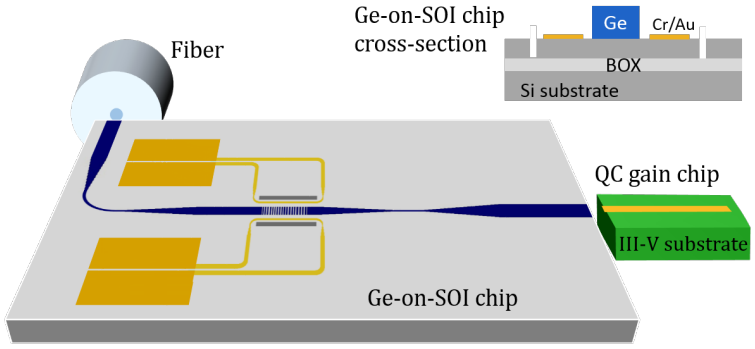

Figure 5.4: A thermally tunable external cavity QCL without any moving parts: the rotating diffraction grating used in conventional ECLs is replaced by a tunable DBR integrated on a Ge-on-SOI chip.

using 2D simulations. The grating is patterned using e-beam lithography. As the shallow etched grating does not cause topography issues, the rest of the circuit is defined by contact lithography and fully etched. Heaters are deposited on both sides of the grating to enable thermal tuning. The laser cavity is formed by the HR coated III-V gain chip facet and the Ge DBR, while the output waveguide is used to direct the light off the Ge chip. The input and output waveguides on the Ge chip are implemented under a 90°angle to avoid direct coupling from the gain chip to the fiber (Fig. 5.4). In order to avoid reflections an anti-reflection coating is deposited on both facets of the Ge chip - the facet facing the III-V gain chip and the facet facing the fiber.

SEM images of the final device are shown in Fig. 5.5, where the grating with the symmetrical heaters is shown on figure Fig. 5.5a), while the AR coated facet and a close-up on the grating pitch are displayed on Fig. 5.5b) and c).

The grating is etched 50 nm in a 10 µm wide Ge waveguide. The Ge waveguide is then tapered down to a single-mode waveguide to avoid coupling to lateral higher-order modes, followed by tapering up to a 10.5 µm waveguide for an optimal overlap with the gain chip mode. The Ge-on-SOI stack is vertically multimode which causes multiple reflection peaks as shown in Fig. 5.6a). However, these higher order modes have low overlap with the gain chip mode. The grating period is set to 660 nm with 60 % duty cycle such that TM_{00} mode of the Ge slab overlaps well with the laser gain and hence avoid multimode lasing (together with the low overlap). The laser power vs. emission wavelength was measured in an EC-configuration (Littrow type) at laser currents well above threshold. On the Fig. 5.6b) we can see that both TM_{00} and TM_{10} overlap with the gain curve. Note that this measurement is done at laser currents well above threshold, while we operate close to the threshold current where the gain bandwidth is more narrow. The grat-

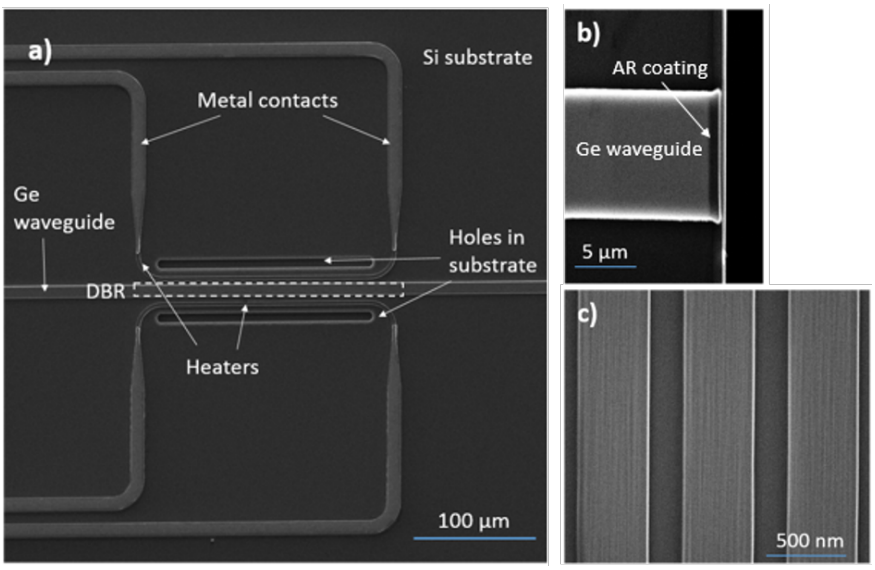

Figure 5.5: SEM images of the used Ge-on-SOI chip: the DBR structure with heaters (a), Ge facet with AR coating (b) and a zoom-in on the grating (c).

ing has 500 periods which corresponds to 27% reflection. The dependence of the grating reflection on the number of periods is plotted in Fig. 5.6c). The FWHM of the grating reflection is 5 nm.

5.3.1 Measurement Results

The thermal tuning of the external cavity laser with DBR mirror is demonstrated in Fig. 5.7. The measurement is done in a pulsed regime, at 100 kHz with 1 µs pulse duration. The bandwidth of the spectra corresponds to the bandwidth of the reflector. We assume that the lasing wavelength is tuned over the bandwidth of the DBR by the power dissipated in the gain chip within one current pulse (approximately 30W (2A x 15V)), due to the change of the gain spectrum and longitudinal mode position during the pulse. In CW operation, we would not expect this wide lasing bandwidth. However, with our setup it is not possible to resolve the wavelength tuning in time on such short time scales. We achieved 50 nm of continuous tuning starting from 5107 nm, at the expense of 1.5 W of tuning power invested in the heaters around the DBR. The laser current density was kept constant at 5.48 kA/cm^2. This corresponds to 1.92 A, which is close to the threshold current of the gain chip lasing on just its AR coating parasitic reflection. The maximum optical peak power estimated with detection scheme 1) is 22 mW, while we still have more than 1 mW of power for the first 40nm of tuning. The side-mode sup-

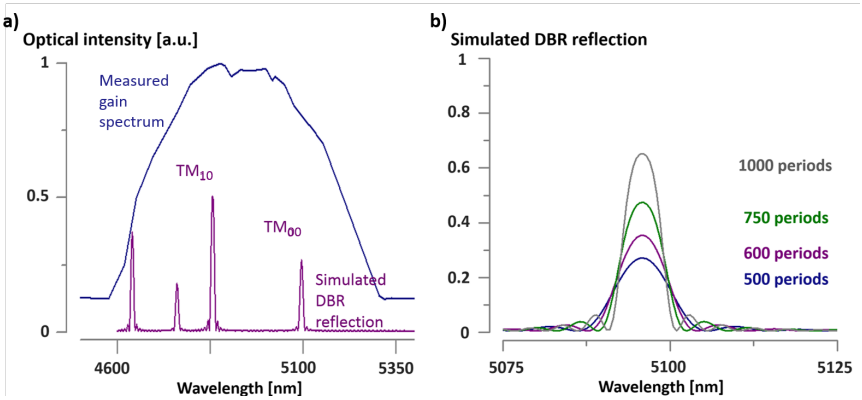

Figure 5.6: Multimode behavior of the Ge waveguide causes multiple reflection peaks from the DBR. Gain curve and its overlap with a simulation of DBR feedback spectrum (a) and DBR strength depending on the number of periods (b) is displayed.

pression is $>$ 20 dB. The strong decrease of the emitted power after 5130 nm wavelength is attributed to the misalignment that occurs during the measurement, as the Ge-on-SOI chip is heated using the micro-heater. Due to the dimensions of the waveguide cross-section and the gain chip mesa (2 μm and 3 μm in vertical direction), the measurement is highly sensitive to misalignment and it is difficult to maintain alignment over longer periods of time. This issue should be resolved when the QC gain chip is flip-chip integrated on the Ge-on-SOI chip. Because the DBR is etched in a 10 μm slab waveguide (more volume to heat up), the tuning efficiency is not optimal - 0.033 nm/mW - and could be improved. It is expected that with improving the tuning efficiency by etching the DBR in a single-mode waveguide (or using sidewall-corrugated gratings), it would be possible to achieve a wider tuning range. After the tuning measurement, we have switched to detection scheme 2) in order to verify the power detected using scheme 1) and we measured 16 mW peak power in the Ge output waveguide without tuning. The difference between the two measurements can come from misalignment or the fact that in the second scheme we are not able to position the thermal detector right after the Ge facet, whereas in the first detection approach the fiber collects the light very close to the output facet.

The current-power (I-P) plot shows a threshold current of 1.61 A. In this measurement, the laser operated without heater bias, so at 5107 nm. Below threshold, a quantum cascade laser is a very inefficient light emitter (much worse that classical diode devices). This, combined with the fact that the used thermal detector had a quite high noise floor ($\sim$ 0.1 mW), no meaningful measurements could be done below threshold.

The threshold current of an EC-QCL depends on the level of the feedback. In

this experiment, that level is determined by the strength of the DBR. A weaker DBR (weaker feedback to the laser) should increase the lasing threshold, whereas a stronger DBR should enable lasing at lower currents. Two representative power-current curves are plotted on Fig. 5.8, again for pulsed operation at 100 kHz and 1 μs pulse duration. The gain chip temperature was fixed to 20 °C. The gratings used in this measurement have 600 and 750 periods, which corresponds to respectively 35 and 48 % reflection. The measurement is started at 2 A by aligning the gain chip such that we have single-mode operation. The laser current is reduced in steps and the power and spectrum are recorded using the FTIR (measurement scheme 1). Close to threshold, the emission spectrum became multimode, an example of which is shown in the triangle inset on the figure. Nevertheless, we have fitted the threshold current relying on the points where we recorded clear single-mode operation. In the measurement with the 600 periods DBR, the threshold current is 1.725 A, while for the 750 periods DBR the threshold is at 1.64 A. As mentioned, the current-power measurement for 500 periods DBR correspond to 1.61 A. Measurements for the 1000 and 1500 periods DBR have the same threshold current, 1.7 A. Unfortunately, the expected threshold's dependence on the DBR strength is not demonstrated, most likely due to the challenge of getting a reproducible alignment. This misalignment causes excess losses in the laser cavity and increases the threshold of the laser.

5.4 Gain chip with racetrack resonator feedback

Significantly smaller FWHM values for the reflection spectrum can be obtained using racetrack resonators compared to DBRs - an important factor for realizing stable single-mode lasing. However, due to the large radius needed for lossless bends on our Ge platforms, the maximum FSR of a single resonator is limited to $\sim$ 10 nm, leading to multiple possible lasing frequencies within the gain bandwidth of the QCL. In order to increase the FSR, the racetrack resonators can be combined in a Vernier configuration, at the expense of a more complex control. In this section we will describe the experiments conducted on a single racetrack resonator external cavity without heaters.

The racetrack resonator is implemented on the Ge-on-SOI waveguide platform, by fully etching the 2 μm thick Ge waveguide layer. The etching is done using a 5 nm Ti + 90 nm Cr metal mask, patterned by one step of e-beam lithography and a lift-off process. After partial etching of the grating couplers (etch depth 0.5 μm), these structures are protected by AZ9260, while the rest of the circuit is fully etched. The circuit comprises the racetrack resonator whose input and drop port are combned by a 1x2 MMI to make a reflector, with test ports ending in grating couplers (OUT_{G1} and OUT_{G2}), and a test coupler that extracts the laser light off the Ge chip. The grating couplers are IV-th order apodized gratings. The design

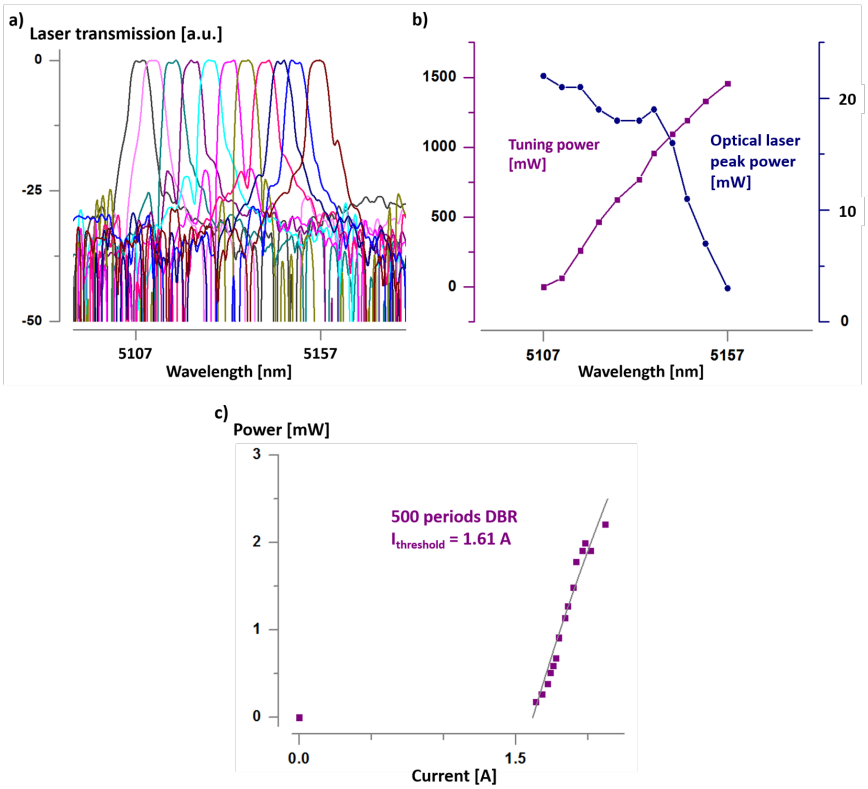

Figure 5.7: A demonstration of thermal tuning over 50 nm starting from 5107 nm of the external cavity QCL (a). The tuning power dissipated in the heaters to achieve this tuning and the optical power in the Ge waveguide (b). The current-power plot (c).

of the gratings is very similar to the IV-th order Ge-on-SOI grating described in Chapter 3, with the main differences being the layer stack underneath the grating. For fabrication simplicity, the grating coupler is not underetched, which limits the maximum coupling efficiency to 40%. The parameters of the Section b are: $p =$ 2.86 µm, the number of periods is 30, the etch depth $h = 0.5$ µm, with apodization parameters $w_{e,start}$ = 1.4 µm and $w_{e,end}$ = 0.5 µm. Section a has n_a = 2, a period of p_0 = 1.8 µm and a duty cycle of dc_0 = 0.5. The 1x2 MMI is 15 µm wide, with 1 µm space between output tapers and has a length of 105 µm. The gratings are used for monitoring of the wavelength, as well as to prevent parasitic reflections since the grating couples $< 4\%$ of light on entire wavelength range of interest, in the opposite direction in the waveguide. The part of the light that still remains in the waveguides after going through the grating couplers is radiated in the tapers. Besides the ports ending with the grating couplers, the output ports of the test

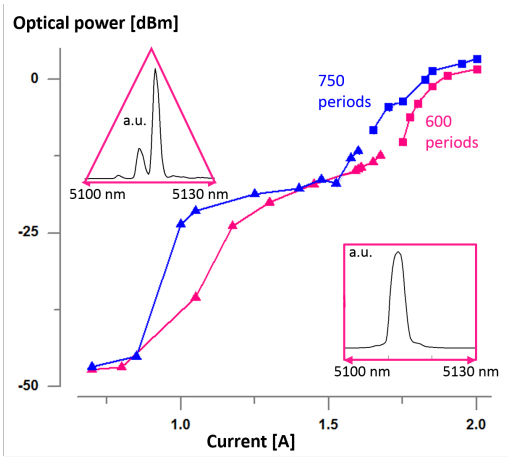

Figure 5.8: The power-current curves for a 600 and 750 period DBR laser are plotted in two parts: for the points plotted with a square symbol, the measured spectrum shows single-mode operation, while for the points plotted with a triangle symbol multimode lasing is observed, which causes the second knee in the curves before power drops to the noise floor around -48 dBm. An example of these two modes of operation measured for the 600 periods grating are shown in the square and triangle inset.

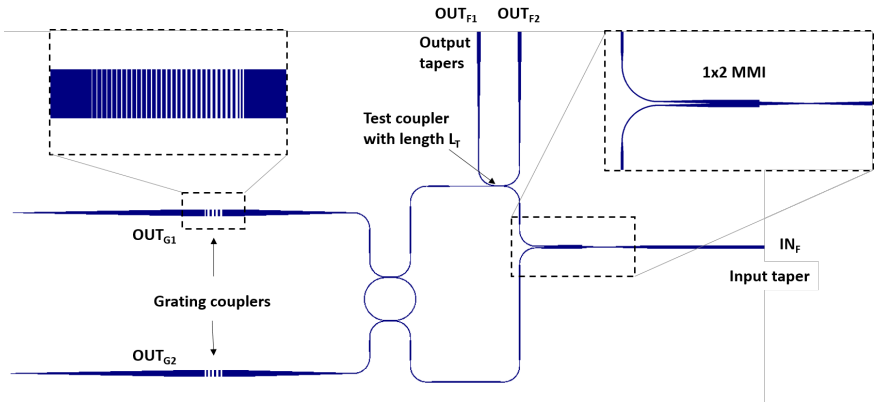

Figure 5.9: Racetrack resonator- based feedback circuit design

coupler are ending in facets (OUT$_{F1}$ and OUT$_{F2}$). The test coupler output tapers are 15 µm wide, while the IN$_F$ input taper is 13.5 µm wide. The advantage of the facets over the grating couplers is unlimited bandwidth. In this experiment, we kept constant racetrack radius of 100 µm with a 40 µm long and 0.5 µm wide coupler gap. To learn about the lower limit of the feedback strength needed for the laser to lase on the external cavity modes, rather than on its parasitic reflection,

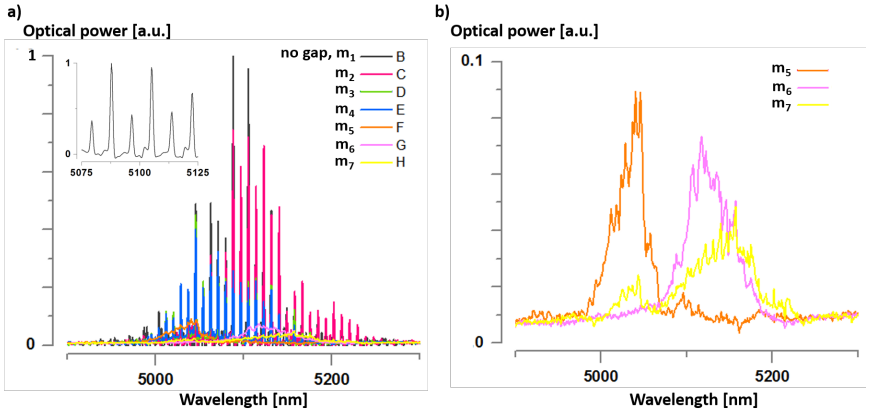

Figure 5.10: Measurements for different gaps between the Ge-chip and III-V gain chip are plotted, starting with the measurement where the two facets are touching (a). magnification to the last three measurements, showing FP lasing on the gain chip facets (b).

we fabricated devices with different length of the test coupler L_T. Similar to the design with the DBR, the laser cavity is formed by a III-V gain chip and a Ge chip, while the test coupler is envisaged to direct the light off the Ge chip. The input taper facing the gain chip and the tapers of the test coupler on the Ge chip are implemented under a 90° angle to avoid direct coupling between the gain chip and the fiber (Fig. 5.9). An anti-reflection coating is deposited on the facet of the Ge chip facing the III-V gain chip.

During the measurement the gain chip was cooled to 20 °C. The circuit design allows us to test the Q-factor of the racetrack resonator, Q = 5000. The low Q-factor is explained by imperfect fabrication which is explained in more detail in Chapter 2. After covering the gratings with resist to protect them from further etching, the resist is not completely removed around the racetrack waveguide and in the coupler gaps of the racetrack before continuing the dry etching which causes additional sidewall roughness and higher losses in the racetrack (Fig. 2.18). IN_F - OUT_{G1} transmission for the device with L_T = 40 µm was measured for different gaps between the gain chip and the Ge chip IN_F facet. The bias current was kept constant at 2 A. By changing the gap between the two facets, the feedback to the laser changes due to the change in coupling efficiency between the two chips. In Fig. 5.10a), measurements for seven different gaps are plotted, starting with the measurement where the two facets are touching. The first five measurements show that the laser is lasing on the resonances of the racetrack circuit, as the FSR and FWHM corresponds to that of the racetrack resonators (inset of Fig. 5.10a). Due to limitations of the camera used in the setup, it is not possible to extract the exact distance between the chips for each measurement, but at the point when the

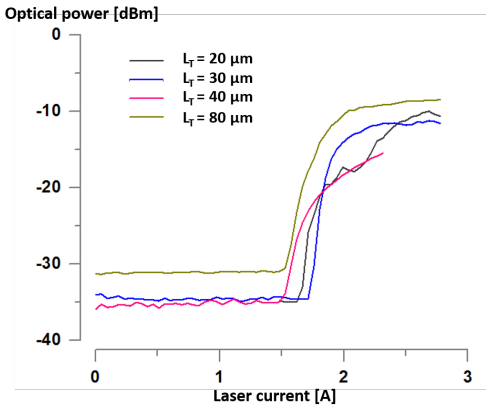

Figure 5.11: I-P measurements for different L_T.

laser stops lasing on the resonances of the racetrack circuit (Fig. 5.10b) the gap is comparable to the IN_F taper width (10-15 µm).

Measurements of the optical power versus the laser current (I-P) using ports OUT_{F1} are done for different L_T (Fig. 5.11). Similar to the experiments with the DBR external cavity laser, it is difficult to make conclusions about the dependence of the laser threshold current on the external cavity feedback reflectance / outcoupling, due to misalignment during the measurements and the fact that every measured curve is obtained from different devices by realigning to its facet.

5.5 Future work : Gain chip with Vernier racetracks filter feedback

Following the experiments with a single racetrack resonator external cavity feedback, in this subsection we will describe approaches to continue this work.

In order to have single-mode lasing, it is important to design an external cavity circuit with an appropriate FSR and FWHM. Previously demonstrated racetrack resonators can provide a sufficiently narrow FWHM to suppress other nearby longitudinal modes, while a Vernier racetrack filter can achieve the FSR needed to have only one dominant reflection peak in the QCL's gain bandwidth. Therefore, all of our proposed designs contain the Vernier filter. The most simple circuit is an expansion of the single racetrack feedback circuit from the previous subsection (Fig. 5.12a), where the gain chip couples to the circuit through the input taper and the useful part of the light is taken off the chip through the two output tapers. The downside of this design is the fact that the structure has two output ports. Also, the coupler length is fixed which means that for each gain chip we have to redesign

the coupler parameters according to the needed external cavity feedback strength. In case of a bad cleave of the input taper facet, it is not possible to overcome the losses due to the gain chip - Ge chip coupling by increasing the strength of the feedback reflectance. A more advanced circuit design comprises a balanced MZI that determines the amount of light coupled out (Fig. 5.12b). Here, again we have two output waveguides due to the symmetry of the MZI. Finally, the design on Fig. 5.12c) combines the two output waveguides into one output taper through a 2x1 MMI. A heater is implemented to tune the phase in one of the waveguides and achieve constructive interference in the 2x1 MMI.

Using the same fabrication flow as for Vernier racetrack resonators (a combination of e-beam and contact lithography to define two etching depths), we defined the circuit from Fig. 5.12b) with heaters on Ge-on-SOI platforms. The chip's substrate was subsequently ground down to 350 μm and cleaved. Both input and output facets were AR coated. The first results are shown in Fig. 5.13 for a laser current of 2.4 A. Although there are hints of the start of single-mode lasing for our circuit design, a more convincing demonstration was not possible at this point. Due to the fabrication challenges caused by e-beam definition of a large-footprint circuit additional losses are introduced caused by fabrication imperfections such as stitching errors or voids, reducing the feedback. However, we expect that using DUV lithography for fabrication would enable a successful experiment.

5.6 Conclusion

Although there is room for improvement, these experiments represent the first proof-of-concept of a QCL based on a tunable external cavity on a Si waveguide circuit, thereby allowing wide tuning without any mechanically moving parts. Thermal tuning over 50 nm starting from a wavelength of 5107 nm using a DBR external cavity is demonstrated. DBR external cavities are thermally less efficient due to their length and they have a higher FWHM ($\sim$5 nm). Implementing the DBR in a single-mode waveguide or as a side-corrugated DBR would improve thermal efficiency. Nevertheless, a Vernier racetrack filter is a better solution due to its small FWHM ($\sim$0.2 nm) and high FSR (typical values range from 100 - 425 nm). The first attempts of building a Vernier racetracks external cavity laser show promising results in spite of fabrication challenges. It is expected that DUV fabrication of such a circuit would enable single-mode tuning over the entire bandwidth of the gain chip.

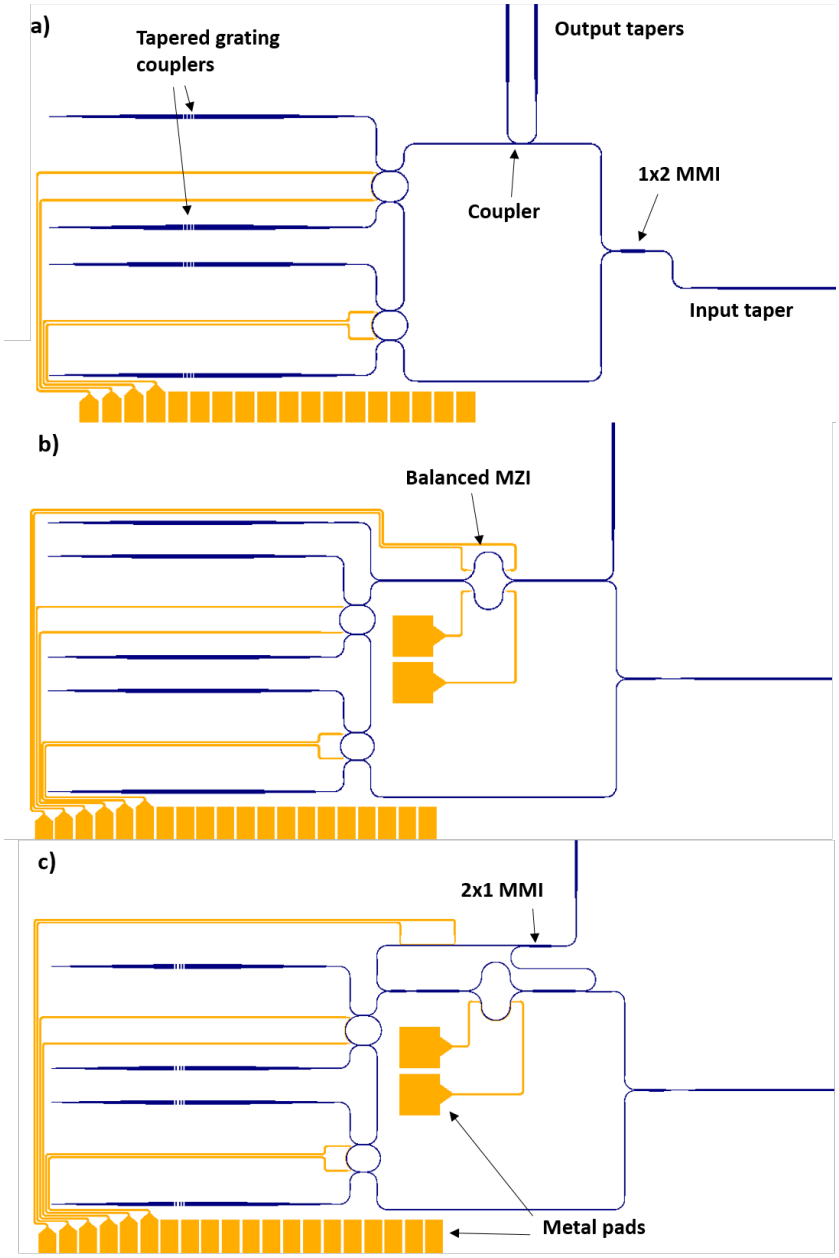

Figure 5.12: High FSR, low FWHM filters in a loop configuration. Vernier filter consisting of two racetracks with a coupler taking the light off the chip (a), Vernier filter in combination with a balanced MZI which sets the portion of light that is coupled out (b) and a similar circuit with combined output waveguides (c).

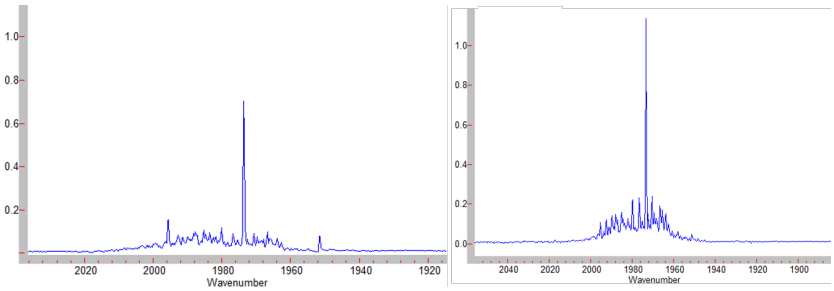

Figure 5.13: The first results of the gain chip coupled to the circut from Fig. 5.12b).

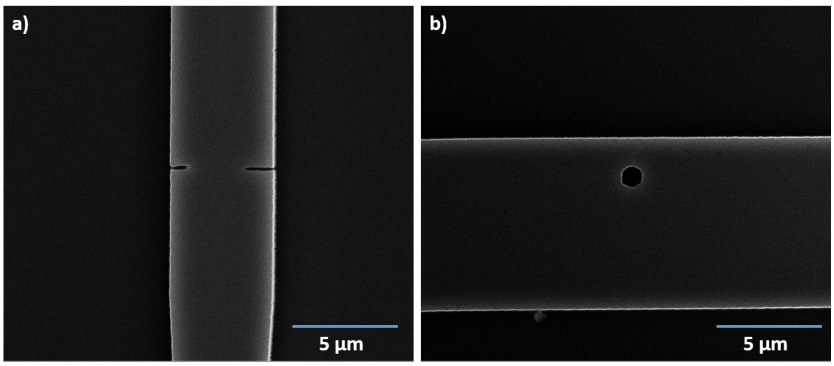

Figure 5.14: Some of the challenges in e-beam fabrication of a large-footprint circuit: stitching errors occur at the boundaries of two e-beam write fields (a) and higher probability of having a particle that lifts off the metal mask and leaves voids in waveguides after dry etching (b).

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6 Conclusion

6.1 Main results and conclusions

Widely tunable QCLs operating with Watt-level optical power, but bulky and confined to laboratory environment as well as the potential of mid-infrared sensing were the driving force for work on miniaturization and integration of QCLs with CMOS compatible waveguide platforms. Here Ge emerged as an excellent candidate for the guiding medium. Over the years, different components and circuits were demonstrated on the Ge platforms, some of which are presented in this thesis.

FWHM of a gas absorption line around 5 μm wavelength can be as small as 0.3 nm, whereas absorption characteristic of liquids usually have wider features. At the same time, it is important to keep in mind the gain characteristic of the III-V chip in order to achieve single mode lasing. For these reasons some of the components and circuits that we considered are better suited for gas sensing (racetrack resonators and Vernier racetracks), while others are a better match for the needs of liquid sensing (MZI, DFB, AWG...). A summary of the devices characteristics is displayed in Table 6.1. For the needs of this work, simulation models, fabrication schemes and measurement setups were developed.

In the first part of our work we focused on different types of interfaces for the Ge chips. An efficient AR coating has been demonstrated which prevents parasitic reflections in facet-terminated designs. A new optimized design for Ge-on-Si and Ge-on-SOI grating couplers which allowed for smaller circuit footprint and enabled wafer level testing, was proposed and simulated. The Ge-on-SOI coupler

	FSR [nm]	FWHM [nm]
Gas absorption line	-	0.3
Liquid absorption feature	-	1 - 100
Racetrack resonator	10	0.3
Vernier racetrack resonators filter	100 - 425	0.2
MZI	25	6
3 cascaded MZIs	100	5
DBR	-	5
AWG	145	5

Table 6.1: Typical values of device characteristics around 5 μm *wavelength*

benefits from locally under-etching the BOX layer and therefore significantly improving the directionality of the coupler. A reasonable match with the measured device with 30% maximum efficiency and a 100 nm 3 dB bandwidth is obtained. The best characterized locally free-standing grating coupler for the Ge-on-SOI platform has a maximum efficiency of 45% and an estimated 3 dB bandwidth of 220 nm, while for the Ge-on-Si grating coupler the fabricated device has a 40% efficiency and a 3dB bandwidth of about 200 nm.

Next, we have proven that thermally tunable wide FSR optical filters are possible in the Ge waveguide platforms. A number of designs was tested, all operating in the 5 μm wavelength range, of which the most significant was a thermally tunable racetrack resonator filter in Vernier configuration on Ge-on-SOI platform, with a 110 nm FSR and a side-peak suppression $>$20 dB. Individual racetrack resonators used in the circuit had a Q-factor of ˜20000 and a FSR of ˜9 nm. Furthermore, our simulations showed that using the racetrack resonators with a Q-factor of 20000 we can even achieve a FSR of the Vernier filter of up to 425 nm and still maintain a 4 dB side-peak suppression. In addition, the temperature shift of the operating wavelength of the filter was assessed (0.5 nm/K). The response time of an individual thermally tunable racetrack resonator was measured to be 125 μs, allowing for KHz rate wavelength tuning.

Finally, a proof-of-principle EC-QCL based on a QC gain chip butt coupled to a Ge-on-SOI chip was demonstrated with thermal tuning over more than 50 nm. The Ge-on-SOI chip comprised of a shallow etched DBR. To improve the tuning range, the DBR filter can also be replaced with e.g. Vernier filters with wide FSR, as mentioned in the previous paragraph.

The combination of QC gain chips and silicon-based waveguide circuits for wavelength selective feedback (as well as implementing other functionalities on the chip) will enable the miniaturization of mid-infrared laser systems. While the

current demonstration relies on two separate chips, our work paved the way for the flip-chip integration of the quantum cascade gain chip on the silicon photonic integrated circuits.

6.2 Continuation of the project

As part of our work, several circuits based on Vernier filters have been proposed as good candidates for the wavelength selection and tuning circuits (Fig. 5.12). Fabrication and characterization of these circuits took place, and although we encountered obstacles in terms of e-beam limitations, good initial results were obtained (Fig. 5.13). Using DUV insted of the e-beam fabrication flow, would improve performance of the circuit. Following a successful single-mode QCL operation, development of flip-chip process should take place. Integration of the gain chip with the tuning Ge circuit would produce a miniaturized robust mid-infrared laser source. As the Ge platforms have low losses for the mid-infrared light, there is a possibility to extend the Ge circuit and implement the sensing functionality on the same chip. If the sensing is done on the Ge chip itself, a less powerful gain chip is needed, as the light is not lost in coupling from the Ge chip to the sensing module, e.g. a gass cell.

All the demonstrations we performed so far are done in pulsed regime. This is due to limitation of the heat sinking. A QCL produces enormous amounts of heat when operating in CW regime and over-heating prevents the laser from functioning properly and even leads to breakage. Another step forward would be to work on the heating challenge and operate the laser in the CW regime. This type of device would in return demand less sensitive detector without complex cooling scheme and the entire sensor system in then applicable in hand-held industrial environment.