

**III-V-on-Si SOAs and DFB/DBR Lasers Realised Using Micro-Transfer
Printing**

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The meticulousness required to write this section makes it more challenging than the rest of the thesis and I hope that I will not forget to mention anyone. In retrospect, the first time I studied the field of optics and photonics was in my undergraduate in Pakistan. I was fascinated by photonics from the start. It made me realize how powerful nature and its processes can be. Light, as it may seem ordinary and mundane to a layman, is one of the most powerful tools of nature. It never fails to amaze you, the deeper you study it, the more you want to learn about it. By the time, I finished my undergraduate, I had already made up my mind to pursue a Ph.D. degree in the field of photonics. Now that I think in retrospect, I am thankful to my teachers who played an important role in developing interest in the field of photonics and told us about various universities and institutes that offer education in this field. I liked the idea of studying abroad, traveling, and living in a different country. I remember applying to many master's degree programs and luckily, I got admission in a few of them with scholarships. I am grateful to my teachers who taught high-quality courses in my master's degree which helped me a lot during the Ph.D. Moreover, I am also grateful to my master's degree supervisor Prof. Rasras for introducing me to the field of silicon photonics.

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List of Acronyms

A

AWG Arbitrary Waveform Generator

B

BOX Buried Oxide

BW Bandwidth

C

CW Continuous Wave

CMOS Complementary metal oxide semiconductor

D

DBR Distributed Bragg Reflector

DFB Distributed Feedback

DC Direct Current

DVS-BCB Divinylsiloxane-bis-Benzocyclobutene

E

EM	Electromagnetism
EBL	Electron beam lithography
EME	Eigenmode Expansion

F

FOM	Figure of merit
FEM	Finite element method
FWHM	Full width at half maximum
FDTD	Finite-difference time-domain
FF	Fill Factor
FSR	Free Spectral Range
FIB	Focused Ion Beam
FP	Fabry-Perot

H

HCl	Hydrochloric Acid
H3PO4	Phosphoric acid

I

ICP	Inductively Coupled Plasma
-----	----------------------------

L

LIDAR	Light Detection And Ranging
LI	Light-Current

M

MZM Mach Zehnder Modulator
MQW Multiple Quantum Wells

N

NRZ Non-Return-to-Zero

O

OSA Optical Spectrum Analyzer

P

PIC Photonic integrated circuit
PC Polarization Controller
PD Photodiode
PDMS Polydimethylsiloxane
PECVD Plasma-Enhanced Chemical Vapor Deposition

R

RIE Reactive Ion Etching
RF Radio Frequency

S

Si	Silicon
SiPh	Silicon Photonic
SEM	Scanning Electron Microscopy
SOI	Silicon-on-Insulator
SOA	Semiconductor Optical Amplifier
SMSR	Side-Mode Suppression Ratio

T

TE	Transverse electric
TM	Transverse magnetic
TL	Tunable Laser
TP	Transfer Printing

W

WDM	Wavelength Division Multiplexing
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Z

ZB	Zettabytes
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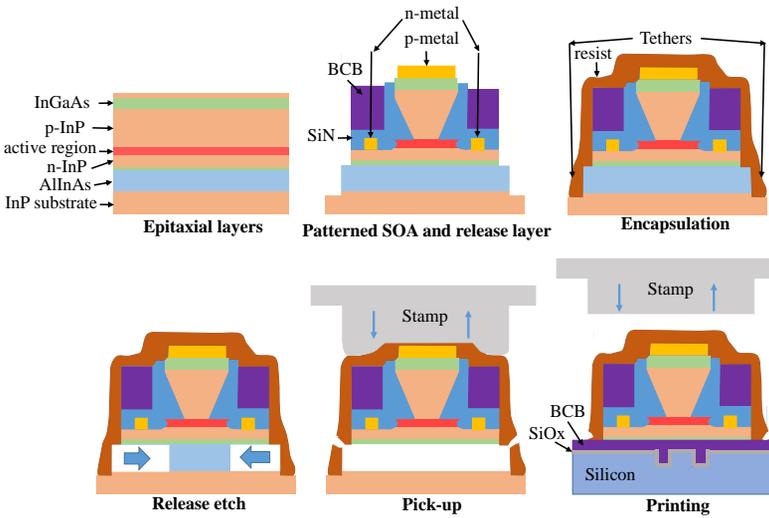
Nederlandse samenvatting

–Summary in Dutch–

In dit werk ontwikkelen we micro-transferprinttechnologie om III-V halfgeleider optische versterkers op siliciumgolfgeleidercircuits te integreren en deze te gebruiken om DFB-lasers en DBR-lasers te demonstreren.

Fotonica wordt beschouwd als één van de faciliterende technologieën van dit decennium. Fotonische geïntegreerde schakelingen worden in het bijzonder gebruikt om licht op micrometerschaal te genereren, te manipuleren en te detecteren. Eén van de vele toepassingen zijn optische interconnecties, die cruciaal zijn voor de toekomstige groei van de datacom-industrie. Optische verbindingen bestaan uit zenders en ontvangers voor snelle gegevensoverdracht in een datacenter, maar ook voor communicatie over langere afstanden. Andere snelgroeïende marktsegmenten zijn onder meer LiDAR voor zelfrijdende auto's. In sommige implementaties maakt LiDAR gebruik van fotonische geïntegreerde schakelingen om miniatuurlichtbronnen en detectoren met laag vermogenverbruik te produceren tegen lage kost. Silicium fotonica is een veelbelovend integratieplatform voor goedkope en grootschalige fabricatie van de fotonische geïntegreerde schakeling. Inherent is het echter een bijna onmogelijke uitdaging om een efficiënte lichtbron in Si te produceren. Daarom worden andere materialen zoals III-V-halfgeleiders op het SOI-substraat geïntegreerd.

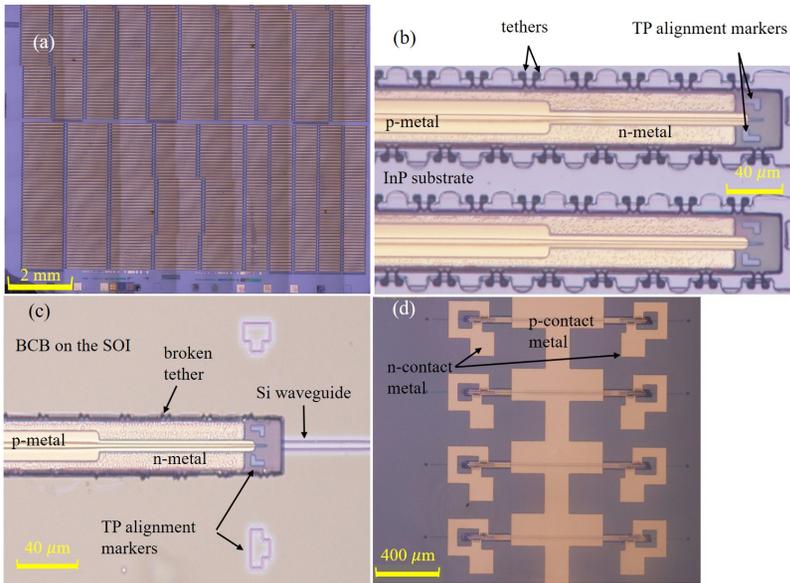
Verschillende heterogene integratietechnieken zijn in de loop der jaren ontwikkeld, waaronder directe en adhesieve hechting, monolithische integratie, hergroei op een hechtings-sjabloon en flip-chip-integratie. Sommige van deze technieken zijn technologisch meer volwassen dan de andere en allen hebben ze zowel voor- als nadelen. Micro-transferprinten is een nieuwe techniek voor de integratie van opto-elektronische componenten. Het biedt de voordelen van zowel flip-chip als adhesieve hechting, hetgeen betekent dat geteste componenten kunnen worden opgepikt met een stempel en in grote volumes kunnen worden geplaatst. Het principe



Figuur 1: Schematische voorstelling van het micro-transfer-printproces van geprefabriceerde SOA-coupons.

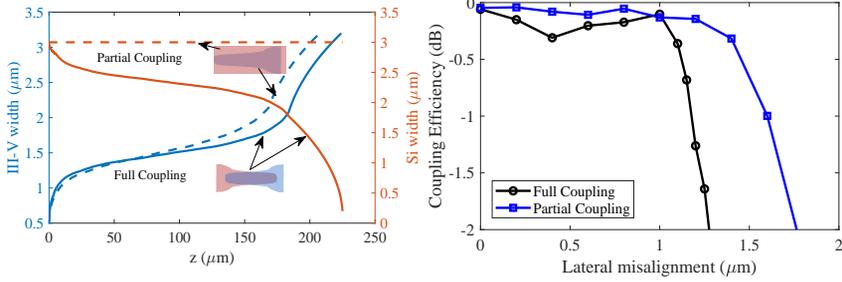
maakt gebruik van de visco-elastische eigenschap van de PDMS-stempels. De stempels kunnen, afhankelijk van hun kinetische energie, zich gedragen als een elastisch of visceus materiaal. Dit betekent dat wanneer een stempel na laminatie met de componenten met hoge snelheid wordt weggehaald, de componenten worden opgepikt door de PDMS-stempel. Aan de andere kant, wanneer de stempel met de componenten gelamineerd wordt met een ander substraat en de stempel traag verwijderd wordt, worden de componenten losgelaten door de stempel.

Figuur 1 toont het proces van micro-transferprinten van SOA-coupons (SOA: Semiconductor Optical Amplifier: Halfgeleider optische versterker). De III-V SOA is gedefinieerd op de InP-wafer. Dit proces omvat de vorming van SOA-mesa, het etsen van de actieve laag, contactmetaalafzetting, planarisatie met behulp van DVS-BCB en het terugetsen van het DVS-BCB en SiN-planarisatie om de coupons te realiseren. De offeringslaag wordt vervolgens gestructureerd en coupons worden ingekapseld met een fotoresist. De offeringslaag die in ons geval uit AlInAs bestaat, wordt ondergeëtsd. Op dit punt worden de coupons zwak vastgehouden door fotoreziststructuren die aan het substraat zijn verankerd. De volgende stap is om het SOA-sample en het SOI-sample in de micro-transferprintto:ol te monteren. Deze tool maakt gebruik van beeldverwerking om de coupons uit te lijnen met het SOI substraat waarop geprint wordt. Uitlijningsmarkerin-



Figuur 2: Microscopiebeeld van a) verwerkte SOA-coupons op het InP-substraat, b) twee SOA-coupons van (a) waarop wordt ingezoomd, c) geprinte SOA-coupon op een Si-golfgeleider, en d) III-V-on-Si SOA's met metaalcontacten.

gen hebben een patroon op zowel de III-V-coupons als op het SOI-substraat om elke coupon uit te lijnen met betrekking tot het Si-golfgeleidercircuit. Wanneer de installatie en uitlijning is voltooid, gaat de stempel naar de opgeslagen x-y-coördinaat op de bron, lamineert een coupon en pikt deze op. Vervolgens beweegt de stempel naar de opgeslagen x-y-coördinaat op het doel, delamineert de coupon en plaatst deze op de gewenste locatie. Nadat alle coupons zijn getransfereerd, wordt de inkapseling verwijderd en wordt de DVS-BCB lijmlaag volledig uitgehard. De laatste stap is het elektrisch contacteren van de component. Figuur 1 toont microscopiebeelden van de III-V-on-Si SOA's bij verschillende processtappen. De uitlijning van de III-V SOA met de Si-golfgeleider is een belangrijke parameter. De beste micro-transferprinttools kunnen een uitlijningstolerantie van $(3\sigma) \pm 1,5 \mu\text{m}$ bieden. Dit betekent dat III-V/Si adiabatische koppeling een goede koppelingsefficiëntie moet hebben binnen de genoemde uitlijningstolerantie. Dit is met name belangrijk voor de ontwikkeling van SOA's met hoge versterking. Daarom hebben we twee adiabatische koppelingsstructuren ontworpen met een uitlijningstolerantie van $1,0 \mu\text{m}$ en $1,5 \mu\text{m}$ als het slechtste geval voor volledige en gedeeltelijke koppeling tussen Si



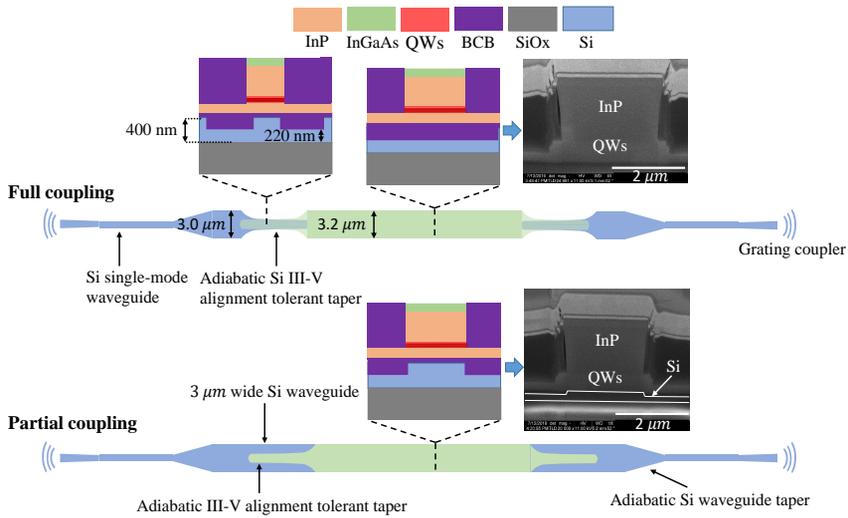
Figuur 3: (links) De III-V en Si adiabatische koppelstructuur in de lengterichting. De blauwe lijn en de linker verticale as stellen de III-V adiabatische conische vorm voor de gedeeltelijke en volledige koppelingsontwerpen. De rode lijn en de rechter verticale as representeren de adiabatische conische vorm van Si en de breedte van de Si golfgeleider in het geval van respectievelijk volledige koppeling en gedeeltelijke koppeling; (rechts) De gesimuleerde koppelingsefficiëntie van de adiabatische structuren voor de ontwerpen voor gedeeltelijke en volledige koppeling versus de laterale uitlijning.

en III-V.

Figuur 3 illustreert de vorm van de twee ontworpen adiabatische koppelingsstructuren en de efficiëntie van de koppeling tegen de laterale uitlijningsfout. De Si adiabatische structuur tapert van $0,2 \mu\text{m}$ naar $3,2 \mu\text{m}$ en het III-V tapert van $3,0 \mu\text{m}$ naar $0,5 \mu\text{m}$. Bovendien is de berekende koppelingsefficiëntie voor zowel de structuren voor gedeeltelijke koppeling als voor de structuren voor volledige koppeling groter dan $-0,3 \text{ dB}$ voor een verkeerde uitlijning van $\pm 1,0 \mu\text{m}$.

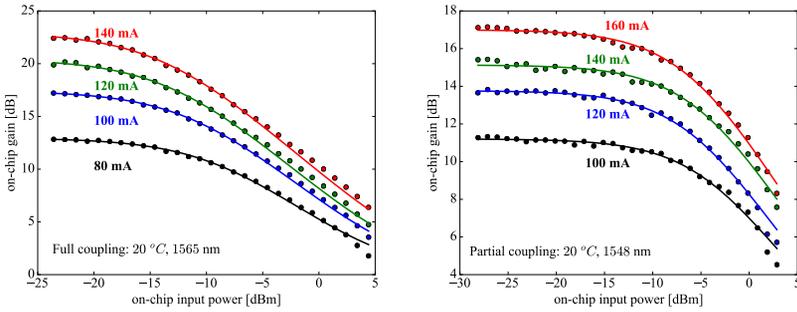
De epitaxiale SOA-stack heeft een hooggedoteerde p-InGaAs-contactlaag met een dikte van 200 nm , een p-InP-bekleding met een dikte van $1,5 \mu\text{m}$ di, een InGaAsP-etsstoplaag van 25 nm , een paar AlGaInAs lagen van 40 nm , overgangslagen die InP van SCH-lagen scheiden, een paar 75 nm AlGaInAs SCH-lagen, een actief gebied met 6 AlGaInAs QW's ingeklemd tussen AlGaInAs-barrièrelagen, een 200 nm n-InP-contactlaag met 60 nm intrinsieke InP-laag eronder en een $50 \text{ nm}/500 \text{ nm}$ InGaAs/AlInAs-opofferingslaag gegroeid op het InP-substraat.

We hebben twee III-V-op-Si SOA-ontwerpen ontwikkeld die een verschillende Si-golfgeleiderbreedte hebben in het versterkingsgedeelte van de SOA. Dit maakt het mogelijk om de opsluiting van de optische modes in de kwantumputten te variëren en zo de klein-sigitaalversterking en het uitgangsverzadigingsvermogen af te stemmen. De Si-golfgeleiderlaag is 400 nm dik en heeft een etsdiepte van 180 nm . De begraven oxidelaag



Figuur 4: Schema's en FIB-doorsnedes die het ontwerp van de volledige koppeling en gedeeltelijke koppeling voor III-V-op-Si SOA's illustreren.

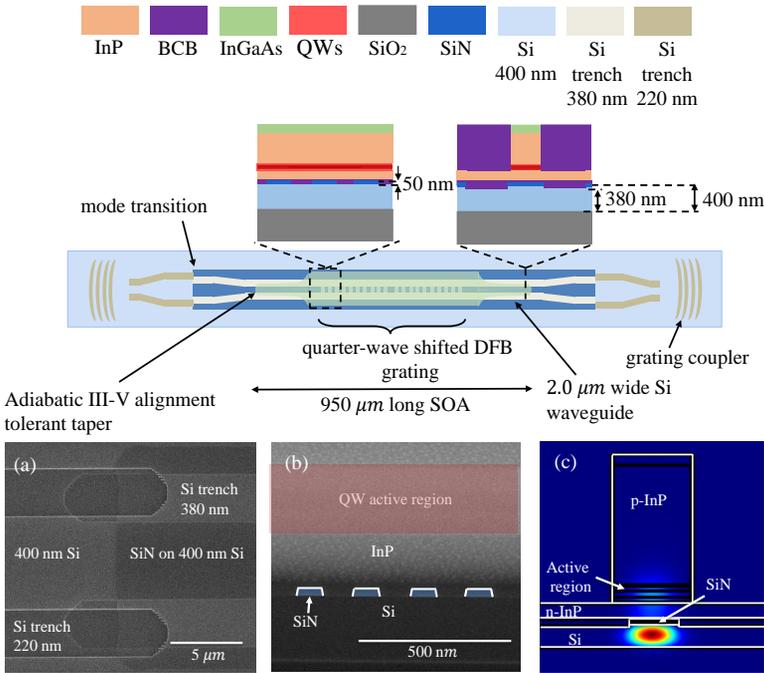
(BOX) is $2 \mu\text{m}$ dik onder de Si-golfgeleiderlaag. Beide SOA-ontwerpen, volledige koppeling (hogere optische opsluiting in de QW's) en gedeeltelijke koppeling (lagere optische opsluiting in de QW's), worden geïllustreerd in figuur 4. De III-V-op-Si SOA wordt voor de metingen op een houder geplaatst waarvan de temperatuur constant gehouden wordt op 20°C . De versterker wordt optisch uitgelezen met single-mode vezels. Roosterkoppelaars worden gebruikt om het licht te koppelen naar de optische vezels. De roosterkoppelaars hebben een golflengte-afhankelijke transmissie. Daarom is het nodig om roosterkoppelaars te karakteriseren als een functie van de golflengte om de versterking op de chip nauwkeurig te kunnen meten. Om dit te doen, worden referentie Si-golfgeleiders op dezelfde chip als de versterkers gerealiseerd en ondergaan ze dezelfde processtappen als de roosterkoppelaars die worden gebruikt om de SOA's te analyseren. De golflengte-afhankelijke transmissie van de roosterkoppelaars wordt gemeten met behulp van een afstembare laser (Santec TSL-510) en een optische spectrumanalysator (OSA, Advantest Q8381A). De hoek van de vezelhouders is geoptimaliseerd om de maximale transmissiegolflengte van de roosterkoppelaars uit te lijnen met de versterkingspiek van de twee besproken SOA's. Aangezien de III-V SOA's die op beide SOI-ontwerpen zijn geprint nominaal hetzelfde zijn, is de serieweerstand ook nominaal hetzelfde, $10,0 \Omega$ bij een stroom van 80 mA stroom of een stroomdichtheid van $1,8 \text{ kA/cm}^2$.



Figuur 5: Variatie van de versterking op de chip met het ingangsvermogen op de chip voor verschillende instelstromen, (links) voor het ontwerp met volledige koppeling bij 1565 nm, (rechts) voor het ontwerp met de gedeeltelijke koppeling bij 1548 nm.

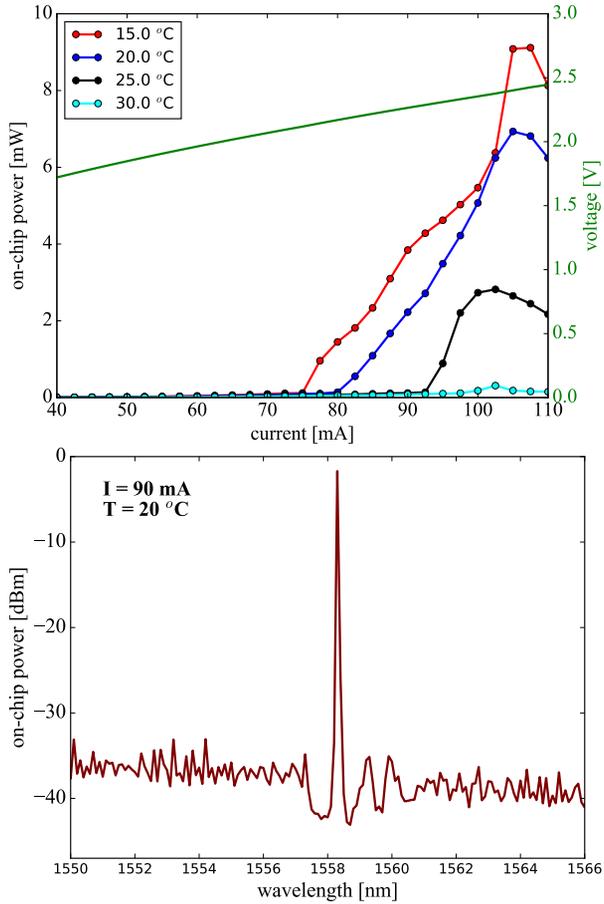
Figuur 5 illustreert de gemeten versterking op chip van de SOA's voor verschillende stromen. Het maximale uitgangsvermogen is 10,8 dBm voor een golflengte van 1565 nm (bij 140 mA) en 11,3 dBm voor een golflengte van 1548 nm (bij 160 mA) voor respectievelijk volledige koppeling en gedeeltelijke koppeling. P_{sat} is 12,8 mW en 9,0 mW voor respectievelijk de gedeeltelijke en volledige koppeling. De SOA met gedeeltelijke koppeling (en lagere overlap met de actieve laag) heeft een maximum P_{sat} van 15 mW bij 160 mA instelstroom (417 mW vermogensdissipatie) en een kleinsignaalversterking van 17 dB. Ter vergelijking: de SOA met volledige koppeling (en hogere overlap met de actieve laag) heeft een maximum P_{sat} van 9,2 mW bij 140 mA instelstroom (336 mW vermogensdissipatie) en een kleinsignaalversterking van 23 dB. De SOA met een hogere overlap leidt dus tot meer versterking, maar heeft een lager verzadigingsvermogen en vice versa. De 3dB-versterkingsbandbreedte van de SOA neemt toe met de biasstroom en is 30 nm bij 120 mA (2,71 kA/cm²). Een vergelijkbare versterkingsbandbreedte wordt verkregen voor de structuur met gedeeltelijke koppeling. Voor 100 mA stroom en een golflengte van 1565 nm is het ruisgetal $F_{\text{sig-ASE}} \approx 8,6$ dB voor een ingangsvermogen op de chip van -24 dBm en is $F_{\text{sig-ASE}} \approx 9,54$ dB bij 0 dBm ingangsvermogen. Evenzo heeft bij 1548 nm de SOA met gedeeltelijke koppeling een ruisgetal $F_{\text{sig-ASE}} \approx 7,0$ dB bij -24 dBm on-chip ingangsvermogen en $F_{\text{sig-ASE}} \approx 8,6$ dB bij 0 dBm ingangsvermogen op de chip. De SOA's laten prestaties zien die vergelijkbaar zijn met de componenten die zijn gemaakt met andere heterogene integratietechnologieën.

In de volgende stap hebben we III-V-op-silicium DFB-lasers ontwik-



Figuur 6: Schematische voorstelling van het ontwerp van de DFB-laser met aanzicht in dwarsdoorsnede van de adiabatische structuur en het zijaanzicht van het DFB-rooster. SEM-afbeeldingen van a) overgang tussen DFB sectie en passieve siliciumgolfsgeleider, b) longitudinale dwarsdoorsnede van het DFB-rooster en c) het modeprofiel in de versterkingssectie.

keld door de SOA's te integreren op een eerste orde diffractierooster. Het siliciumgolfsgeleiderplatform bestaat uit een 400 nm dikke Si-golfsgeleiderlaag op een 2 μm dikke oxide laag (BOX). De Si-golfsgeleider in het versterkingsgedeelte van de DFB-laser is 2,0 μm breed en heeft een etsdiepte van 20 nm. De golfsgeleider wordt gedefinieerd door het etsen van 3,0 μm brede sleuven. 50 nm PECVD SiN wordt afgezet en periodiek geëtsd op de bovenkant van de Si-golfsgeleider om het diffractierooster te definiëren. Het ontwerpschema en de longitudinale doorsnede worden geïllustreerd in Fig. 6. De serieweerstand van de laser is 8,0 Ω . Figuur 7(links) toont de LI-curve voor de DFB-laser bij verschillende bedrijfstemperaturen. Een enkelzijdig golfsgeleidergekoppeld optisch vermogen van 9,1 mW, 6,9 mW en 2,8 mW wordt verkregen bij 15 $^{\circ}\text{C}$, 20 $^{\circ}\text{C}$ en 25 $^{\circ}\text{C}$, respectievelijk. De drempelstroom bij 20 $^{\circ}\text{C}$ is 80 mA en neemt toe met de stijging van de bedrijfstemperatuur. De differentieel efficiëntie is 0,27 W/A bij 20 $^{\circ}\text{C}$. Monomodale



Figuur 7: (boven) Golfgeleider-gekoppeld uitgangsvermogen (enkel-zijdig) als functie van stroom voor verschillende bedrijfstemperaturen en de stroom-spanningskarakteristiek, (onder) Gemeten spectrum (0,05 nm resolutie) bij 90 mA en 20 °C bedrijfstemperatuur.

werking bij een golflengte van 1558,3 nm met een onderdrukking van de zijmode van meer dan 33 dB wordt verkregen bij 90 mA, zoals te zien in Fig. 7(rechts). De DFB stopband is 2 nm breed, wat overeenkomt met een κL van 2,6.

Bovendien demonstreerden we ook DBR-lasers met behulp van de ontwikkelde technologie en onderzochten we het effect van het micro-transfer-printen op de prestaties van de laser, met name de drempelstroom. Micro-transfer-printing kan extra verlies in de lasercaviteit veroorzaken en daardoor de drempelstroom verhogen. We vonden echter geen verband tussen de drempelstroom en de verkeerde uitlijning tussen de III-V en Si-golfgeleider.

English Summary

In this work, we develop micro-transfer-printing technology for integrating processed SOA devices on silicon waveguide circuits and use them to demonstrate DFB and DBR lasers.

Photonics has been recently coined as one of the disruptive technologies of the next decade. Photonic integrated circuits are in particular used to generate, manipulate and detect light on the micron scale. One of the several applications include optical interconnects that are crucial for the prospective growth of the datacom industry. Optical interconnects consist of transmitters and receivers for high speed data transfer in a data center. Other rapidly growing market segment is LiDAR. In some implementations, LiDAR relies on photonic integrated circuits to produce miniature low-cost sources and detectors. Silicon photonics is a promising platform for low-cost and high volume manufacturing of the photonic integrated circuits. Inherently, it is challenging to produce efficient and high-performance light sources in Si. Therefore, other materials such as III-V semiconductors need to be integrated on the SOI substrate.

Several heterogeneous integration techniques have been developed over the years: direct and adhesive bonding, monolithic integration, regrowth on a bonding template and flip-chip integration. Some of these techniques are technologically more mature than the others and they all have their own pros and cons. Micro-transfer printing is a novel technique for the integration of opto-electronic devices. It offers the combined benefits of flip-chip and adhesive bonding, which means that pre-processed and tested devices can be picked and placed massively parallel. The technique takes advantage of the viscoelastic properties of the PDMS stamp used to pick up and print devices. The stamps, depending on their kinetic energy, can behave either as an elastic or viscous material. This simply means that when stamps that are laminated with the devices are removed with high velocity, the devices get attached to the PDMS stamp. On the other hand, when the stamp is slowly removed after printing the coupons on the target wafer and a shear

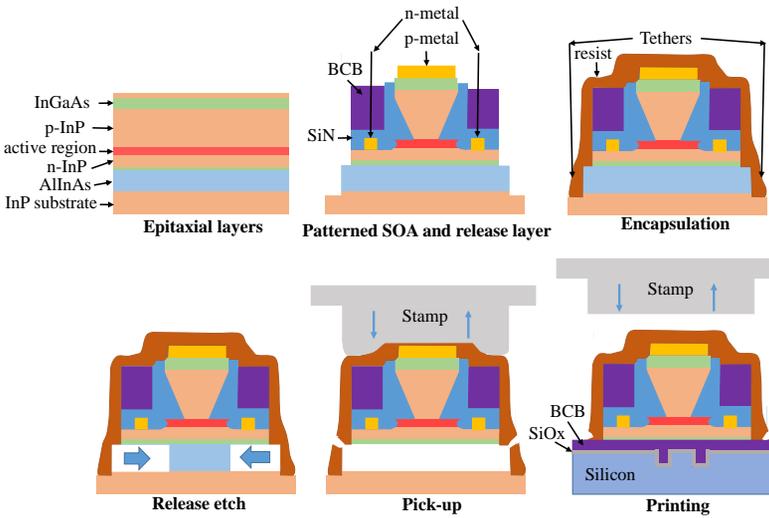


Figure 8: Schematic illustrating the micro-transfer printing process of pre-processed SOA coupons.

force is applied, the devices get detached from the stamp. Hence, dependent on the size of the stamp and the number of posts, multiple devices can be transferred from the source substrate to the target substrate.

Figure 8 depicts the process flow for the micro-transfer printing of patterned SOA coupons. The III-V SOA is patterned on the InP wafer. This patterning involves the formation of the SOA mesa, patterning of the QWs, contact-metal deposition, planarization using DVS-BCB and etch-back of the DVS-BCB and SiN and patterning of the coupon boundary. The sacrificial layer is then patterned and coupons are encapsulated with a photoresist. The sacrificial layer which is AlInAs in our case is under-etched. At this point, the coupons are held in place by tethers anchored to the substrate. The next step is to mount the released III-V SOA sample and the SOI sample on their respective translation stage in the micro-transfer printing tool. This tool uses image processing to align the source and target coupons in the x-y plane. Alignment markers are patterned on both the III-V coupons and on the SOI target to align each coupon with respect to the Si waveguide circuit in the x-y plane. After all the coupons have been printed, the encapsulation from the printed coupons is removed and the DVS-BCB adhesive layer is fully cured to strongly bind the coupons at the printed location. The final processing step is to deposit metal pads to probe the device. Figure 9 shows microscope images of the III-V-on-Si SOAs at various processing

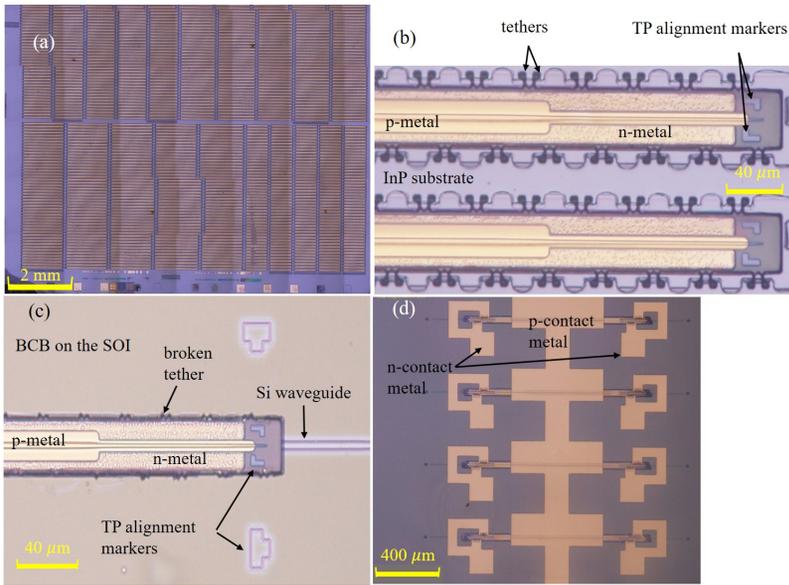


Figure 9: Microscope image of a) processed SOA coupons on the InP substrate, b) two zoomed-in SOA coupons from (a), c) micro-transfer-printed SOA coupon on a Si waveguide, and d) III-V-on-Si SOAs with contact pads.

steps.

The alignment of the III-V SOA with the Si waveguide is an important parameter. The state-of-the-art micro-transfer printing tools can provide an alignment tolerance of $\pm 1.5 \mu\text{m}$ (3σ). This means that the evanescent III-V/Si adiabatic taper must have good coupling efficiency within the aforementioned alignment tolerance. This is particularly important for the development of high gain SOAs. Therefore, we designed two adiabatic tapers taking $1.0 \mu\text{m}$ alignment tolerance and $1.5 \mu\text{m}$ as the worst case for full coupling and partial coupling into the III-V SOA. The partial-coupling III-V adiabatic taper is design for coupling into a $3.0 \mu\text{m}$ wide hybrid III-V/Si waveguide, whereas, in the full-coupling design the III-V and Si are both inversely tapered. Figure 10 illustrates the shape of the two adiabatic taper designs and coupling efficiency against the lateral misalignment. The calculated coupling efficiency for both the partial-coupling and full-coupling designs are greater than -0.3 dB for $1.0 \mu\text{m}$ misalignment. In the partial-coupling design a $1.5 \mu\text{m}$ misalignment leads to 1dB excess loss.

The SOA epitaxial stack has a 200 nm highly doped p-InGaAs contact layer, a $1.5 \mu\text{m}$ p-InP cladding, a 25 nm InGaAsP etch stop layer, a pair

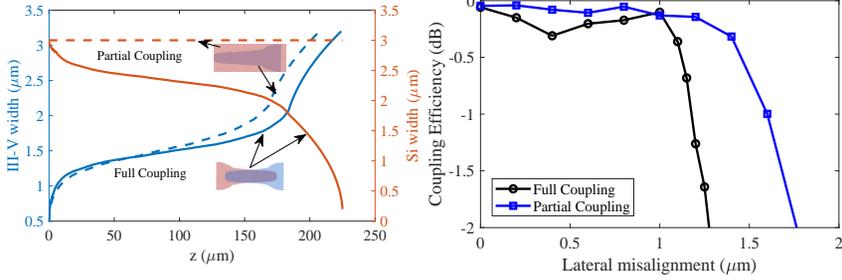


Figure 10: (left) The III-V and Si adiabatic taper width variation along its length. The blue line and the left vertical axis represents the III-V adiabatic taper shape for the partial and full coupling designs. The red line and the right vertical axis represents the Si adiabatic taper shape and Si waveguide width in the case of full coupling and partial coupling, respectively; (right) The simulated coupling efficiency of the adiabatic taper structures for the partial and full-coupling designs versus the lateral misalignment.

of 40 nm AlGaInAs transition layers separating InP from SCH layers, a pair of 75 nm AlGaInAs SCH layers, an active region with 6 AlGaInAs QWs sandwiched between AlGaInAs barrier layers, a 200 nm n-InP contact layer with 60 nm intrinsic InP layer underneath and a 50 nm/500 nm InGaAs/AlInAs release layer grown on the InP substrate.

We developed two III-V-on-Si SOA designs that either have or do not have a Si waveguide underneath the gain section of the SOA. This allows to vary the confinement of the optical mode in the quantum wells and hence tune the small-signal gain and output saturation power. The Si waveguide layer is 400 nm thick and has a 180 nm etch depth. The buried oxide (BOX) layer is 2 μm thick underneath the Si waveguide layer. Both SOA designs, full coupling (higher optical confinement in the QWs) and partial coupling (lower optical confinement in the QWs), are illustrated in Fig. 11. The III-V-on-Si SOA is placed on a temperature-controlled stage at 20 $^{\circ}\text{C}$ for the measurements. The PIC is optically probed with cleaved standard single mode fibers using a fiber stage. Grating couplers are used to interface with the optical fibers. The grating couplers that couple light into the PIC have a wavelength-dependent transmission. Therefore, it is necessary to characterize the grating coupler efficiency as a function of wavelength to measure the on-chip gain of the amplifiers accurately. In order to do this, reference passive Si waveguides are also fabricated along with amplifiers on the same chip and they undergo the same processing steps as the grating couplers used for interfacing with the SOAs. The wavelength-dependent

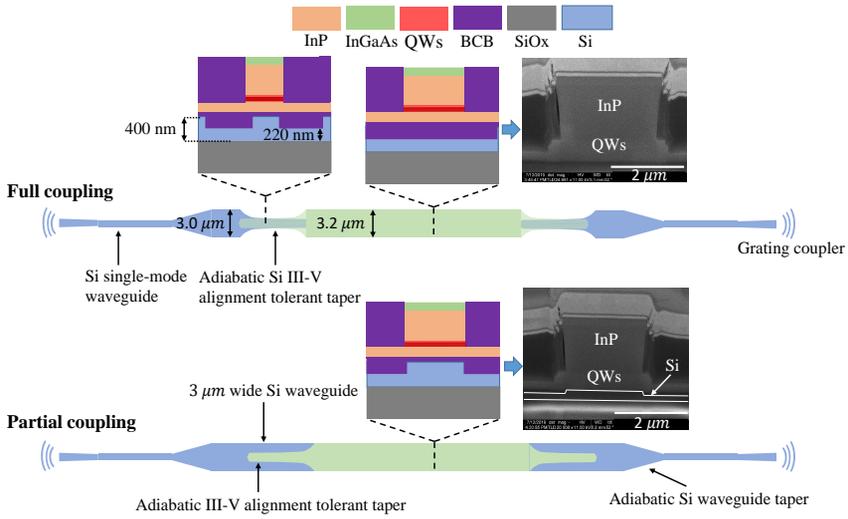


Figure 11: Schematics and FIB cross-sections illustrating the design of the full-coupling and partial-coupling III-V-on-Si SOAs.

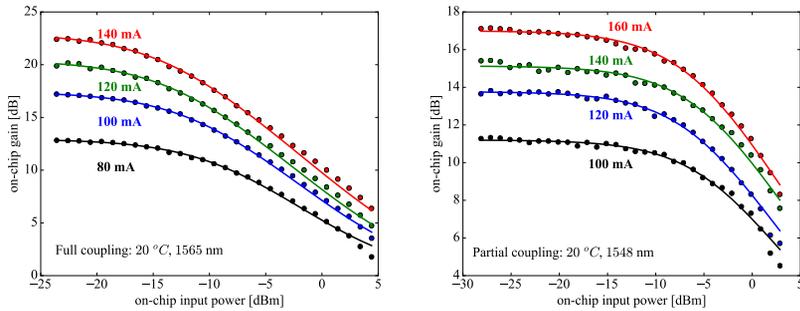


Figure 12: Variation of the on-chip gain with the on-chip input power for various bias currents, (left) for the full-coupling design at 1565 nm, (right) for the partial-coupling design at 1548 nm.

transmission response of the grating coupler is measured using a tunable laser (Santec TSL-510) and an optical spectrum analyzer (OSA, Advantest Q8381A). The angle of the fiber holders is optimized to align the maximum transmission wavelength of the grating couplers with the gain peak of the two discussed SOAs. Since the III-V SOAs printed on both SOI designs are nominally the same, the differential resistance is also nominally the same, 10.0Ω at 80 mA bias current or 1.8 kA/cm^2 current density. Figure 12 illustrates the measured on-chip gain of the SOAs at multiple input bias currents. The maximum output power is 10.8 dBm for the

full-coupling design (at 140 mA) and 11.3 dBm for the partial-coupling design (at 160 mA). P_{sat} is 9 mW and 15 mW for the full (at 140 mA) and partial (at 160 mA) coupling SOA, respectively. The partial-coupling SOA (lower confinement in the QWs) has a small signal gain of 17 dB. In comparison, the full-coupling SOA (higher confinement factor in the QWs) has a small signal gain of 23 dB. Hence, the SOA with higher optical confinement factor can provide more gain, however, has lower saturation power and vice versa. The 3-dB gain bandwidth of the SOA increases with the bias current and it is 30 nm at 120 mA (2.71 kA/cm²). Similar gain bandwidth is obtained for the partial-coupling device. At 100 mA and 1565 nm, $F_{\text{sig-ASE}} \approx 8.6$ dB for an on-chip input power of -24 dBm and $F_{\text{sig-ASE}} \approx 9.54$ dB at 0 dBm on-chip input power. Similarly, at 1548 nm the partial-coupling SOA has $F_{\text{sig-ASE}} \approx 7.0$ dB at -24 dBm on-chip input power and $F_{\text{sig-ASE}} \approx 8.6$ dB at 0 dBm on-chip input power. The SOAs performance is comparable to the devices made using other heterogeneous integration technologies such as die-to-wafer bonding.

In the next step, we developed III-V-on-silicon DFB lasers by integrating the SOAs on a quarter-wave-shift DFB grating. The silicon waveguide platform consists of a 400 nm thick Si device layer on a 2 μm thick buried oxide (BOX). The Si waveguide in the gain section of the DFB laser is 2.0 μm wide and has a 20 nm etch depth. It is defined by etching 3.0 μm wide trenches. 50 nm PECVD SiN is deposited and etched periodically on the top of the Si waveguide to define the quarter-wave-shift grating. The design schematic and the longitudinal cross-section are illustrated in Fig. 13. The differential series resistance of the laser is 8.0 Ω . Figure 14(left) shows the LI curve for the DFB laser at various operating temperatures. Single-sided waveguide-coupled optical power of 9.1 mW, 6.9 mW and 2.8 mW is obtained at 15 $^{\circ}\text{C}$, 20 $^{\circ}\text{C}$ and 25 $^{\circ}\text{C}$, respectively. The threshold current at 20 $^{\circ}\text{C}$ is 80 mA and increases with the increase in operating temperature. The slope efficiency is calculated to be 0.27 W/A at 20 $^{\circ}\text{C}$. Single mode operation at 1558.3 nm (resolution of 0.05 nm) with a side mode suppression better than 33 dB is obtained at 90 mA, shown in Fig. 14(right). The stop band is 2 nm wide which corresponds to a κL of 2.6.

Moreover, we also demonstrated DBR lasers using the developed micro-transfer-printed SOAs and investigated the effect of the micro-transfer printing on the performance of the laser, particularly the threshold current. Micro-transfer-printing can introduce additional loss into the laser cavity and therefore can increase the threshold current. However, we found no correlation between the threshold current and the misalignment between the III-V and

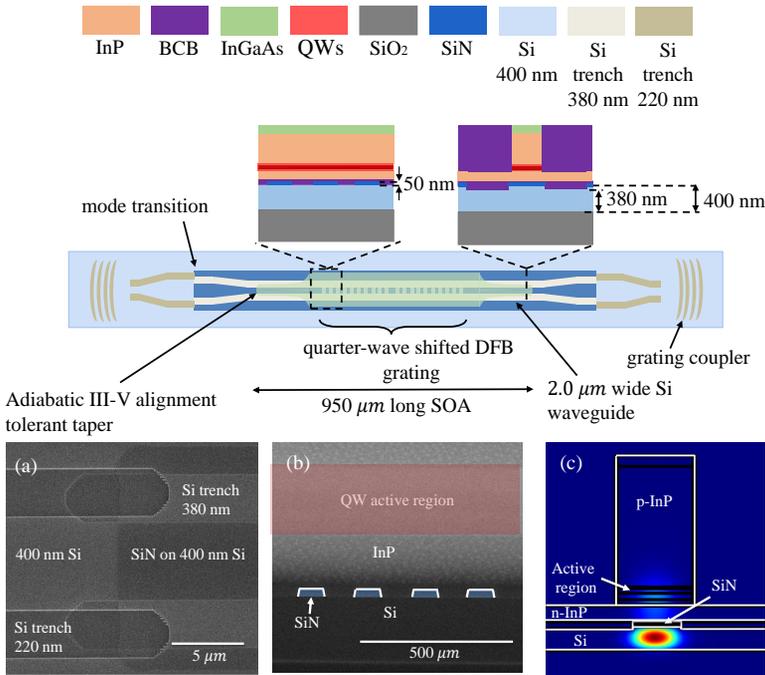


Figure 13: Schematic illustrating the design of the DFB laser with cross-section view of the adiabatic taper and the side view of the DFB grating. SEM images of a) mode transition, b) longitudinal cross-section of the DFB grating and c) the mode profile in the gain section are also shown.

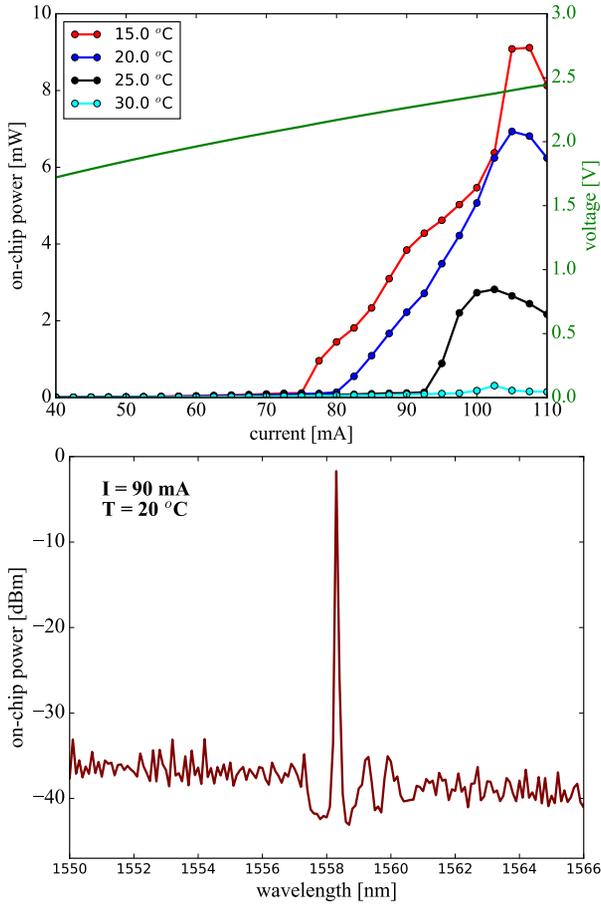


Figure 14: (top) Waveguide-coupled output power (single-sided) as a function of bias current for various operating temperatures and the current-voltage characteristic, (bottom) Measured spectrum at 0.05 nm resolution, at 90 mA and at 20 °C operating temperature.

Si waveguide.

1

Introduction

Photonic integrated circuits (PICs) are now being widely used both commercially and for research and development. The market was valued at USD 385.5 million in 2017 and is expected to reach USD 1.4 billion by the end of 2023 as illustrated in Fig. 1.1 [1]. Telecom and datacom is one of the major market segments for PICs (high-speed optical transceivers). These PICs enable many complex functionalities on-chip with a compact footprint and high reliability. Moreover, the current state-of-the-art wafer-level PIC manufacturing processes have reduced the manufacturing cost significantly as compared to conventional technologies relying on bulk optics and complex assembly. There are several mature PIC platforms such as monolithic InP, Si photonics and many more are under development (AlGaAs-on-insulator, LiNbO₃-on-insulator, etc.) [2, 3]. Moreover, wafer-level hybrid and heterogeneous integration of different materials have also shown promising results. Each of the aforementioned material platforms and integration techniques are attractive depending on the application, cost and density of components required to achieve the desired functionality. In this chapter, we will discuss various photonic integration platforms. Furthermore, we will discuss the emerging micro-transfer-printing technology and its features. However, before delving into PIC technology, a few major applications will be discussed in the next section.

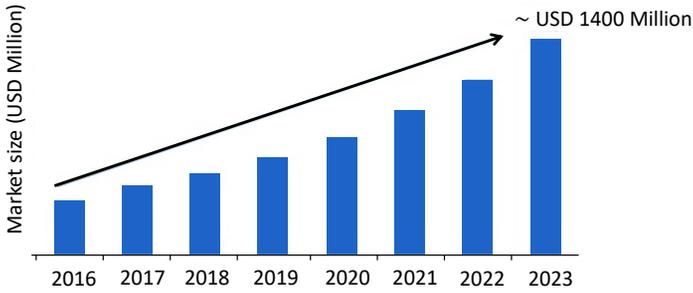


Figure 1.1: Expected PICs market growth, reproduced from [1]

1.1 Applications

1.1.1 Photonics and optical interconnects

Over the last century electronics ICs has significantly impacted the way we live. They can be found everywhere, for example in cars, computers, home appliances, healthcare tools etc. The human race is going through a digital transformation; today we spend a large amount of our time on digital devices, either for work, education or for connecting to people around us. Recently, the outbreak of Covid-19 has been a catalyst for businesses to evolve and to digitize all their processes and services. Therefore, the advent of electronic ICs can be considered one of the most important achievements of the 20th century. This was all possible because of the ever evolving CMOS manufacturing and the persistent effort to follow Moore's law.

The case of photonics seems to be no different. The invention of optical fibers and semiconductor lasers were a seminal stepping stone for photonics. Photonics runs the internet of today and connects most of the world through an optical fiber network. In 2020, the year of the pandemic, it would have been very difficult for businesses to survive without the infrastructure and years of research in optical fiber communication.

The internet technologies have developed at a meteoric rate. Social networking, online-video streaming, cloud computing and other web applications have astronomically increased the online data traffic and the demand for storage capacity. This can be seen from the growth of hyper-scale data centers worldwide in Fig.1.2. They are expected to grow approximately two-fold from 2016 to 2021. Moreover, it is also estimated that by the end of 2021 the annual global data center IP traffic will reach 20.6 Zettabytes (ZB), up from 6.8 ZB in 2016 [4]. Due to the ever-increasing number of devices, applications and online services, photonic components and circuits are being used to meet the demand of high-bandwidth and capacity as

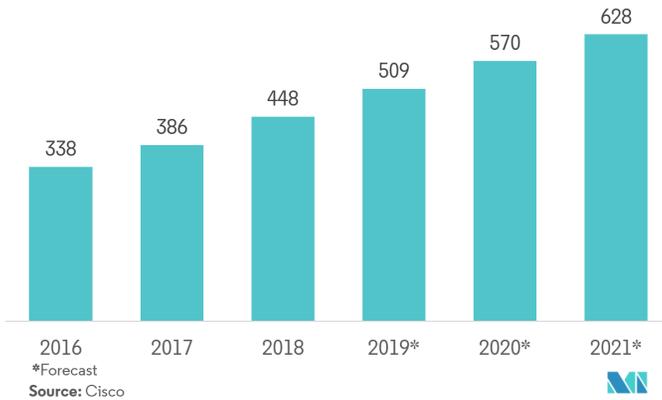


Figure 1.2: Predicted two-fold increase in hyper-scale data centers from 2016 to 2021 [4]

compared to electrical copper cables used in the past. However, these components and circuits require constant improvements in terms of bandwidth and energy consumption to meet the ever growing demand. This calls for solutions that can be easily scaled up and requires intimate integration of electronics and photonics. Therefore, the development of advanced integrated photonic circuits is crucial and will continue to play an important role in the datacom and telecom industry.

1.1.2 Spectroscopy and sensing

Light interacts with matter in a unique way depending on its constituent molecules and the state of matter. Many chemical species exhibit strong absorption in the Ultra-Violet/Visible (UV/Vis) (200 nm - 700 nm), near infrared (NIR) (700 nm - 2.5 μm) or mid-infrared region (MIR) (2.5 μm - 14 μm). The absorption lines are distinct for each chemical species and are the source of identification and concentration measurement. There are multiple origins of absorption lines depending on the spectral region, for example, UV/Vis photonics probe the electronic transitions, whereas, MIR photons are associated with the rotational and vibrational states of the molecules and near-infrared with the overtones of the rotational and vibrational states. In the MIR region, often called the "fingerprint region", various naturally occurring gasses have narrow distinct absorption lines. In the near-infrared, the strength of the absorption lines is weaker, since they are overtones of the fundamental transitions in the MIR region. How-

ever, high-quality and inexpensive sources and detectors are readily available in the near-infrared due to several years of research in telecommunication systems. This makes the near-infrared region attractive for sensing applications despite the lower absorption cross-section as compared to the MIR [5].

In simple terms, absorption spectroscopy can be described by the Beer-Lambert law

$$I(\lambda) = I_0 e^{-\alpha(\lambda)L} \quad (1.1)$$

where I is the intensity of light through the gas path, I_0 is the incident light intensity, α is the absorption coefficient at a particular wavelength λ defined as the product of gas concentration and the specific absorptivity of the gas in $\text{cm}^{-1}\text{atm}^{-1}$, and L is the optical path length. The absorption cross-section σ_a is defined as

$$\sigma_a = \alpha/\rho \quad (1.2)$$

where ρ is the molecular density in $\text{molecules}/\text{cm}^3$. σ_a defines the absorption strength per molecule at a given temperature, pressure and state. Another important parameter is the absorbance $A = 1 - I/I_0$. It can be approximated in the case of small αL as

$$A = \frac{I_0 - I}{I_0} \approx \alpha L \quad (1.3)$$

A is a unitless quantity and it is often quantified in absorbance units (AU). Moreover, often times the limit of detection of a spectrometer is also calculated in noise equivalent absorbance (NEA) or minimum detectable absorption coefficient α_{min} . NEA is the value of the absorption at which signal-to-noise ratio equals unity. Figure 1.3 and 1.4 depict the absorption spectra of some gasses that are e.g. released during a fire, and detecting and measuring the concentration of these gasses can aid fire fighters in their risk assessment.

Small and portable gas sensors also have a high demand for industrial monitoring and in assuring the health and safety of the staff on-site. Integrated photonics can play an important role in developing such miniaturized sensors to detect the unique spectral lines associated with a particular molecule. An integrated optical sensor consist of three main components: 1) appropriate light sources and detectors, 2) a probing structure which can be a waveguide in the case of a fully integrated sensor on-chip or a multi-path gas cell, and 3) electronics for driving lasers and reading out detectors depending on the method of spectroscopic sensing. In this work, we will mainly focus on the development of integrated laser sources through

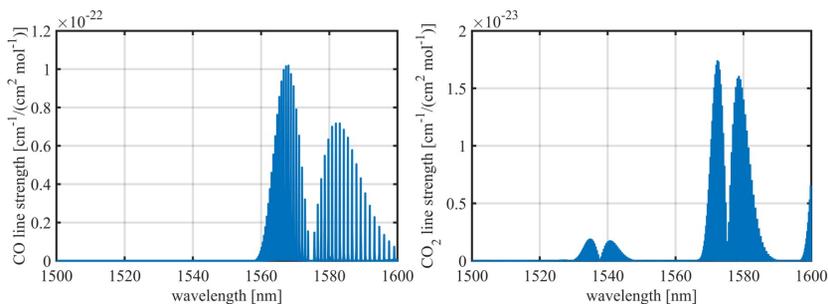


Figure 1.3: Absorption spectra of pure CO and CO₂ (100 % by volume) in the NIR spectral region at 273 K and 1 atm pressure.

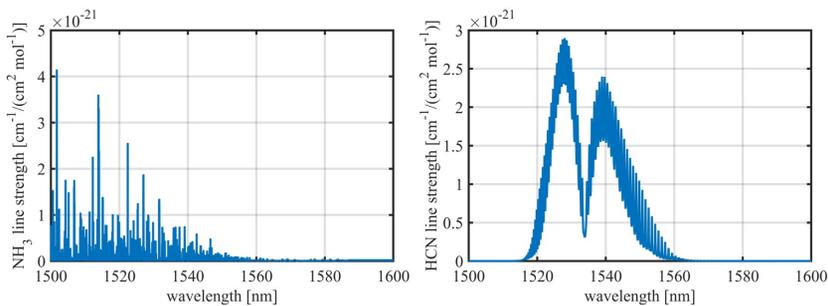


Figure 1.4: Absorption spectra of pure NH₃ and HCN (100 % by volume) in the NIR spectral region at 273 K and 1 atm pressure.

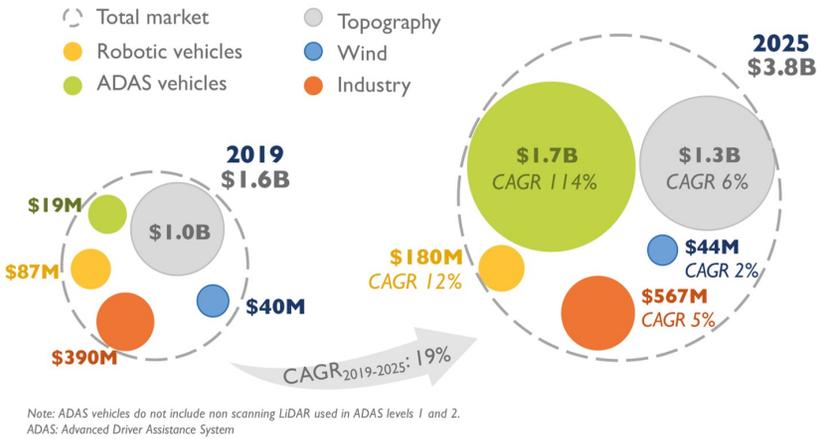


Figure 1.5: LiDAR market forecast by Yole development [6]

micro-transfer printing of pre-fabricated III-V semiconductor optical amplifiers (SOAs). This integration technique has the potential to integrate different laser sources on a single chip to realize ultra-wide tunability for the spectroscopy of multiple gas species.

1.1.3 Light detection and ranging (LiDAR)

LiDAR has become very popular in the last few years as major high-tech companies, and recently big automobile companies like Volvo and Audi are in the race to develop autonomous self-driving cars. Startups like Luminar and Aeva have received significant attention recently as they secured large investments from automobile industry for the development of their LiDAR technology. Moreover, the iPhone 12 Pro includes a LiDAR with a range of 5 m to enable 3D mapping and AR experience. The LiDAR market is expected to reach 3.8 billion dollars in 2025 as shown in Fig. 1.5. Currently, there are five major application segments of the LiDAR market: Robotic vehicles, ADAS (Advanced driver-assistance systems) vehicles, Topography, Wind and Industry [6].

A typical LiDAR uses one or more laser beams to scan its field of view. A beam steering system aids in directing the laser beam. The light from the lasers is intensity or frequency modulated. The reflected light from the surrounding is captured by a detector system. A fast-electronics system filters the signal and determines, in conjunction with models and algorithms, the distance and velocity of the surrounding objects with respect to the scanning system. The output of a LiDAR system includes 3D point clouds and

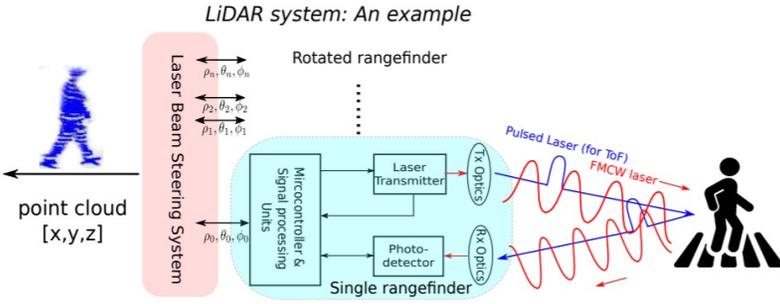


Figure 1.6: A conceptual diagram of a LiDAR system [7]

reflected intensities from the surrounding. An example of such a LiDAR system is shown in Fig.1.6.

Direct detection and coherent detection are both used. The difference lies in the type of laser signal modulation. Direct detection utilizes a pulsed laser signal to measure the time of flight (ToF). On the other hand, if the laser signal is frequency modulated continuous wave (FMCW), coherent detection is used which can measure both distance and velocity (Doppler effect).

A time-of-flight (TOF) range finder measures the range by calculating the time difference between the transmitted and received signal

$$r = \frac{1}{2n} c \Delta t \tag{1.4}$$

where c is the speed of light, n is the refractive index of the propagating medium ($n = 1$ for air) and Δt is the time difference between the transmitted and the received signal. TOF LiDARs are currently prevalent in the market, however, their range is limited by the maximum allowed eye-safe laser power. Another caveat is the possible interference of the received signal with an external light source such as the sun or laser light from other LiDARs.

In the FMCW LiDAR the received and transmitted signal are mixed, which allows recording the frequency shift, therefore, making it possible to calculate the distance and velocity of the target. Figure 1.7 shows an example of transmitted, received and mixed signal in a coherent LiDAR system. The mixed signal is obtained by mixing transmitted and received signal. It consists of two intermediate frequencies f_{if}^- and f_{if}^+ , that can be used to compute the distance and velocity of the reflecting object.

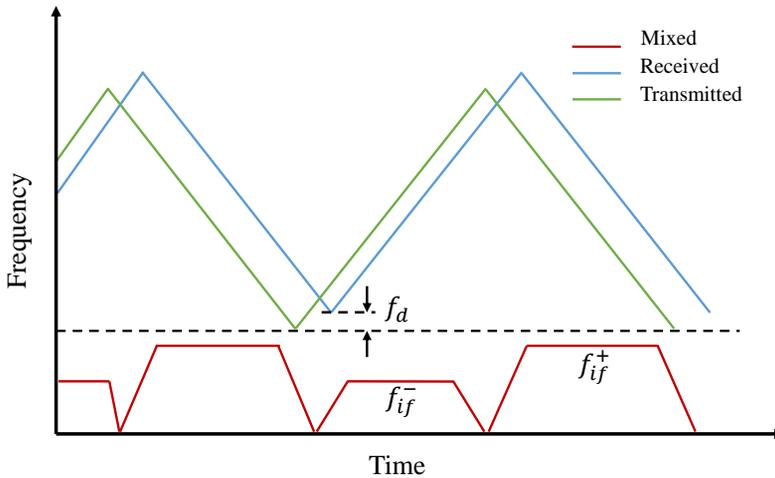


Figure 1.7: An example of received, transmitted and mixed signal in coherent LiDAR system.

The power reduces quadratically with the distance r . Furthermore, at adverse weather conditions such as snow, fog, rain etc. the laser beam gets scattered and absorbed reducing the received power further. However, as the power can't be increased beyond the eye safety limit, the overall collection efficiency of the system, the sensitivity of the receivers and the algorithms must be optimized to render the LiDAR operational. Integrated photonics can help in this respect, especially in the case of FMCW LiDAR as coherent detection is readily implemented on a photonic integrated circuit, and the micro-transfer printing of lasers and photodetectors on such a platform can push this field forward.

1.2 Silicon Photonics

1.2.1 Silicon-on-insulator PICs

Silicon has been the most important material for the electronics industry in recent history. The ability to fabricate very large scale electronic integrated circuits with high throughput, high yield and in large volumes have made sophisticated high-tech gadgets, partially autonomous automobiles, state-of-the-art health care etc. possible and affordable. Over the years, the semiconductor industry has followed Moores's law to produce cheaper and better electronic ICs and this has enabled unprecedented technological ad-

vancements in the last few decades [8]. They were able to do the aforementioned by reducing the size of each transistor. The 5 nm CMOS technology node is the current state-of-the-art and it features 130-230 million transistors per square millimeter [9]. Silicon photonics (SiPh) manufacturing also takes place in semiconductor foundries using CMOS manufacturing technology, however, on the older technology nodes such as the 90 nm node in the case of Globalfoundries because a thicker Si device layer and BOX is required to develop low-loss waveguides.

One of the most promising integrated photonics platforms is silicon-on-insulator (SOI). It consists of a silicon substrate (200 mm or 300 mm in diameter), a thermally grown silicon oxide layer (1 μm to 3 μm thick) and a silicon device layer (220 nm, 400 nm, 500 nm, and 3 μm thick) [10–12]. The prominent feature of the SOI platform is the high index contrast between the Si and SiO₂ layers which enables high confinement in the waveguide, sub-micrometer geometries, and tight bends. The importance of silicon for photonic integrated circuits (PICs) was realized when silicon waveguides and electro-optic effects in silicon were studied for telecommunication wavelengths [13]. The presence of the CMOS fabrication infrastructure facilitated the rapid growth of research and development efforts in the field of silicon PICs. One of the initial bottlenecks was the high waveguide loss, however, with the development of improved fabrication processes, the waveguide losses dropped to 0.5-2 dB/cm [14]. Several high-performance passive and active components have been demonstrated including low-loss waveguides, arrayed waveguide grating wavelength (de)multiplexers, high-Q microring resonators, low-reflection grating couplers for vertical coupling into the PIC and spot-size converters for horizontal coupling. Similarly, high-speed modulators (typically 50 Gbaud) have been demonstrated in SOI utilizing the plasma dispersion effect [15]. High-speed CMOS-compatible germanium-on-silicon photodetectors have also been realized [16]. On the contrary, the development of a high-performance integrated laser source has been a major bottleneck due to the indirect bandgap of silicon. Most of the efforts to date are focused on the heterogeneous integration of III-V direct bandgap materials on SOI. There are several possible approaches including flip-chip of micro-packaged lasers or bare laser dies, die-to-wafer/wafer-to-wafer bonding of III-V on Si, hetero-epitaxial growth, a mix of wafer-bonding and epitaxial (re)growth, and last but not the least micro-transfer-printing. Some of these approaches will be discussed in the next section.

1.2.2 Heterogeneous III-V-on-Si integration

The Si photonics platform may be ideal for the low-cost dense integration of large scale photonic integrated circuits. However, the indirect band gap is a hindrance to integrate efficient electrically-pumped laser sources and amplifiers. III-V alloys are ideal for this purpose. Multi-quantum-well structures formed in III-V quaternary alloys are widely used to make integrated laser sources. The emission of these alloys can be tuned by varying the composition of the alloy. Thus, in the past few years, significant efforts have been made to integrate III-V epitaxial materials or III-V pre-processed laser sources on silicon waveguide circuits. Several integration approaches exist and have their own advantages and disadvantages. We will discuss some of these in the upcoming sections.

1.2.2.1 Direct or adhesive bonding

In direct or adhesive bonding, III-V wafers (2, 3 or 4 inch) or dies are bonded either by molecular bonding or by a polymer adhesive bonding agent to the SOI wafer. In the former, both surfaces are intimately contacted on an atomic scale. The surfaces are activated either chemically or with plasma. Van der Waals interactions between both surfaces is achieved when the two activated wafer surfaces are attached to each other because of the presence of a H₂O interface layer, which is readily adsorbed at the wafer surface. The following annealing step creates stronger bonds and removes water molecules [17, 18]. The molecular bonding is very sensitive to surface roughness and contamination.

The adhesive bonding technique utilizes a oligomer solution of DVS-BCB which can be either spin-coated or spray-coated on the patterned SOI wafer. In the case of spin-coating the SOI wafer surface is planarized. In the case the wafer has topography, spray coating can be used. After a series of baking steps, the III-V dies or wafers are attached to the SOI wafer and cured at 250 °C for 1 hour to polymerize the DVS-BCB completely. A uniform pressure is applied to the wafer stack during curing to achieve a close contact between both surfaces. DVS-BCB was chosen as the bonding agent because of its optical transparency, excellent planarization properties, low curing temperature and the fact that no outgassing occurs during cure [19]. Several high-performance III-V/Si photonic devices have been demonstrated using direct and adhesive bonding. This technique has been matured and is currently being used in the industry. Several III-V-on-Si bonding technology platforms are available in the academia and industry. The most prominent ones are from UGent-IMEC, UCSB, CEA-Leti and Intel. Nevertheless, the III-V-on-Si wafer/die bonding approach requires significant

change to an existing CMOS-foundry process flow and the integration of different epitaxial materials in close proximity is very challenging.

1.2.2.2 Direct epitaxial growth

Direct epitaxial growth is believed to be the ultimate solution for the integration of III-V semiconductors on Si. However, this approach is not yet mature enough to be utilized in industry. It is challenging to grow high quality and low threading dislocation density III-V layers on Si due to the lattice mismatch of the III-V and Si. Nevertheless, several research groups have demonstrated active devices.

The planar growth of III-V quantum dot stacks can be made possible by introducing intermediate layers such as GaAs-on-V-grooved-Si (GoVS), a GaP buffer layer, or a dislocation filter layer. These aforementioned approaches can significantly reduce the dislocation density [20–22]. The lasers fabricated with quantum dots as active material have several advantages including low threshold current, higher operating temperature and longer lifetime compared to their quantum well counterparts. However, coupling from III-V layers to Si photonic integrated circuit is challenging in the presence of several μm -thick buffer layers.

In contrast to the planar growth, selective-area growth (SAG) is also an emerging technique to monolithically integrate III-V materials on Si and, unlike planar growth, it doesn't require thick buffer layers. In SAG, the III-V materials are grown on patterned Si substrates masked by SiO_2 . The growth on the masked area is much slower which enables selective/controlled growth in the exposed regions. Moreover, it enables techniques such as directional heteroepitaxy, vertical/planar nanowires growth and aspect ratio trapping to reduce the dislocation density. These techniques are described in detail in the PhD thesis of Yuting Shi [23]. However, none of these methods are mature enough to be utilized for volume production in the industry today.

1.2.2.3 Regrowth on a bonding template

A recently emerging III-V-on-Si heterogeneous integration method combines III-V wafer bonding and regrowth of the III-V active and/or passive layers. This enables co-integration of multiple III-V functional layers on SOI PICs. It promises advantages of both III-V wafer bonding and monolithic growth including efficient coupling to the Si PICs, a low dislocation density, and a scalable cost-effective manufacturing [24]. Figure 1.8 shows the process flow of the regrowth on a bonding template integration tech-

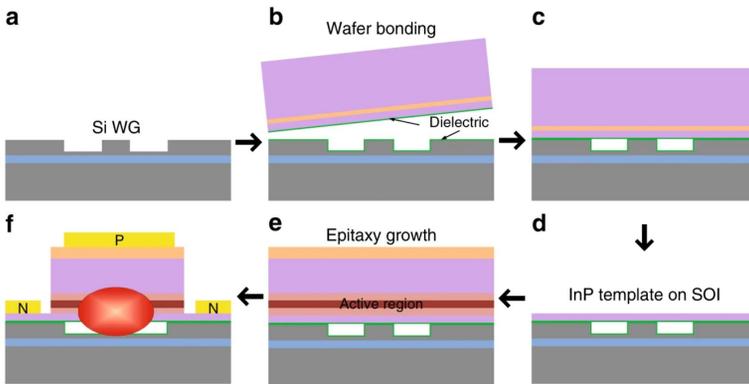


Figure 1.8: Process flow schematic of regrowth on a bonding template III-V-on-Si integration [24]

nique. The first step is to define waveguides and bonding outgassing structures in the SOI substrate. In the following step, an InP substrate with InP template layer and InGaAs etch-stop layer is bonded on the silicon substrate with direct bonding. Subsequently, the InP substrate and InGaAs is selectively etched to leave the InP template layer on top of the SOI. A typical p-i-n laser layer stack is grown on the InP-on-Si wafer in a metal-organic chemical vapor deposition (MOCVD) chamber. The layer stack is then processed to form a laser mesa with electrical connections. The bonded template removes the lattice and polarity mismatch issues without the need of intermediate thick buffer layers usually required for monolithic integration. This technique also promises the growth of a variety of III-V layer stacks using selective area growth techniques. In fact, devices such as DFB laser diodes and MZM modulators have been co-integrated on SOI using this technique [25]. However, one of the major drawbacks of this technique is that the thickness of the epitaxial layers grown are limited to 450 nm as dislocations are observed above the aforementioned thickness [24].

1.2.2.4 Flip-chip integration

In this technique, a III-V laser or an RSOA is attached to the SOI PICs either directly with solder or it is placed in a micro-optical bench (MOB) [26–28]. These MOBs consist of a Si or AlN submount carrying an edge-emitting laser chip, a ball lens for collimating and focusing, an optical isolator and a mirror for deflecting the beam towards the silicon photonic IC as shown in Fig.1.9

The beam from the edge-emitting laser is imaged on the grating cou-

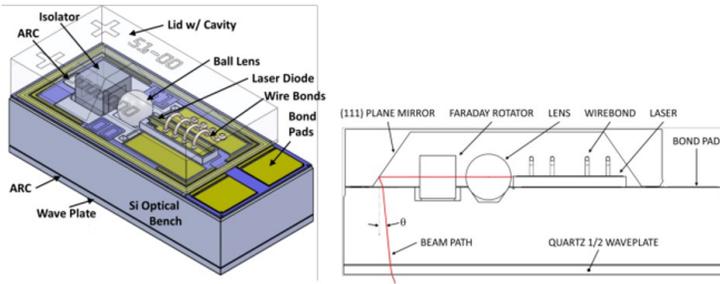


Figure 1.9: Micro-optical bench packaging from Luxtera [29]

pler of the PIC. The MOB is actively aligned with respect to the grating coupler on the PIC. Although the MOB is a mature technology and has the advantages of wafer level assembly, packaging and testing, the complexity of the packaging and sequential active alignment required makes it a resource-intensive solution. Furthermore, coupling with grating couplers can lead to higher coupling loss and limited bandwidth. Waveguide in/out devices such semiconductor optical amplifiers have not been demonstrated using the MOB approach.

1.2.2.5 Micro-transfer printing

Micro-transfer printing is a heterogeneous integration method that allows thin III-V membranes and/or processed devices to be picked from their native substrate and placed onto the desired substrate. In the case of III-V semiconductors, the layer stack has an additional sacrificial layer at the bottom of the functional layer stack that enables picking of the devices and membranes. When processed devices are picked and placed this technique can be very powerful as it allows wafer-level integration, prior electrical testing, and integration of various layer stacks in close proximity on a SiPh circuit. Another advantage of this method is the possibility to integrate III-V devices in trenches. This is particularly useful when integrating III-V devices in various Si foundry platforms. Moreover, the aforementioned is possible without the need to change the foundry process flow. This way it combines the advantages of flip-chip integration and wafer bonding.

In this work, micro-transfer printing will be utilized to integrate SOAs and lasers on SiPh circuits and it will be discussed in more detail in the following chapters.

1.3 State-of-art heterogeneously integrated SOAs

Semiconductor optical amplifiers (SOAs) are a key component in many PICs. Large-scale integration of silicon photonic components for applications like optical beam steering and programmable photonic integrated circuits will need optical amplification to maintain sufficient output power as light passes through multiple optical components. For the aforementioned applications the desired SOA attributes are high gain and/or high output power. Additionally, the seamless integration of SOAs with SiPh integrated circuits can enable the development of state-of-the-art advanced lasers. In these lasers, the SOA and the Si PIC provides the gain and feedback, respectively. A prominent example is a widely tunable laser with a booster amplifier to increase output power. This is particularly useful in longer reach DWDM links, in addition to providing higher optical launch powers per channel the SOA can be used for power flattening [30]. In the next section, we will discuss the most common figures of merit of SOAs.

1.3.1 Figures of Merit

SOA figure of merits include the unsaturated gain factor G_o which is defined as the ratio of output power to input power at low input power levels, the input saturation power which is the input power at which the gain is half the unsaturated value $G_o/2$, the saturated output power and noise figure. The gain of an SOA decreases with the increase of input power. It can be modelled as [31]:

$$G(P_{in}) = G_o \frac{1 + \frac{P_{in}}{P_{sat}}}{1 + G_o \frac{P_{in}}{P_{sat}}} \quad (1.5)$$

where G_o is (peak) unsaturated gain, P_{in} is the input power, and P_{sat} is the power for which the gain coefficient (per unit length) drops by a factor of 2. It is evident from equation 1.5 that G decreases with P_{in} and eventually approaches 1 when $P_{in} \gg P_{sat}$. P_{sat} can be calculated using the following expression [31]:

$$P_{sat} = \frac{hc}{\Gamma} \frac{\sigma_{xy}}{a\tau\lambda} \quad (1.6)$$

where σ_{xy} is the quantum well cross sectional area, λ is the wavelength, a is the differential gain, Γ is the confinement factor in the pumped region of the quantum wells, h is Planck's constant, τ is the carrier lifetime and c is the speed of light in vacuum. When operating the SOA at high bias current, a (in SL-MQW material) and τ reduces, which increases P_{sat} . As

indicated by equation 1.6, P_{sat} can be increased by reducing the confinement factor (decreasing the modal gain) and increasing the cross-sectional area of the active area (increasing the power consumption). These trade-offs must be taken into consideration during the design process. Typically, the SOA noise consists of two components: Signal-to-ASE beat noise and shot noise and the noise figure (NF) of the SOA is calculated from the recorded spectrum attributed to Signal-to-ASE beat noise [31].

$$NF = \frac{2\lambda^3}{Gc^2h} \frac{P_{ASE}}{\delta\lambda} + \frac{1}{G} \quad (1.7)$$

where G is the on-chip gain. The on-chip P_{ASE} is measured in a wavelength range of $\delta\lambda$ for a given input power using the OSA. The final important figure of merit is the wall-plug efficiency (WPE) and it is defined as [32]:

$$WPE = \frac{P_{out}(mW) - P_{in}(mW)}{I_{gain}(mA) \times V_{gain}(V)} \times 100 \quad (1.8)$$

WPE is simply the ratio of optical power generated to the electrical power provided to the SOA. In the following section, we will present a concise review of literature on III-V-on-Si SOAs.

1.3.2 Review on III-V-on-Si SOAs

Heterogeneous III-V-on-Si SOAs have mostly been implemented by utilizing direct bonding and adhesive bonding of MQW III-V layer stacks and by monolithic integration of quantum dot layer stacks.

One of the earliest demonstrations of SOAs can be traced back to 2007. III-V epitaxial layers were bonded with oxygen plasma-assisted wafer bonding to realize integrated photodetectors and SOAs on a Si waveguide circuit. A taper structure evanescently coupled the light from III-V to Si. The SOA mesa was 14 μm wide and had 4 μm opening in the proton implantation to constrain the flow of charge carriers. The epitaxial layer stack had 8 AlGaInAs QWs. Additionally, the SOA was 1240 μm in length and had a small signal gain of 9.5 dB at 1575 nm [33]. In another demonstration by the same research team, 13.0 dB and 11 dBm of small signal gain and output saturation power was reported [34].

In 2012, an SOA was demonstrated using a 40 nm thick DVS-BCB adhesive bonding layer. The adiabatic tapers on both sides of the SOA coupled light to a 400 nm thick Si waveguide. The III-V mesa was 2 μm wide and 400 μm in length. The length of the adiabatic tapers were 100 μm . The SOA had a small signal gain of 13 dB at 1560 nm for a 40 mA bias current [35].

In 2015, a directly bonded SOA with intermediate SiO_2 was demonstrated. Similar to the previous demonstration the SOA gain section was coupled to the Si waveguide with adiabatic tapers on both sides. The gain section was $1100 \mu\text{m}$ long and the SOA was fully packaged with fibers attached to the grating couplers. It exhibited 28 dB on-chip gain and 10 dB of fiber to fiber gain. The on-chip input saturation power was -16 dBm [36].

In the same year, another research group demonstrated a III-V-on-Si SOA with high WPE of 12.1% for 2 mW input power. The design of the SOA was optimized to achieve high WPE. The active region of the SOA consisted of eight 7 nm thick AlGaInAs MQWs. The adiabatic taper was also used here to evanescently couple III-V and Si waveguides. The SOA had significantly lower resistance of 3.4Ω resulting in high WPE. The $400 \mu\text{m}$ long SOA exhibited the same gain of 7.5 dB for 0.1 mW and 2.0 mW of input power. The maximum output power reported was 11.42 dBm [37].

In 2016 another manuscript was published which showcased various III-V-on-Si SOAs developed using the direct bonding technique. In this manuscript, the impact of the Si waveguide width was studied in detail which is one of the important design parameters of III-V-on-silicon SOAs. It allows the designer to tune the small-signal gain and the output saturation power without changing the III-V epitaxial layers. The active region had three AlGaInAs MQWs to demonstrate high output saturation power. The design exhibited 25 dB small-signal gain and an output saturation power of 12.35 dBm. Alternatively, the high output saturation power design exhibited 10.9 dB gain and an output saturation power of 14.5 dBm [38]. The performance of the devices was limited by the self-heating of the SOAs and this remains one of the major bottlenecks for III-V-on-Si integrated devices.

Another III-V-on-Silicon SOA was demonstrated with significantly higher output power of 17.5 dBm. The III-V layer stack consisted of six InGaAsP QWs and was adhesively bonded on SOI waveguide with a thin layer of DVS-BCB. The III-V mesa was $5.0 \mu\text{m}$ wide and the silicon waveguide underneath was $4.0 \mu\text{m}$. The wide silicon and III-V waveguide significantly improved the output saturation power of the SOA. Moreover, the SOA has a very low series resistance of 1.4Ω resulting in high efficiency and improved thermal performance. The small signal gain was 27.0 dB [39].

In a recent demonstration of III-V-on-Si SOAs, hetero-epitaxial quantum dots on Si are used as the active region. The quantum dots as an active region have inherently the benefit of low optical confinement which results in higher output saturation power and most importantly they have higher temperature stability. The device was fully grown on a (001) on-axis silicon substrate with a 45 nm GaP buffer layer. First a thick $3.1 \mu\text{m}$ GaAs buffer layer along with dislocation filter layer was grown. The III-V gain

section was 5 mm long and 11.0 μm wide. The SOA exhibited superior performance characteristics with maximum small-signal gain of 39.0 dB, an output saturation power of 23.0 dBm and a wall plug efficiency of 14.8 % at 1314 nm [40]. The SOA was not coupled to a Si waveguide circuit which is challenging in the presence of thick buffer layers.

In this work, we will use a novel heterogeneous integration technique called micro-transfer printing. The goal is to demonstrate an SOA that is better or comparable to III-V-on-silicon SOAs previously demonstrated. In most of the aforementioned SOAs, a large die of III-V was bonded on the Si waveguide and post-processed to form the SOA. We will develop a design and process to transfer print a processed III-V SOA on the desired target site on the Si waveguide circuit. This technique is very promising for the integration of SOAs on mature SiPh foundry process flows without significant modification of the process flow.

1.4 Publications in international journals

1. **Bahawal Haq**, Javad Rahimi Vaskasi, Jing Zhang, Agnieszka Gocalinska, Emanuele Pelucchi, Brian Corbett, and Gunther Roelkens. "Micro-transfer-printed III-V-on-silicon C-band distributed feedback lasers." *Optics Express* 28, no. 22 (2020): 32793-32801.
2. **Bahawal Haq**, Sulakshna Kumari, Kasper Van Gasse, Jing Zhang, Agnieszka Gocalinska, Emanuele Pelucchi, Brian Corbett, and Gunther Roelkens. "Micro-Transfer-Printed III-V-on-Silicon C-Band Semiconductor Optical Amplifiers." *Laser & Photonics Reviews*: 1900364.
3. Camiel Op de Beeck, **Bahawal Haq**, Lukas Elsinger, Agnieszka Gocalinska, Emanuele Pelucchi, Brian Corbett, Günther Roelkens, and Bart Kuyken. "Heterogeneous III-V on silicon nitride amplifiers and lasers via microtransfer printing." *Optica* 7, no. 5 (2020): 386-393.
4. Jing Zhang, Grigorij Muliuk, Joan Juvert, Sulakshna Kumari, Jeroen Goyvaerts, **Bahawal Haq**, Camiel Op de Beeck et al. "III-V-on-Si photonic integrated circuits realized using micro-transfer-printing." *APL photonics* 4, no. 11 (2019): 110803.
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1.5 Publications in international conferences

1. Jing Zhang, Camiel Op de Beeck, **Bahawal Haq**, Jeroen Goyvaerts, Stijn Cuyvers, Sulakshna Kumari, Grigorij Muliuk et al. "Micro-Transfer-Printing for III-V/Si PICs." In *Asia Communications and Photonics Conference*, pp. T4G-3. Optical Society of America, 2020.
2. **Bahawal Haq**, Sulakshna Kumari, Jing Zhang, Agnieszka Gocalinska, Emanuele Pelucchi, Brian Corbett, and Gunther Roelkens. "Micro-transfer-printed III-V-on-Silicon DBR lasers." In *Frontiers in Optics*, pp. FW5D-5. Optical Society of America, 2020.
3. **Bahawal Haq**, Sulakshna Kumari, Jing Zhang, Agnieszka Gocalinska, Emanuele Pelucchi, Brian Corbett, and Gunther Roelkens. "Micro-transfer-printed III-V-on-silicon distributed feedback lasers." In *2020 Optical Fiber Communications Conference and Exhibition (OFC)*, pp. 1-3. IEEE, 2020.
4. Jing Zhang, Grigorij Muliuk, Jeroen Goyvaerts, **Bahawal Haq**, Sulakshna Kumari, Joan Juvert, Camiel Op de Beeck et al. "Heterogeneous integration in silicon photonics through micro-transfer-printing." In *2019 24th Microoptics Conference (MOC)*, pp. 64-65. IEEE, 2019.
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2

Enabling micro-transfer printing of III-V-on-Si SOAs

2.1 Introduction to micro-transfer printing

Micro-transfer printing is a heterogeneous integration technique in which (arrays of) micron-sized films, also referred as coupons, are transferred from a source substrate to a target substrate. This technique can be used to transfer all sorts of different materials, however, in this work micro-transfer printing of processed III-V semiconductor optical amplifiers (SOAs) on a silicon-on-insulator (SOI) waveguide platform is discussed. Polydimethylsiloxane (PDMS) stamps are used to pick and print films and devices with an alignment accuracy of $\pm 1.5 \mu\text{m}$ (3σ) [1]. The technique is particularly advantageous in terms of the usage of the relatively expensive III-V material. Dense arrays of devices can be fabricated on the III-V source wafer and can be transferred in a parallel fashion to the target substrate using a stamp with an array of posts, shown in Fig. 2.1. Therefore, depending on the number of posts in an arrayed stamp many devices can be integrated simultaneously resulting in a high-throughput process. For instance, one printing cycle takes up to 45 s and more than 1000 devices can be printed in that time. Additionally, this allows to integrate devices from different III-V wafers in close proximity on the SOI wafer. It also allows for area magnification as one InP source wafer can populate one or more SOI wafers.

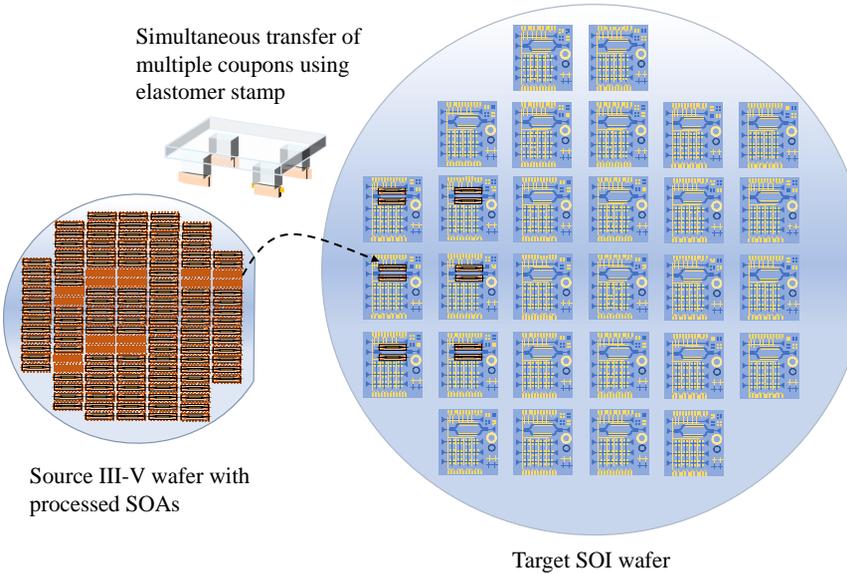


Figure 2.1: Schematic illustrating the micro-transfer printing of four SOA coupons to a SOI wafer using a PDMS stamp.

Below we discuss more physical details of the micro-transfer-printing technology and discuss the hardware used.

2.2 Working principle of micro-transfer printing

One of the key enablers of this technology is the PDMS rubber stamp. It is chosen because of its very high resolution molding capabilities, chemical stability, non-toxicity, low mechanical stiffness, its smooth surface and its viscoelastic properties, enabling a kinetically switchable adhesion to the coupons [2, 3]. The micro-transfer printing can only work if the adhesion of the film or device to be transferred has stronger adhesion with the PDMS stamp than with the source substrate. The viscoelastic property of the PDMS stamp allows its adhesion to be tuned by varying the velocity of the interaction between stamp and device. This can be quantified in terms of separation energy G between stamp and device and the velocity of delamination v as:

$$G = G_0 \left[1 + \left(\frac{v}{v_0} \right)^n \right] \quad (2.1)$$

where G_0 is the separation energy at standstill, v_0 is the velocity at which the separation energy is twice its standstill value ($2G_0$) and n is the fitting

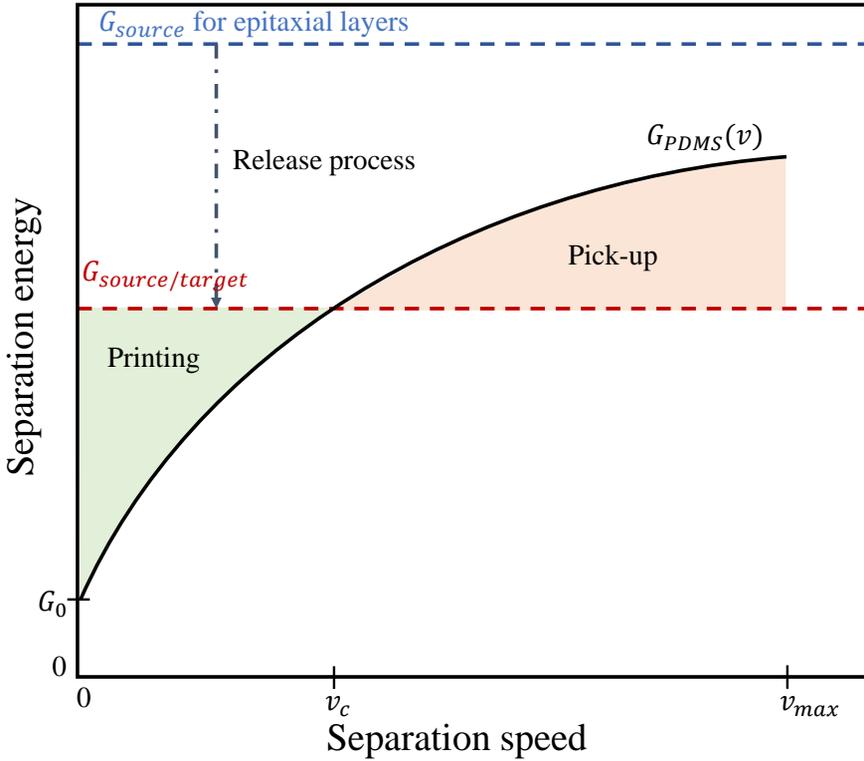


Figure 2.2: Schematic illustrating the dependence of separation energy on the separation velocity of the PDMS stamp. The blue dotted line shows the high separation energy of semiconductor epitaxial layers. For simplicity we assume that $G_{source} = G_{target}$ in this graph.

parameter. From Eq. 2.1, it can be deduced that the separation energy G increases monotonically with the velocity v . Therefore, a high velocity will result in a large separation energy between stamp and the device. This is particularly useful in the picking process, to pick up a film or device. Lower velocity results in lower separation energy and therefore the stamp will delaminate easily from the coupon. This is useful in the printing process, to release the device or film on the target site [4]. In order to transfer print a III-V device the adhesion of the PDMS stamp defined by its separation energy G_{PDMS} to the device should be greater than the adhesion of the III-V device to its substrate G_{source} .

$$G_{PDMS} > G_{source} \quad (2.2)$$

Similarly, for printing the separation energy of the device/substrate in-

terface should be greater than the device/stamp interface.

$$G_{\text{target}} > G_{\text{PDMS}} \quad (2.3)$$

This condition can be satisfied at low peeling velocities. Therefore, for each device/stamp interface there is a critical velocity v_c : if the velocity of the separation is greater than v_c , the device can be picked and vice versa, also shown in Fig. 2.2. The critical velocity v_c can be computed as:

$$v_c = v_0 \left(\frac{G_{\text{source/target}} - G_0}{G_0} \right)^{\frac{1}{n}} \quad (2.4)$$

So far we have assumed that v_c is less than the maximum achievable velocity v_{max} . In other words, the separation energy required to pick-up a device can be produced by the PDMS stamp. However, this assumption is not true for III-V epitaxial layers. The separation energy required for these devices G_S is much higher than the maximum G_{PDMS} possible, shown in Fig. 2.2. This is mainly because of the strong chemical bonds that form semiconductors. These bonds are stronger than the weak Van der Waals bonds formed on the device/stamp interface. Therefore, to pick up the devices fabricated on the III-V semiconductor the adhesion to the substrate should be weakened. This is done by under-etching the sacrificial layer incorporated during the epitaxial growth in the device layer structure. After the under-etching the devices are suspended in the air and held by supporting structures called tethers anchored to the substrate. The strength of these tethers are engineered to support the device after release and to break at the right position during the picking process.

Therefore, to micro-transfer-print III-V semiconductors the epitaxial layer structure should be grown on a sacrificial layer that can be under-etched with a good selectivity with respect to the substrate. Given the successful patterning and release of the device, as mentioned in this section, the released devices can be picked by retracting the stamp with higher velocity and can be printed on the target at lower separation speeds. It is also possible to increase the adhesion of the device/substrate interface at the target site by spin coating a thin adhesive layer, such as DVS-BCB. This is also commonly used in III-V die-to-die or die-to-wafer bonding processes [5]. The micro-transfer-printing process flow is described in the next section.

2.3 Process flow for micro-transfer printing SOAs

The micro-transfer printing of III-V semiconductors is not a straightforward process because of the higher separation energies required, which cannot be

Layer	Type	Material	Thickness (nm)	Doping (cm^{-3})
27	Cap layer	InP	100	nid
26	Contact P	InGaAs(lattice matched)	100	$> 1 \times 10^{19}$
25	Contact P	InGaAs (lattice matched)	100	$\sim 1 \times 10^{19}$
24	Cladding P	InP	1000	$\sim 1 \times 10^{18}$
23	Cladding P	InP	500	$\sim 5 \times 10^{17}$
22	etch stop	InGaAsP ($\lambda_g = 1.17 \mu\text{m}$)	25	$\sim 5 \times 10^{17}$
21	Transition	(Al _{0.9} Ga _{0.1}) _{0.47} In _{0.53} As	40	
20	SCH	(Al _{0.7} Ga _{0.3}) _{0.47} In _{0.53} As	75	
9x6	barrier	(Al _{0.45} Ga _{0.65}) _{0.51} In _{0.49} As	10	
8x6	well	(Al _{0.25} Ga _{0.75}) _{0.3} In _{0.7} As	7.5	
7	barrier	(Al _{0.45} Ga _{0.65}) _{0.51} In _{0.49} As	6	
6	SCH	(Al _{0.7} Ga _{0.3}) _{0.47} In _{0.53} As	75	
5	Transition	(Al _{0.9} Ga _{0.1}) _{0.47} In _{0.53} As	40	1×10^{18}
4	Cladding N	InP	200	2×10^{18}
3	Cladding N	InP	60	nid
2	Sacrificial	InGaAs (lattice matched)	50	nid
1	Sacrificial	AlInAs (lattice matched)	500	\sim 0.5×10^{18}
0	Buffer layer	InP	150	

Table 2.1: III-V SOA epitaxial layer stack

realized using a PDMS stamp. This is solved by including a sacrificial layer under the main functional device layers and undercutting the devices, while they are anchored to the substrate using tethers [6].

The III-V epitaxial stack designed for micro-transfer printing is shown in Table 2.1.

The functional device layers include a 200 nm thick highly-doped p-InGaAs contact layer. The p-cladding layer prevents the optical mode from overlapping with the highly-doped p-contact layer is 1500 nm thick. After the p-cladding, a thin InGaAsP layer is used to act as an etch-stop layer. The active region consists of 6 quantum wells (QWs) and 7 barriers of 7.5 nm and 10 nm, respectively. The separate confinement heterostructure (SCH) layers to confine photons are 75 nm thick. The transition layers are 40 nm thick. The n-InP layer for n-contacts is 260 nm thick. It also acts as a spacer layer between the active region and the silicon waveguide and

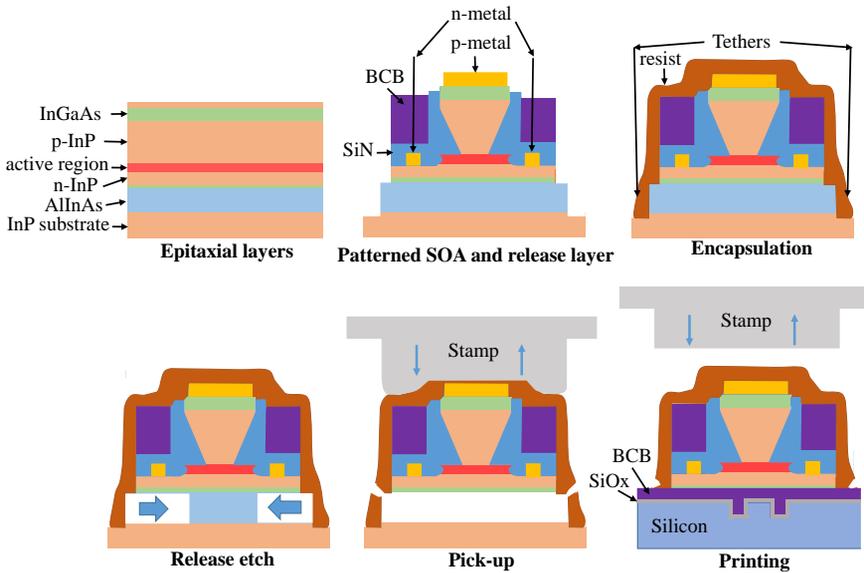


Figure 2.3: Schematic illustrating the micro-transfer printing process of processed SOA coupons.

changing its thickness can significantly change the optical confinement in the active region.

The release layers that are part of micro-transfer-printing process are Al InAs and InGaAs. The AlInAs layer is 500 nm thick and will be under-etched to release the devices together with the InGaAs. AlInAs is chosen because it allows fast, isotropic under-etching using FeCl_3 , with good selectivity to InP. 50 nm InGaAs is used to improve the quality of the epitaxial layer stack grown on top of the sacrificial layer. Next, a micro-transfer-printing process flow is developed using the aforementioned epitaxial stack.

The epitaxial stack and the processing steps to micro-transfer print patterned SOA coupons are illustrated in Fig. 2.3. The III-V SOA is patterned on the InP wafer. This patterning involves the formation of the SOA mesa, patterning of the QWs, contact-metal deposition, planarization using DVS-BCB and etch-back of the DVS-BCB and SiN planarization and the patterning of the coupon boundary. After the formation of coupons, the micro-transfer-printing related processing begins. The processing of the SOA will be discussed in detail in the later chapters. In the next section, the process related to micro-transfer printing is discussed in detail.

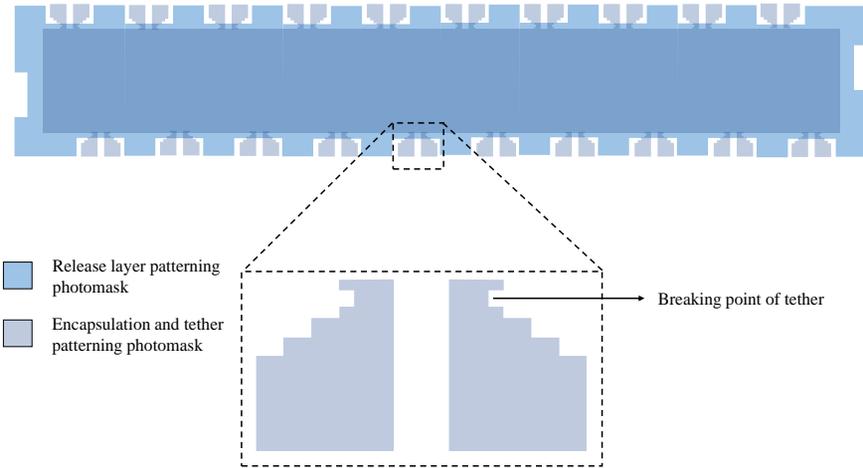


Figure 2.4: Schematic illustrating the photomask used to pattern the release layer and to encapsulate the device. The zoom-in schematic of the tether design is also depicted.

2.3.1 Micro-transfer-printing process

After patterning of the SOA coupon, the release layer has to be patterned. The photomask used to pattern the release layer is shown in Fig. 2.4. The patterning of the release layer should allow the tethers to be anchored to the substrate. And, while the device is encapsulated by the resist, the release layer should still be exposed to the etchant. This is done by making rectangular teeth on the side as shown in Fig. 2.4.

To pattern the release layer, a positive photoresist with $3.5 \mu\text{m}$ thickness is utilized. Standard i-line optical lithography exposure defines the pattern in the photoresist. Following the lithography, the InGaAs/AlInAs release layer is etched in a 1:1:20 $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ solution at room temperature. The etching stops on the InP substrate and it takes about 2 min and 30 s to etch a 500 nm thick AlInAs release layer and 50 nm InGaAs. When the InP substrate is exposed, dry etching in ICP is used to etch 400 nm into the substrate. This improves the adhesion of resist to the substrate and on this surface the tethers will be anchored to the substrate.

The photoresist tethers should have good adhesion with the substrate, implying that the InP substrate should be cleaned and de-oxidized. For this purpose, the sample is dipped in 1:1 $\text{HCl}:\text{H}_2\text{O}$ for 15 s. This etches 40 nm of InP substrate and results in a cleaner surface. The photoresist is removed with Acetone and the sample is cleaned with Isopropanol (IPA) and, immediately, another layer of photoresist is spin-coated on the surface for another

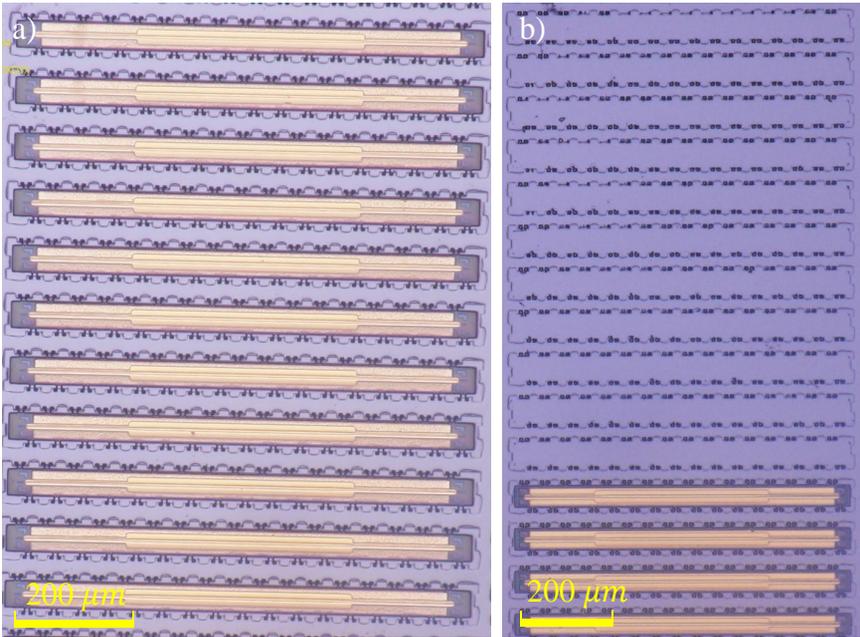


Figure 2.5: a) Microscope image of the released SOA coupons, b) Microscope image of the sample after coupons have been picked-up.

lithography step. For encapsulation and tether formation, $3.5 \mu\text{m}$ thick positive photoresist is used. This photoresist is a good choice since it is thick enough to encapsulate the SOAs and its resolution is sufficient to pattern the tethers. Again, standard i-line optical lithography defines the tether patterns, as shown in Fig. 2.4. The sample is now ready for the release.

A $50 \text{ mg}:100 \text{ ml FeCl}_3:\text{H}_2\text{O}$ solution is prepared and cooled down to 5°C . At lower temperatures, the solution provides better etch selectivity between the release layer and n-InP. It takes about 45 mins to etch a $40 \mu\text{m}$ wide SOA coupon. The released sample is immersed in DI-water to wash down the FeCl_3 and then left to dry in a wet-bench with a fume-exhaust. Figure 2.5 shows the microscope image of the released coupons and the sample after coupons have been picked up by sticky tape. It can be seen that as tethers break on pick-up, the feet of the tethers are still attached to the substrate. These coupons are now ready to be picked-up and printed by the micro-transfer-printing tool.

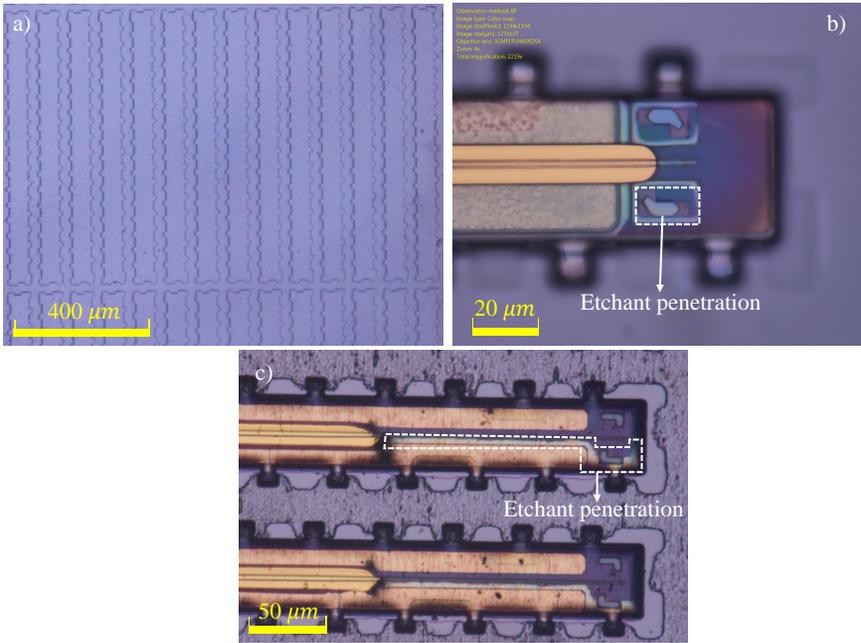


Figure 2.6: (a) Microscope image of a failed release process, the coupons detached from the substrate. b) and c) Microscope image depicting the effects of FeCl_3 penetration in the SOA coupons.

2.3.2 Processing issues and fixes

The processing steps described in the previous section have failed several times during the process development. Several issues have been identified and solved. One of the major issues was the adhesion of the photoresist tethers to the InP substrate. Multiple times during the cleaning process after the release etch coupons detached from the substrate as shown in Fig. 2.6. To identify the cause of failure, several different possible solutions were tried on test samples. It was identified that post-baking of the photoresist can cause it to dry and swell which increases the chances of delamination. Moreover, it was also identified that before spin-coating the photoresist for tether patterning, the sample should be dipped in diluted HCl to expose a clean layer of InP and no oxidizing process should be carried out after the cleaning in HCl, such as a soft resist removal recipe in RIE which uses O_2 and can oxidize InP. The hypothesis is that the native oxide layer on InP gets etched in FeCl_3 and, hence, can cause detachment of the tethers.

In order to make the release process more robust, the patterned device layers should be passivated with SiN and DVS-BCB. This prevents the penetration

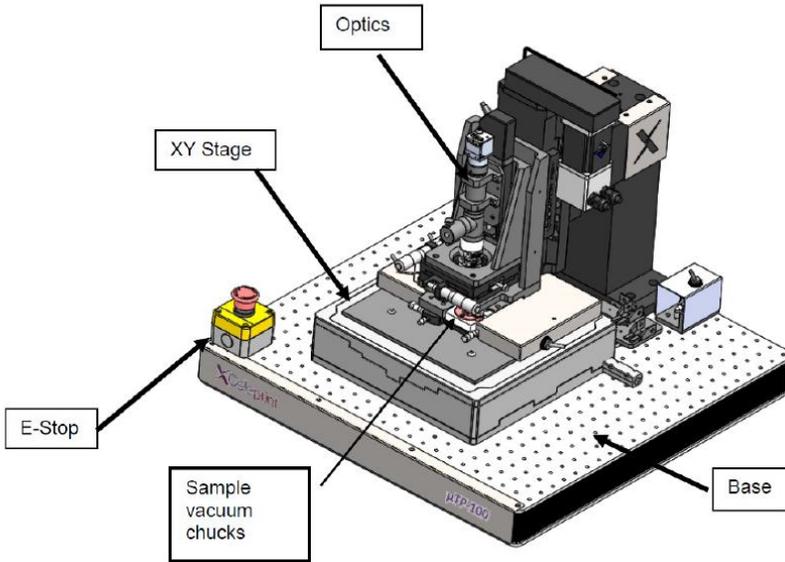


Figure 2.7: Schematic of the μ TP-100 lab scale printer.

of FeCl_3 in the device layers. Especially, when the release layer in the epitaxial growth is pure InGaAs, it becomes more critical as it requires 7-8 hours of release etching time. The effect of etchant penetration in the device layers can be seen in Fig. 2.6(b)(c). The SOA process flow in which the device layers are fully encapsulated with SiN is more robust. Therefore, using SiN tethers instead of photoresist tethers is also an option. In this section, we discussed some of the major problems encountered in the process development. Next, we will elaborate more on the micro-transfer-printing tool, its limitations and solutions for III-V-on-Si heterogeneous integration of SOA coupons on silicon-on-insulator (SOI).

2.4 Micro-transfer printing tool

In this work, a μ TP-100 lab scale printer (X-Celeprint) is used. The schematic of the μ TP-100 is shown in Fig. 2.7. The optics and translation stage is mounted on a base. The stage has 4 vacuum chucks. These can hold 2 inch substrates. However, other tools handling larger substrates are also commercially available.

The two chucks at the front hold the target and source substrate. They can be rotated through a micro-meter screw to rotationally align the samples.

The manual alignment through screws is a tedious process and it is one of the major draw-backs of the μ TP-100 lab scale printer. Additionally, one of the two chucks at the back is mounted with double-sided sticky tape and is used to clean the stamp after each print cycle.

The translation stage can move horizontally, vertically and diagonally. The optics includes a camera and interchangeable 5x and 10x objective lenses. It is used to focus on the coupons and samples, and its main function is to capture images to enable pattern recognition of alignment markers on the source and target. Under the optics, a mount holds the glass plate which carries the stamp. The glass plate is placed upside down and held by a vacuum chuck. The head and the camera can move independently in the z-direction. The camera is moved vertically to set the focus, whereas, the head moves the stamp closer or further away from the source or target in the z-direction.

A general transfer printing work flow includes the following: The stamp with an appropriate post size is loaded on a glass plate. It is then flipped and fixed onto the vacuum chuck under the head. The source and target samples are loaded into the tool. The stage is then moved manually to visualize the source. The optics focus setting and head position setting are saved for pick-up in the software. A similar operation is performed for the target sample for printing. The coupon(s) is (are) then picked up and the camera and COGNEX VisionPro software [7] is used to auto-align the coupon by pattern recognition of the alignment markers. After the alignment, the coupons are printed. The stamp is then cleaned by touching it on the cleaning pad. This whole process cycle can be performed manually and can also be automated.

The tool is specified to provide an alignment accuracy of $\pm 1.5 \mu\text{m}$ (3σ) [1]. This is limited by the magnification and resolution of the optics in the transfer-printing-tool. The aforementioned alignment tolerance is considerably poor in terms of integrating processed SOAs on Si waveguide circuits. Typically, adiabatic tapers couple light in III-V-on-Si heterogeneously integrated devices. Standard tapers structures used in wafer bonded III-V-on-Si devices have few hundred nanometer of alignment tolerance [8], which is not sufficient to develop high-performance III-V-on-Si transfer-printed devices.

In the next section, we will discuss the design of an alignment-tolerant adiabatic taper that significantly improves the alignment accuracy and enables the integration of SOAs using micro-transfer printing.

2.5 Adiabatic alignment-tolerant taper design

The alignment-tolerant adiabatic taper should be able to work within the alignment tolerance of state-of-the-art micro-transfer-printing tools. It should have a reasonable footprint and should be manufacturable. The aforementioned constraints were kept in mind while designing the adiabatic taper.

2.5.1 400 nm thick Si with 180 nm etch-depth

The III-V epitaxial stack described in Table 2.1 is used and a 400 nm thick Si waveguide layer with 180 nm etch depth is assumed. The adiabatic taper is designed using the formalism discussed in [9]. It is given that an adiabatic taper designed to follow Eq. (2.5) can transform the mode from one waveguide into the other waveguide with a lost power fraction less than ϵ .

$$\gamma = \tan[\arcsin(2\epsilon^{\frac{1}{2}} \int_{z_0}^z \kappa(z') dz')] \quad (2.5)$$

where $\gamma \equiv \frac{\beta_2 - \beta_1}{2\kappa}$. $\beta_2 - \beta_1$ is the propagation constant mismatch between the individual uncoupled waveguide modes, ϵ is the fraction of power in the unwanted mode, z are the points along the length of the taper and $z = z_0$ is the phase matching point. κ is the coupling strength between the two waveguide modes and is defined as

$$\begin{aligned} \kappa_{mp} &= \frac{k_0^2}{2\beta} \int \int_{-\infty}^{+\infty} (n'^2 - n_p^2) F_m F_p^* dx dy \\ \kappa_{pm} &= \frac{k_0^2}{2\beta} \int \int_{-\infty}^{+\infty} (n'^2 - n_m^2) F_p F_m^* dx dy \\ \kappa &= \sqrt{\kappa_{mp} \kappa_{pm}} \end{aligned} \quad (2.6)$$

where F_m and F_p are the normalized eigenmodes of each uncoupled waveguide and where n' is the refractive index profile of the coupled waveguide system, n_p and n_m are the refractive index profiles of the uncoupled waveguides, k_0 is the free-space propagation constant and β is the propagation constant of the supermode. F_m and F_p must be normalized such that $\int \int_{-\infty}^{+\infty} |F_{m,p}(x, y)|^2 dx dy = 1$. Equation (2.5) gives us the γ distribution along the length of the III-V and Si adiabatic taper structure, assumed to be along the z -axis. It can be rewritten by assuming κ to be linearly varying between two consecutive points along z and making z the subject of the expression

$$z_N = \frac{\sin(\arctan(\gamma_N))}{\epsilon^{\frac{1}{2}} (\kappa_{N-1} + \kappa_N)} - \frac{2}{\kappa_{N-1} + \kappa_N} \sum_{i=0}^{N-1} A_i + z_{N-1} \quad (2.7)$$

where $z = z_N$ is a point N along the length of the taper, $A_i = \frac{1}{2}(\kappa_{i-1} + \kappa_i)(z_i - z_{i-1})$ and γ_N is the value of γ at $z = z_N$. Equation (2.7) gives the location z along the length of the taper for a given κ and γ value which are related to the width of III-V and Si waveguides in a coupled waveguide system.

In order to design the taper structure a map of κ and γ is calculated, using the Lumerical Mode waveguide simulator [10], for all possible width combinations of III-V and Si waveguide, assuming a lateral misalignment of $1 \mu\text{m}$ as the worst case. A DVS-BCB bonding layer thickness of 60 nm is assumed in the simulation. Equation (2.6) together with the eigenmode solver is used to calculate κ . Similarly, the γ and β values are also computed with the eigenmode solver. The maps of κ and γ for various III-V waveguide and Si waveguide widths are illustrated in Fig. 2.8. To completely transform an optical mode confined in the Si waveguide to an optical mode confined in the III-V waveguide, γ should follow a trajectory from negative to positive values crossing the zero line on the map. The zero line indicates the III-V and Si width combinations at which the optical modes in both waveguides are phase matched. It can be seen from the optical mode profiles in the inset of the Fig. 2.8, when $\gamma = -10$ that the light is confined in the Si waveguide. Alternatively, when $\gamma = 10$ the optical mode is confined in the III-V waveguide. The two different trajectories chosen to design the III-V and Si adiabatic taper (for full coupling and partial coupling) are shown with a white dashed line on the γ and κ map in Fig. 2.8. In one of the two trajectories (full coupling with higher confinement factor), γ varies from -10 to 40 and the optical mode intensity is completely transformed from the Si waveguide to the III-V waveguide and vice versa. In this case the trajectory is chosen such that a high kappa value is obtained in the section where the mode transitions from III-V to Si. The next step in designing the adiabatic taper is to insert the chosen values of the γ and κ trajectory into Eq. (2.7). This will give us their corresponding z location along the length of the adiabatic taper, hence, defining the taper geometry. The value of ϵ is set to be 0.02 and 0.01 for the calculation of the taper geometry in the case of the full coupling design and partial coupling design, respectively. A smaller value of ϵ results in a longer adiabatic taper length. The adiabatic Si and III-V taper should follow one more criterion to avoid power coupling into higher order modes (beyond the two supermodes in the III-V/Si waveguide structure). The local half angle of the Si and III-V taper must satisfy $\theta < \frac{\lambda_0}{2Wn_{eff}}$ [11]. This means that the tapering should be slower than the diffraction of the fundamental mode of each waveguide. The taper geometry calculated from Eq. (2.7) violates this criterion at the end of the taper, where the variation of κ along z is rapid and the mode is

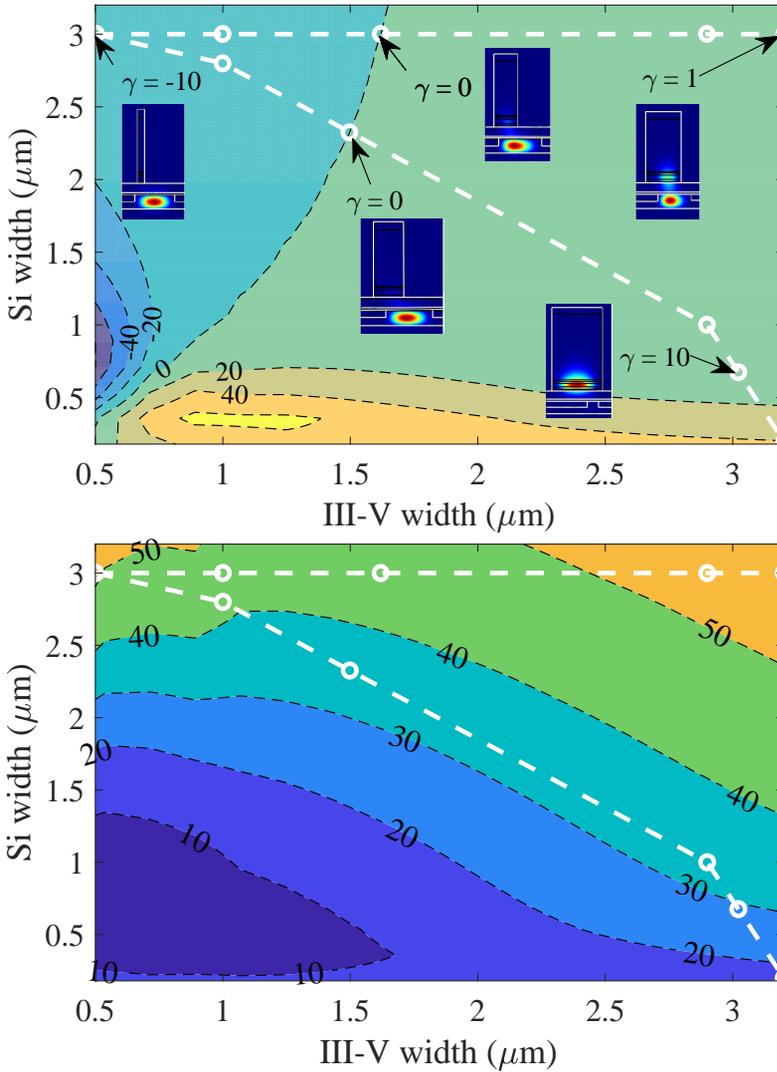


Figure 2.8: (Top) Calculated map of γ for several width combinations of the III-V and Si waveguide. The white dashed lines represent the trajectory of the points chosen to design the adiabatic tapers. The insets are the optical modal profiles found using simulations at $\gamma = -10$ (the optical mode is mostly confined in the Si waveguide), $\gamma = 0$ (this is the phase matching point at which the coupling takes place), $\gamma = 1$ (the optical mode is distributed unevenly in both Si and III-V waveguide), and $\gamma = 10$ (the optical mode is confined in the III-V waveguide), (Bottom) Calculated map of κ in mm^{-1} for several width combinations of the III-V and Si waveguide.

mostly confined in the III-V waveguide. Therefore, the values of z at the end of the III-V and Si adiabatic taper waveguides are adjusted to follow the aforementioned formula. This slows down the tapering and thus prevents the transformation of the fundamental mode into higher order modes.

The taper shapes are illustrated in Fig. 2.9(top). The blue curve and the left vertical axis represents the III-V adiabatic taper for both designs. The initial width of the III-V adiabatic tapers is $0.5 \mu\text{m}$ and the final width is $3.2 \mu\text{m}$. The length of the partial-coupling and full-coupling adiabatic tapers are $210 \mu\text{m}$ and $225 \mu\text{m}$, respectively. The partial-coupling taper is shorter because of the higher κ values. However, to simplify the fabrication and development, the full-coupling adiabatic taper design is used for both partial and full coupling SOAs and only the Si waveguide design is adapted. In the full-coupling design, the Si adiabatic waveguide taper narrows down from $3 \mu\text{m}$ to $0.2 \mu\text{m}$ over $225 \mu\text{m}$ length and for the partial-coupling SOA, it is a $3.0 \mu\text{m}$ waveguide, shown in red curve and on the right vertical axis. The final taper structures are then exported into the Lumerical 3D-EME solver [10] and the power coupling between the Si and III-V waveguides is simulated at $1.55 \mu\text{m}$ wavelength. The coupling efficiency for both designs remain high ($> -0.3 \text{ dB}$) until $1 \mu\text{m}$ misalignment, shown in Fig. 2.9(top). It drops to -2 dB at $1.24 \mu\text{m}$ misalignment and $1.76 \mu\text{m}$ misalignment for the full-coupling design and partial-coupling design, respectively. Moreover, the coupling efficiency of the partial coupling design is higher in the low-misalignment case because of the lower value of ϵ (0.01) chosen to calculate the geometry. It was possible to have the length of the full coupling adiabatic taper below $250 \mu\text{m}$ with ϵ equal to 0.01.

The coupling efficiency of the full-coupling III-V adiabatic taper design is also simulated for different Si waveguide widths. The calculated coupling efficiency is shown in Fig. 2.10. As the width of the waveguide reduces, the lateral misalignment tolerance also degrades. For a $3.0 \mu\text{m}$ Si waveguide, 1 dB excess loss occurs beyond $1.5 \mu\text{m}$ of lateral misalignment. Plus, we find that the full-coupling III-V adiabatic taper works for both full coupling and partial coupling to the III-V active region. In order to simplify and to reduce the number of designs, the III-V adiabatic taper for full coupling is used for both the cases. Although, the alignment tolerance of the adiabatic taper is above $1.0 \mu\text{m}$, due to the drop of confinement factor in the QWs with increasing misalignment the performance of SOAs/lasers will be impacted, shown in Fig. 2.11. Wider Si waveguide exhibit less change in the confinement factor with the misalignment. However, wider waveguides can support multiple transversal modes which leads to multi-mode lasers, if proper mode-filtering is not employed in the designs. Angular misalign-

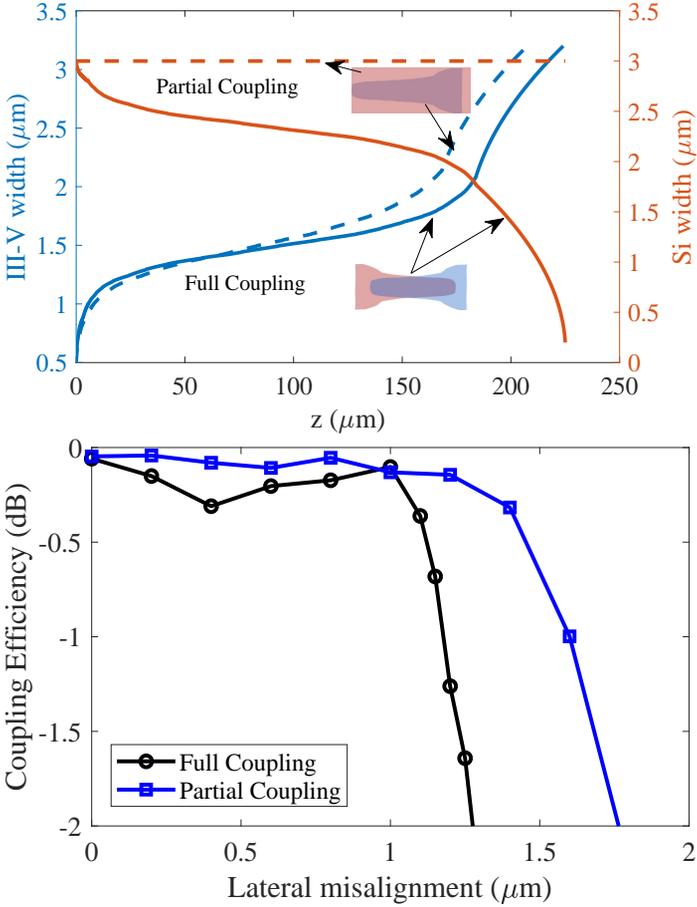


Figure 2.9: (Top) The III-V and Si adiabatic taper width variation along its length. The blue line and the left vertical axis represents the III-V adiabatic taper shape for the partial and full coupling designs. The red line and the right vertical axis represents the Si adiabatic taper shape and Si waveguide width in the case of full coupling and partial coupling, respectively; (Bottom) The simulated coupling efficiency of the adiabatic taper structures for the partial and full-coupling designs versus the lateral misalignment.

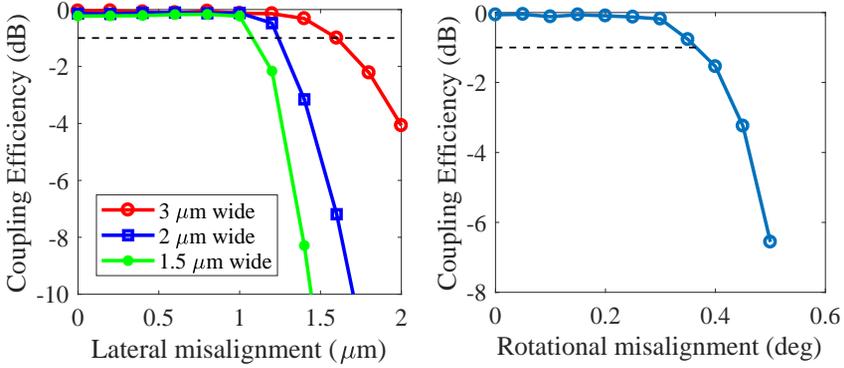


Figure 2.10: (left) Calculated power coupling between full-coupling III-V adiabatic taper design and Si waveguide of width 3.0 μm , 2.0 μm and 1.5 μm , (right) Calculated coupling efficiency against the rotational misalignment between III-V adiabatic taper and Si waveguide.

ment of the III-V adiabatic taper with 3.0 μm Si waveguide is simulated, the result is shown in Fig. 2.10. Simulations indicate that 0.36 degree angular misalignment results in 1 dB excess coupling loss. This is however only relevant for devices with one port, or with two port on the same side of the coupon, as such a large rotational misalignment will lead to a high lateral misalignment on the other side of the coupon. To study the fabrication tolerance of the adiabatic taper, the effect of variation in various parameters is calculated, shown in Fig. 2.12. An offset in the width of the III-V taper or III-V QW width from the designed value doesn't have a major impact on the coupling efficiency. However, a decrease in BCB thickness or the n-InP thickness can significantly degrade the performance. This can be attributed to a significant change in coupling strength between the III-V and Si waveguide.

In this section, we discussed the method used to design an alignment-tolerant adiabatic taper to overcome the misalignment inherent to the micro-transfer-printing tool. This adiabatic taper is designed for a 400 nm thick Si passive platform with 180 nm etch-depth. Additionally, adiabatic tapers are designed using the same methodology for different waveguide cross-sections and will be discussed in the following sections.

2.5.2 Design for imec iSIPP50G platform

The integration of SOAs on complex SiPh platforms such as iSIPP50G is quite critical to develop advanced systems-on-chip. It is possible to integrate SOAs with micro-transfer printing on the iSIPP50G platform by lo-

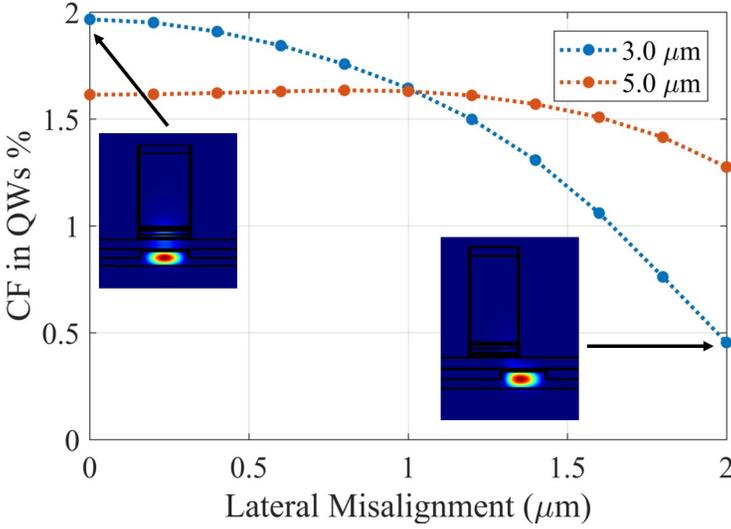


Figure 2.11: The change in confinement factor in QWs with the misalignment variation for 3.0 μm and 5.0 μm Si waveguide width, insets illustrate the mode profile at zero and 2.0 μm misalignment.

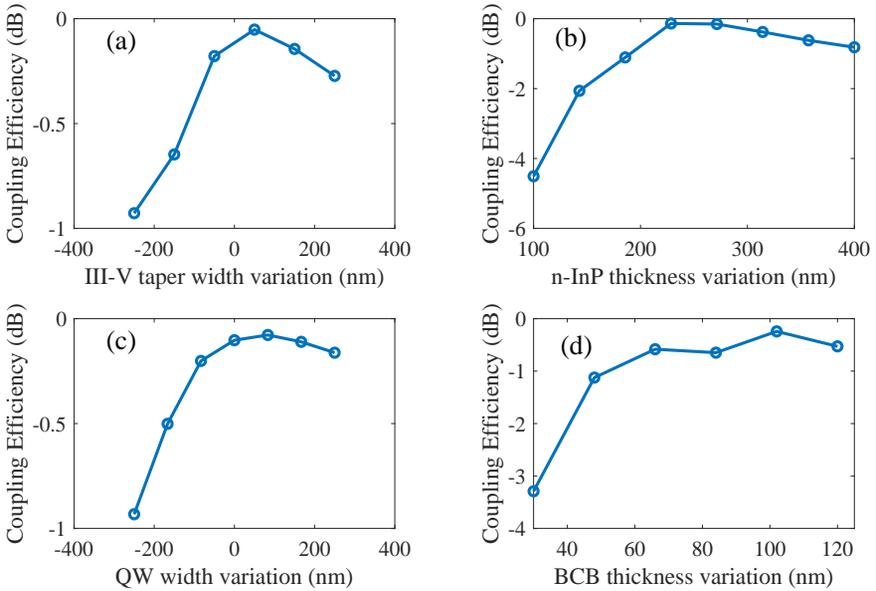


Figure 2.12: (a) Calculated coupling efficiency for variation in a) adiabatic III-V taper width, (b) n-InP thickness, (c) QW width and (d) BCB thickness.

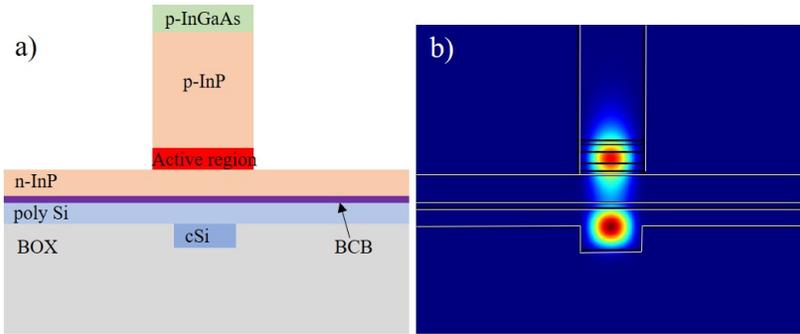


Figure 2.13: Schematic illustration and simulated mode profile of the ISIPP50G waveguide cross-section with integrated SOA.

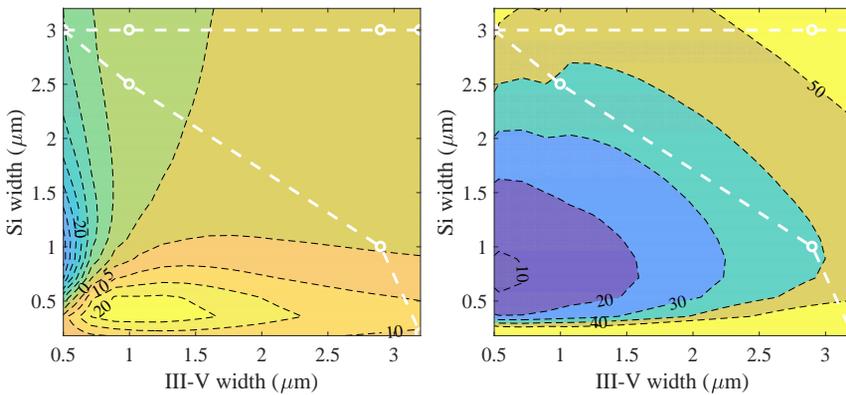


Figure 2.14: Calculated γ (left) and κ map (right) to design the adiabatic taper for the ISIPP50G platform. The white dashed lines represent the selected III-V and Si width combinations for the full-coupling and partial-coupling designs.

cally removing the back-end stack on the top of Si waveguide circuit. The Si waveguide is 220 nm thick and has 160 nm thick poly-silicon on top. The opening process is available as EXPO and is commonly used for grating couplers. Therefore, the SOA integration with micro-transfer printing doesn't require any changes to the iSIPP50G process flow. The resulting waveguide cross-section and the mode profile is shown in Fig. 2.13.

By using the methodology described in the previous section, an alignment-tolerant adiabatic taper is designed. The map of κ and γ is calculated assuming a DVS-BCB layer thickness of 60 nm at a wavelength of 1550 nm, shown in Fig. 2.14. To define the shape of the adiabatic taper, III-V and Si waveguide width combination are selected for both the full coupling and partial coupling to the III-V waveguide. As described in the previ-

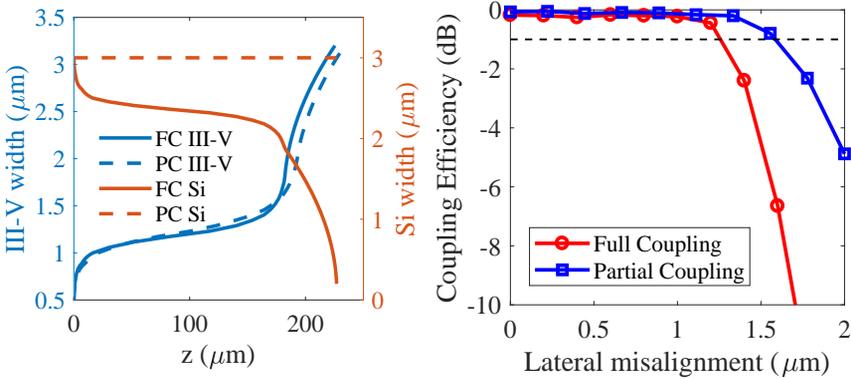


Figure 2.15: (left) Designed shape of the adiabatic alignment tolerant tapers. The full-coupling design and partial-coupling design is represented by the solid curves and the dashed curves, respectively.

ous section, the full coupling design involves inverse tapering of III-V and Si waveguides, whereas, in the partial coupling Si waveguide has a constant width and III-V is only tapered. The shape of the adiabatic tapers is illustrated in Fig. 2.15 for both the full coupling and partial coupling design. In the full-coupling design, the III-V structure tapers from $0.5 \mu\text{m}$ to $3.2 \mu\text{m}$ and the Si taper from $3.0 \mu\text{m}$ width to $0.2 \mu\text{m}$ taper tip.

The partial-coupling design has a $3.0 \mu\text{m}$ Si waveguide and a III-V adiabatic taper. The calculated coupling efficiency against lateral misalignment is shown in Fig. 2.15. Both the tapers have high-coupling efficiency until $1.0 \mu\text{m}$ chosen as the worst case. The full coupling design has 1 dB excess loss at $1.3 \mu\text{m}$ and for the partial coupling design it is $1.5 \mu\text{m}$.

2.6 Conclusion

In this chapter, micro-transfer-printing technology was introduced. We discussed the various properties of the PDMS stamp, particularly, the viscoelastic property and how it plays a role in micro-transfer-printing. The need to release semiconductor devices for micro-transfer printing was also discussed. The fabrication of micro transfer-printing-compatible SOAs was described and the challenges were discussed. It was also highlighted that the alignment accuracy of the micro-transfer-printing tool requires the design of an alignment-tolerant adiabatic taper to efficiently couple between the SOA and the Si waveguide. The methodology behind the design of the alignment-tolerant adiabatic taper was also discussed and alignment tolerance simulations were carried out. The adiabatic taper was designed for a

400 nm thick Si platform and also for the imec iSIPP50G platform. The developed process flow for micro-transfer printing SOAs along with the alignment-tolerant taper structures allows to integrate SOAs using micro-transfer-printing technology. This will be discussed in the next chapter.

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3

Micro-transfer-printed C-band SOAs

In the previous chapter we discussed the micro-transfer-printing technology in detail. We also described the important ingredients that make the micro-transfer-printing of the SOAs possible including the adiabatic alignment-tolerant taper design and the developed process flow. In this chapter, we will use the knowledge developed from the previous chapter to demonstrate semiconductor optical amplifiers micro-transfer-printed on Si photonic integrated circuits. This chapter is based on [1].

3.1 Introduction

Photonic Integrated Circuits (PICs) have become a commercial reality in a number of markets, especially in telecom and datacom [2]. PICs enable complex optical and opto-electronic functions on a very compact footprint with high reliability [3–5]. And because of wafer-scale manufacturing, the cost of a PIC can be significantly lower than with conventional technologies (relying on bulk optical or other assembly platforms) for the same function. Silicon photonics is the field that takes advantage of more than 50 years of massive investment in silicon technology for electronic ICs. It leverages the vast know-how of the CMOS world to develop PICs in the technologies of existing CMOS fabs [6]. It is a relatively young field: research activities geared up less than 20 years ago and widespread industrial interest less than 10 years ago. Nevertheless, the field of silicon photonics has been growing

at an amazing rate, both scientifically and industrially [7–9]. Today more than 15 CMOS fabs (industrial fabs or semi-industrial R&D fabs) around the world have developed a mature process flow for silicon photonics [6]. Some of them manufacture products that are competitive in the market today [8, 9].

While state-of-the-art silicon photonic integration platforms are being developed by various companies and research institutes, having integrated light sources at wafer level is still a stumble block. This limits the functionalities that can be implemented on a single chip. However, several approaches for wafer-level light source integration are being pursued, each with their own advantages and drawbacks, and with different technology readiness levels (TRL). There is a consensus that monolithically integrated Group IV lasers are still far from being practical, and that III-V semiconductor materials and devices are needed. Currently, the method that has the highest maturity-pioneered by Luxtera-is the use of a micro-packaged laser (coined a LaMP), comprising a III-V laser diode on a micro-optical bench with a ball lens, isolator and mirror to focus the light on a grating coupler on the Si PIC [10]. While this approach has several advantages (mature InP technology, wafer-level assembly, packaging, test and burn-in), the complexity of the LaMP itself and its sequential active alignment on the silicon photonic wafer make it an expensive solution. Moreover, the use of a grating coupler as an optical interfacing limits the coupling efficiency and bandwidth. Also, waveguide-in/waveguide-out components such as semiconductor optical amplifiers (SOAs) are quite difficult to realize this way, and these are key components in advanced PICs. Therefore, more intimate integration approaches are being pursued, ranging from flip-chip integration of III-V opto-electronic devices over III-V die-to-wafer/wafer-to-wafer bonding to hetero-epitaxial growth. Front-end hetero-epitaxial growth of III-V semiconductors represents the ultimate path to integrate light sources on silicon photonics and proof-of-concept devices have been demonstrated [11], but many technological hurdles need to be overcome before this becomes a viable technology. In the case of flip-chip integration mature III-V technology can be used and with efficient optical coupling devices such as semiconductor optical amplifiers (SOAs) can be realized. Testing the devices on the source wafer prior to integration is possible, but the sequential assembly (using active or passive alignment) can be a bottleneck and double-sided coupling is difficult for III-V chips with a cleaving tolerance of several micrometer.

The die-to-wafer bonding approach has the advantage of high-throughput integration: with die-to-wafer bonding unstructured III-V dies are bonded epi-side down to a silicon photonic wafer. The unpatterned III-V does not

need accurate alignment, making this a low-cost approach. After bonding and III-V substrate removal the III-V epitaxial layers can be processed on wafer-scale, lithographically aligned to the underlying silicon waveguides, thus removing the need for active alignment. While this enables dense integration of efficient light sources and optical amplifiers, the silicon photonics back-end flow needs to be modified for the III-V integration [12–14]. Therefore there is a need for an alternative approach that combines the advantages of flip-chip integration (processing of III-V devices on the III-V source wafer, pre-testing) and die-to-wafer bonding (high throughput integration), straightforward integration of waveguide-in/waveguide-out devices such as SOA).

In this chapter, we demonstrate the first III-V-on-Si SOAs integrated through micro-transfer-printing. We discuss two distinct SOA designs with different confinement factor in the multiple-quantum-well stack (MQW). We also discuss the fabrication process including patterning of the SOA on the InP substrate, release, micro-transfer printing and post-processing. we will use the alignment-tolerant adiabatic taper designed in the previous chapter. We report on the performance of the SOAs and discuss the future prospects. This work substantiates the micro-transfer-printing technique for heterogeneous integration of III-V devices on Si photonics platforms enabling the creation of more complex and powerful chip-scale photonic systems.

3.2 Design of the III-V-on-Si SOA

The SOA epitaxial stack has a 200 nm highly doped p-InGaAs contact layer, a 1.5 μm p-InP cladding, a 25 nm etch stop InGaAsP layer, a pair of 40 nm AlGaInAs transition layers separating InP from SCH layers, a pair of 75 nm AlGaInAs SCH layers, an active region with 6 AlGaInAs QWs sandwiched between AlGaInAs barrier layers, a 200 nm n-InP contact layer with 60 nm intrinsic InP layer underneath and a 50 nm/500 nm InGaAs/AlInAs release layer grown on the InP substrate [15].

As discussed in the previous section, we report two III-V-on-Si SOA designs that have different Si waveguide width in the gain section of the SOA. This allows to vary the confinement of the optical mode in the quantum wells and hence tune the small-signal gain and output saturation power. The Si waveguide layer is 400 nm thick and is etched 180 nm. The buried oxide (BOX) layer is 2 μm thick underneath the Si waveguide layer. Both SOA designs, full-coupling (higher optical confinement in the QWs) and partial coupling (lower optical confinement in the QWs), are illustrated in Fig. 3.1. In the full-coupling case, the light couples from the Si waveguide

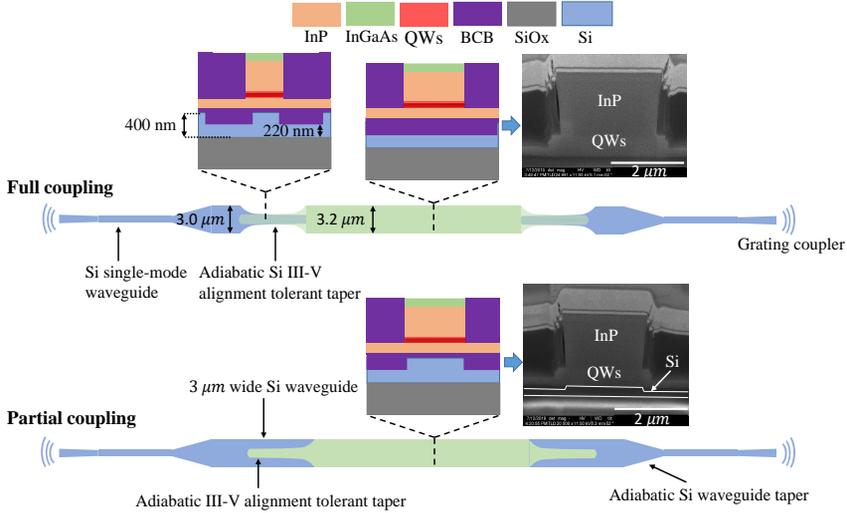


Figure 3.1: Schematics and FIB cross-sections illustrating the design of the full-coupling and partial-coupling III-V-on-Si SOAs.

to the III-V waveguide using an alignment-tolerant Si/III-V adiabatic taper structure and there is no Si waveguide underneath the III-V active region as shown by the cross-sections. In contrast, the partial coupling design uses the same adiabatic III-V alignment-tolerant taper to partially couple the light from the Si waveguide to the III-V/Si waveguide section of the SOA. A focussed ion beam (FIB) cross-section in the gain section of the SOA for both types is also shown in Fig. 3.1. We are using the same III-V SOA device (coupon) on two different Si waveguide designs (based on full coupling and partial coupling to the III-V device layer). These different Si waveguide designs tune the confinement factor in the active region of the SOA. In the full-coupling SOA design, there is no Si waveguide underneath the III-V waveguide gain section and light fully couples into the III-V waveguide. The partial-coupling design has a 3- μm wide Si waveguide underneath and light is only partially coupled to the III-V active region of the SOA. The taper is designed to overcome the coupling losses due to the lateral misalignment, inherent to the transfer printing tool, between the prefabricated III-V SOA and the Si waveguide. Outside the III-V/Si SOA, the wide Si waveguide is adiabatically tapered to a single mode waveguide. Focusing grating couplers are used for fiber interfacing on both sides of the SOA.

3.3 Fabrication

The fabrication of heterogeneously integrated III-V-on-Si devices using micro-transfer printing is a complicated process. It requires successful processing steps to be carried out diligently. The complete process can be divided into four major headings: fabrication of SOAs on the InP based epitaxial wafer/die, patterning of structures in SOI (which in the case of SOAs includes waveguides, grating couplers, and alignment markers), micro-transfer printing and, finally, processing steps on SOI for electrical contacting. We will discuss them in the following sections chronologically. Moreover, instead of processing complete wafers, smaller dies of various sizes have been processed to avoid wastage of material in the case of processing failure. In this PhD project, all the aforementioned processing steps have been performed using Ghent University clean room facilities.

3.3.1 Lithography mask design for processing on InP die

A successful process run starts with a well-thought-through lithography mask design. Several lithography mask layers are required to realize an SOA. These mask layers include structures to pattern SOAs, alignment markers for overlay of subsequent lithographic steps, and a number of test structures to assess the quality of each step during processing. Figure 3.2 shows the schematic of the photomask for the SOA processing on the InP die. It is $11 \times 14 \text{ mm}^2$ in size.

There are four different designs of SOAs in the photomask. These designs have four different lengths $700 \mu\text{m}$, $900 \mu\text{m}$, 1.1 mm and 1.4 mm . Each design is arranged in a 50×5 formation. Therefore, in total there are 250 SOAs of each length. The gap between adjacent coupons in both directions is $24 \mu\text{m}$. The coupons themselves are $45 \mu\text{m}$ wide. The alignment markers are crosses and vernier structures. The latter are used for fine alignment of consecutive lithographic layers. In particular, it is useful to place multiple copies of similar markers, in case if some of them are no longer usable during the complex fabrication process. The test structures on the right-hand side include rectangular boxes (e.g. to measure etch progress), TLM structures to measure electrical characteristics and fine features to assess development time of the photoresist after exposure.

3.3.2 SOA processing on the III-V source wafer

The SOAs are fabricated on an InP wafer. The epitaxial layer structure is grown by metal-organic vapour-phase epitaxy (MOVPE). The InP die of $15 \times 19 \text{ mm}^2$ is first cleaved. The detailed process flow is depicted in

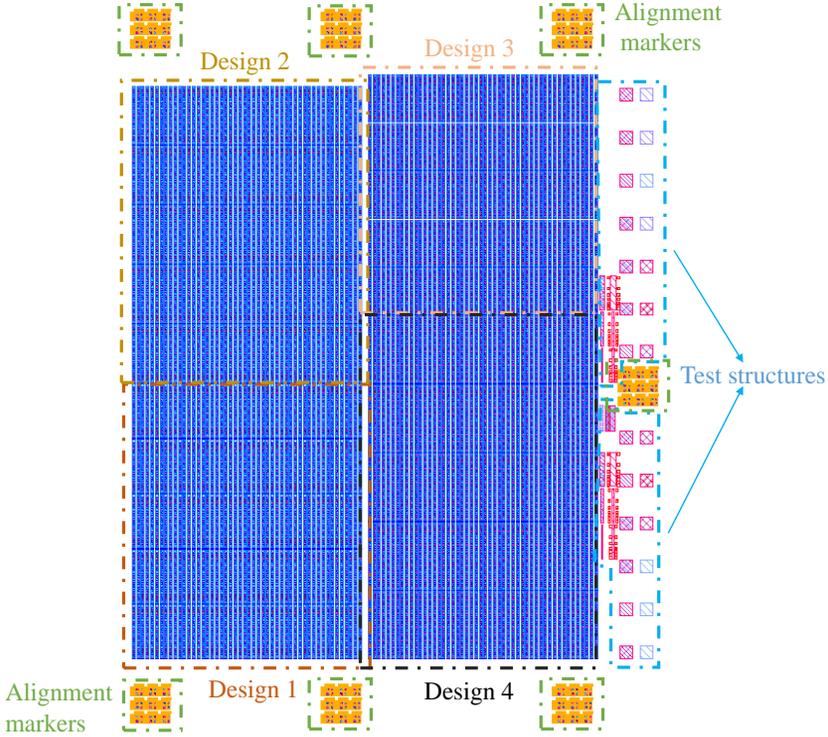


Figure 3.2: Schematic of a complete photomask for SOA processing on an InP die.

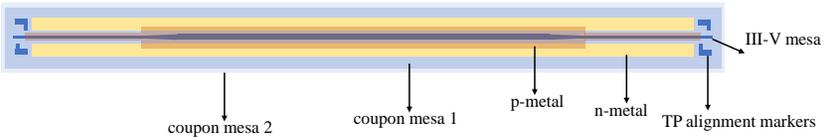


Figure 3.3: Schematic of different layers for SOA processing on InP.

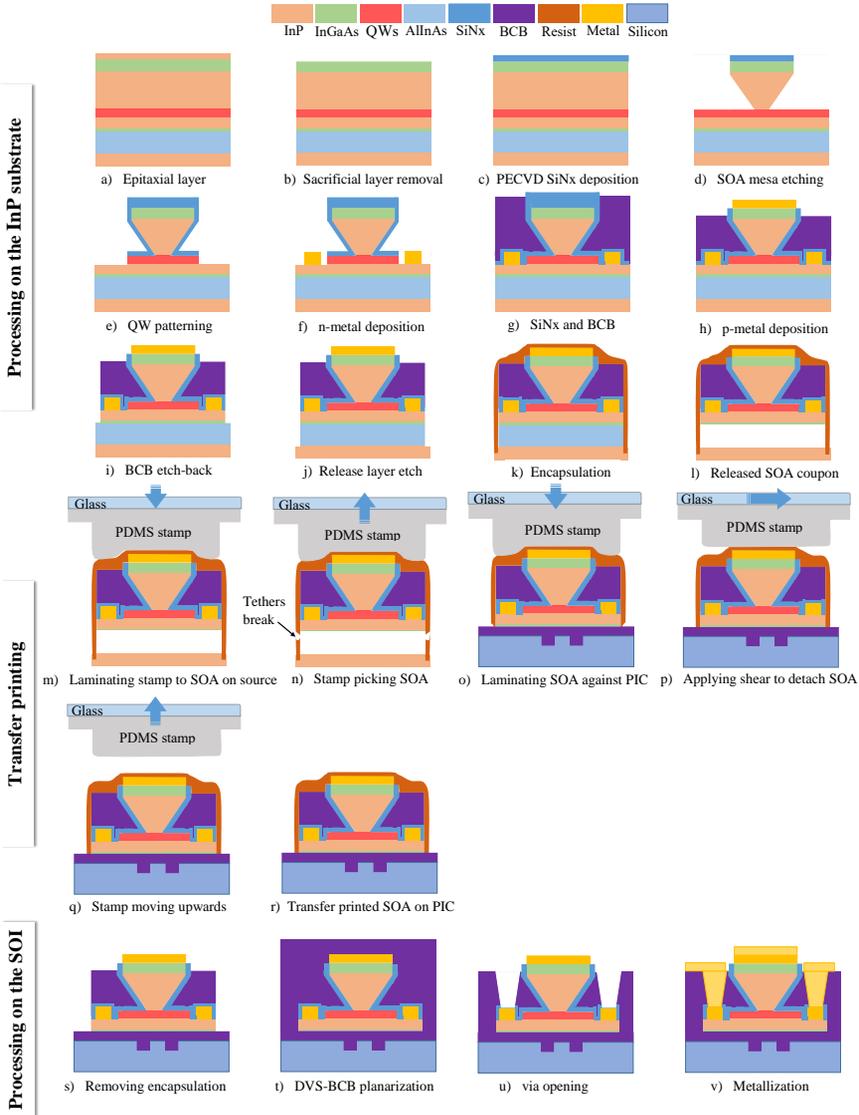


Figure 3.4: The complete process flow of SOA device fabrication which includes patterning on the source InP substrate, micro-transfer-printing, and final processing steps on the SOI target substrate.

Fig. 3.4 and various lithographic layers for the fabrication of the SOA are shown in Fig. 3.3. There are five different lithography steps for patterning the III-V mesa along with alignment markers for micro-transfer printing, n-metal deposition, p-metal deposition, coupon mesa 1 and coupon mesa 2. The fabrication process starts by removing the 100 nm InP sacrificial layer with pure HCl (Fig. 3.4(b)). A PECVD hard mask of 10 nm SiO₂ and 320 nm SiN is then deposited (Fig. 3.4(c)). The hard mask is then patterned using i-line UV lithography to define the SOA mesa and III-V adiabatic taper structures. The photomask is centered on the cleaved die. This leaves some gap between the structures and the edge bead produced during various lithography processing steps. ICP etching is used to etch the InGaAs and p-InP cladding layer. The dry etch process stops when the active region is exposed. Subsequently, p-InP is anisotropically etched in 1 : 1 HCl: H₂O for less than a minute. This creates an inwards angled side-wall of the p-cladding when the mesa is oriented along the [01 -1] direction (Fig. 3.4(d)). Surface oxides on the active region are removed by dipping in 1 : 1 : 20 H₂SO₄:H₂O₂:H₂O and 1 : 10 BHF:H₂O. Next, a layer of 200 nm SiN_x is deposited at 270 °C to protect the side-walls of the SOA mesa. The SiN_x layer also acts as a hard mask for the patterning of the AlGaInAs QWs. The QWs are partially etched using ICP and partially in 1 : 1 : 20 H₃PO₄:H₂O₂:H₂O (Fig. 3.4(e)) to stop on the n-InP. After the QW etching, Ni/Ge/Au contacts are formed on the n-InP through a lift-off process (Fig. 3.4(f)). The sample is again passivated first with SiN_x and then planarized with DVS-BCB. In the following step DVS-BCB and SiN_x are etched to expose the p-InGaAs contact layer for Ti/Au metal deposition (Fig. 3.4(h)). The coupon boundaries are then formed by etching back the DVS-BCB and InP using a dry-etching process (Fig. 3.4(i)). The exposed release layer is then patterned using 1 : 1 : 20 H₃PO₄:H₂O₂:H₂O (Fig. 3.4(j)). The etching stops at the InP substrate. Afterwards, ICP is used to etch into the substrate so that tethers can anchor to the substrate. At this moment, the sample is also dipped in 1 : 1 HCl: H₂O for few seconds to have a cleaner surface and better adhesion of the tethers to the InP substrate. A thick photoresist of 3.5 μm is spin-coated on the sample and patterned to encapsulate the device and to form tethers that will hold the device after the under-etching of the release layer. An aqueous FeCl₃ solution at 7 °C is used to under-etch the AlInAs release layer. It takes 2 hours to etch a 45 μm wide coupon. The coupons at this point stand on the resist anchors (tethers). These coupons are fabricated in a dense array with a vertical pitch of 90 μm on the InP substrate. The top view of patterned and released coupons is illustrated in Fig. 3.5. The SOA coupons discussed herein are 45 μm wide and 1.4 mm in length.

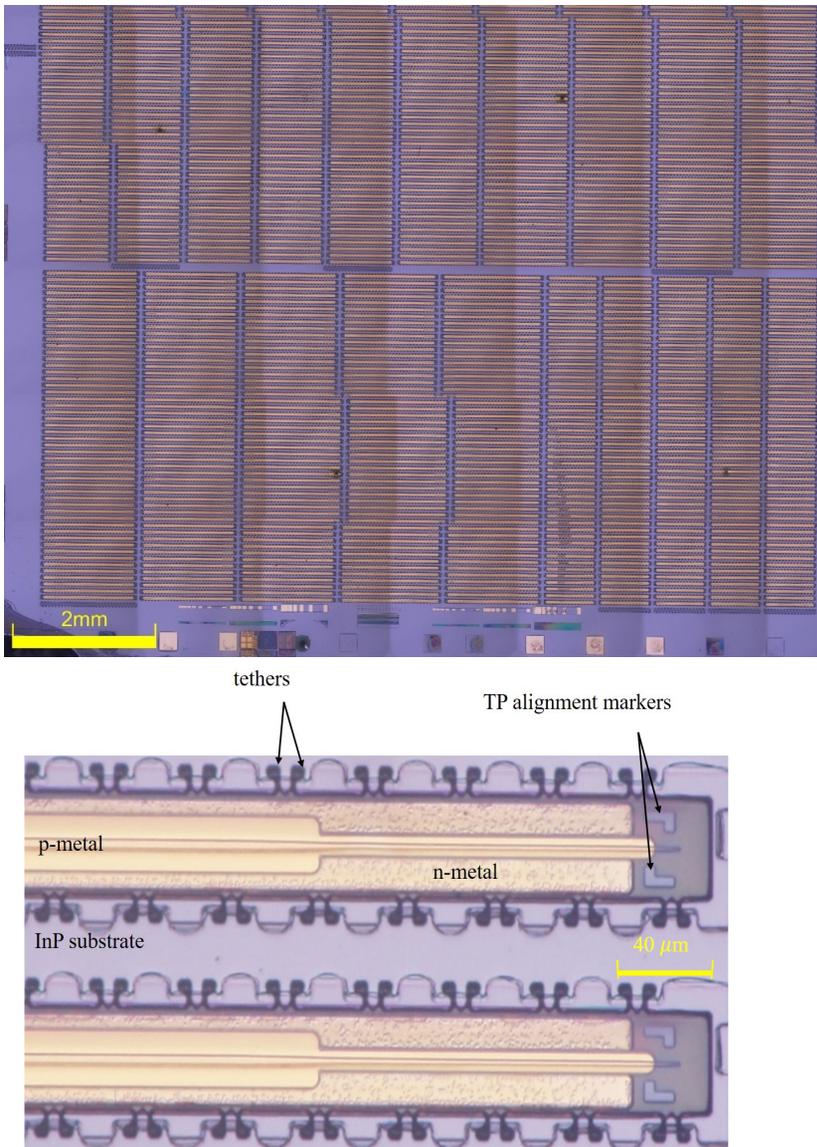


Figure 3.5: (top) Microscope top image of an array of SOA devices patterned and released on the native InP substrate, (bottom) Zoomed-in microscope image of two SOA coupons.

3.3.3 SOI processing

3.3.3.1 e-beam lithography

The Si sample is processed using our in-house Electron-beam (e-beam) lithography setup. E-beam lithography is a great tool for in-house prototyping and testing because of faster turn-around time as compared to multi-project-wafer (MPW) runs offered by various research institutes and foundries.

E-beam lithography allows direct writing of structures when a sample coated with a thin-layer of resist is exposed to a focused electron beam. The electron beam alters the chemical composition of the resist, which makes the exposed part soluble (positive resist) or insoluble (negative resist) in a developer solution. After the development, the pattern in the resist can be transferred to the Si layer underneath with dry-etching.

In our cleanroom, the e-beam lithography system is a Raith-VOYAGER. It can be used to pattern and measure various samples, masks and wafers. The important system features include operation with acceleration voltages up to 50 KV, maximum write field size of 500 μm and automatic system setup (autofocus/autostigmator/automatic stage adjustment with mark recognition/automatic write-field alignment). The system can be used to pattern complex structures on masks of up to 7-inch diameter and wafers of up to 8-inch diameter, using direct-write procedures with ultra-high resolution in the nanometer range [16]. A more detailed description of e-beam parameters can be found in the PhD thesis of Sulakshna Kumari [17].

It is important to mention that the aforementioned e-beam system has two different writing modes, conventional writing and Fixed Beam Moving Stage (FBMS) writing. In conventional e-beam writing, the stage remains stationary and the electron beam is deflected. Therefore, the size of the writing field depends on the maximum deflection angle of the e-beam. The e-beam system in our cleanroom has a maximum write field of $500 \times 500 \mu\text{m}^2$. Beyond each write field, the stage has to be moved which can produce alignment inaccuracies at the boundary of the writing field. Therefore, longer structures that occupy more than one write field are susceptible to misalignment at the boundary of each write field, often called stitching errors. The stitching errors result in higher optical waveguide losses and can produce reflections. Hence, it is critical to reduce the number of stitching errors to avoid performance degradation. Fortunately, Raith-Voyager provides a solution for writing long waveguides with a novel continuous writing mode, called Fixed Beam Moving Stage (FBMS).

The FBMS writing mode allows exposing smooth and stitching-error-free paths of arbitrary curvature of any length, even up to several cm long, by

maintaining the beam at a fixed position and then continuously moving the stage (and thus the sample) with respect to the beam [16]. Therefore, it is ideal to write longer waveguides. A detail description of the FBMS writing method can be found in the PhD thesis of Sulakshna Kumari. Nonetheless, a combination of conventional writing and FBMS writing is used to pattern the Si waveguide for the SOA. The waveguide underneath the gain section and the adiabatic tapers are written with FBMS, since the total length is longer than the maximum write field length and we want to avoid stitching errors. The grating couplers, lithography alignment markers and micro-transfer-printing alignment markers are written with the conventional writing mode.

3.3.3.2 Patterning of SOI

The definition of the waveguides in the SOI is a single-etch-step process. First, an SOI sample is cleaved from a 400 nm thick SOI wafer depending on the size of the lithography mask to be patterned. The protective photoresist layer on top the sample is removed and AR-P 6200.09 (CSAR 62) resist is spin coated. CSAR 62 is a new positive -ebeam resist with excellent structural resolution and comparable broad process windows to other resists. CSAR 62 has superior performance in terms of contrast and sensitivity when developed in AR 600-546. It is an attractive and cheaper alternative to ZEP. AR-P 6200.09 is spin coated at 2000 rpm for 40 s. The sample is then baked at 150 °C for 1 min. Subsequently, a water-soluble conductive polymer Electra 92 (AR-PC 5090), which is compatible with CSAR 62 is also spin coated on top of the AR-P 6200.09 layer to reduce the effect of charging. This is particularly important when patterning dielectrics as charge can easily accumulate at a point which defocuses the e-beam and degrades the writing process. Electra 92 is spin coated at 2000 rpm at 60 s and the sample is then baked for 2 min at 90 °C. The sample is now ready to be loaded in the e-beam lithography tool for exposure. After the e-beam exposure, the sample is immersed in DI-water for 30 s to remove the water soluble charge reduction layer and then for 1 min in n-amylacetate. This is followed by 30 s immersion in IPA. At this stage, the pattern on the resist has been formed and can be transferred to Si. We use a dry etching process called Reactive Ion Etching (RIE) in an Advanced Vacuum Vison 320 RIE tool equipped with 13.56 MHz RF excitation and a cooling system to maintain the sample plate temperature at 20 °C. The 180 nm partial etch of the silicon device layer is realized through RIE. A mixture of CF₄, H₂ and SF₆ is used, which is inspired by an in-house developed etching process for silicon nitride and germanium. A power of 210 W, a pressure of 20

mTorr optimized with gas flow parameters (100 sccm for CF_4 , 7 sccm for H_2 and 3 sccm for SF_6) are used. The etch rate is around 50 nm per minute, both for the e-beam resist and the silicon. Note that the actual etch rate can vary strongly with time. In order to measure the etch depth, squares of size $60 \mu\text{m}^2$ are included in the design. The thickness of Si in these squares can be measured using a Filmetrics tool before and after etching. The difference in the thickness indicates the amount of Si etched. Finally, the resist can be removed in the RIE chamber with O_2 plasma. We prepared several test samples and observed them under SEM. We measured the difference in designed and fabricated structures and to compensate for the differences adjustments were made accordingly in the final design. Figure 3.6 shows the SEM images of different components in the SOI design. Figure 3.6(a) and Fig. 3.6(b) shows the DBR and the grating coupler, whereas, Fig. 3.6(c) is the taper tip of the adiabatic taper.

3.3.4 Micro-transfer printing of SOAs

A PDMS stamp with a post of $1400 \times 60 \mu\text{m}^2$ in size is used for printing $1400 \times 50 \mu\text{m}^2$ SOA coupons using an X-Celeprint $\mu\text{TP-100}$ tool. Although a single post stamp was used in this experiment, a multiple post array stamp can print multiple devices at the same time. This is more useful for high throughput integration on wafer-scale. The SOA coupons are printed on a passive Si photonic waveguide circuit. It has a 400 nm thick Si device layer and the waveguides are etched 180 nm deep. The BOX layer is $2 \mu\text{m}$.

The target sample (Si photonic waveguide circuit) is spin-coated with a DVS-BCB:mesitylene 1 : 4 solution at 3000 rpm, followed by a soft bake at 150°C and cooling down to room temperature. After the preparation of the target sample, both the SOA coupon source sample and the SOI target sample are loaded into the micro-transfer-printing tool. The source and

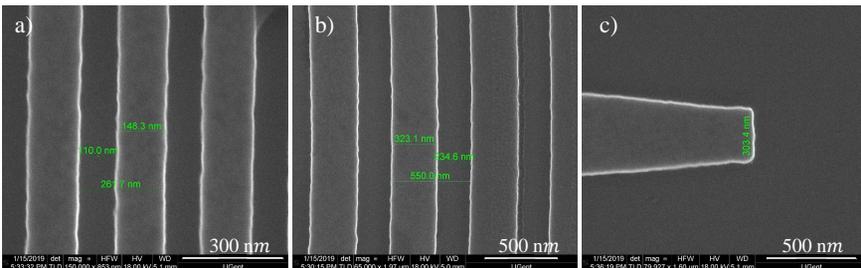


Figure 3.6: a) SEM image of the DBR, b) grating coupler and c) taper tip of the adiabatic taper in Si

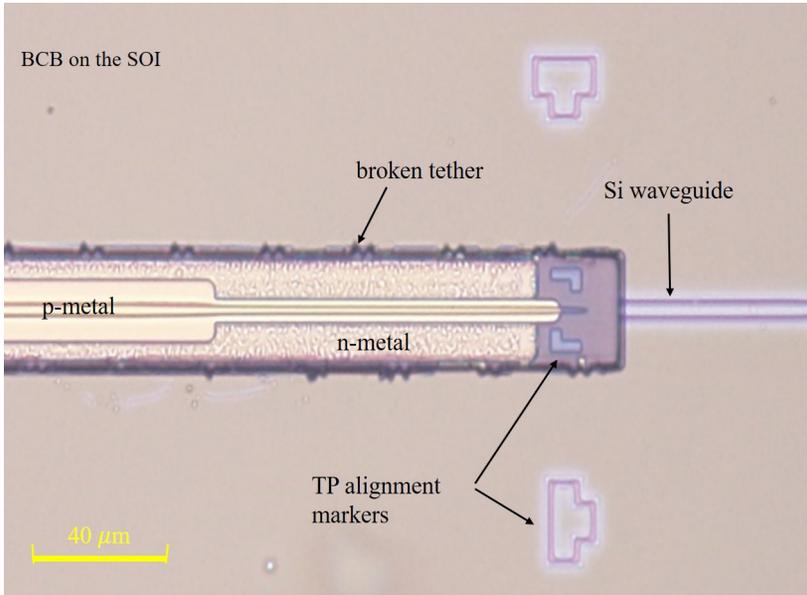


Figure 3.7: Microscope image of a SOA coupon after micro-transfer-printing on SOI.

the target samples are aligned. A good angular alignment is critical for the long SOA devices. The printing process is shown in Fig. 3.4. It starts with laminating the stamp to the released SOA coupon. The stamp then accelerates away from the coupon breaking the tethers at the narrowest point on top of the previously present AlInAs release layer. After the pickup, the COGNEX VisionPro software [18] is used to auto-align the coupon doing pattern recognition on the alignment markers both on the SOA coupon and the target circuit, shown in Fig. 3.7. After the auto-alignment, the stamp is laminated to the target SOI and when in contact, a shear force is applied to the stamp in the x and y direction to detach the SOA coupon from the stamp. The stamp then slowly moves up leaving the SOA coupon on the target site.

3.3.5 Post-processing of the III-V/SOI structures

In order to avoid having to process III-V semiconductor devices on the SOI target wafer, all SOA processing steps were carried out on the III-V source. The post-processing steps are limited to the removal of the encapsulation, planarization and electrical contacting. The processing steps are shown in Fig. 3.4. The first step is to remove the encapsulation resist using a dry

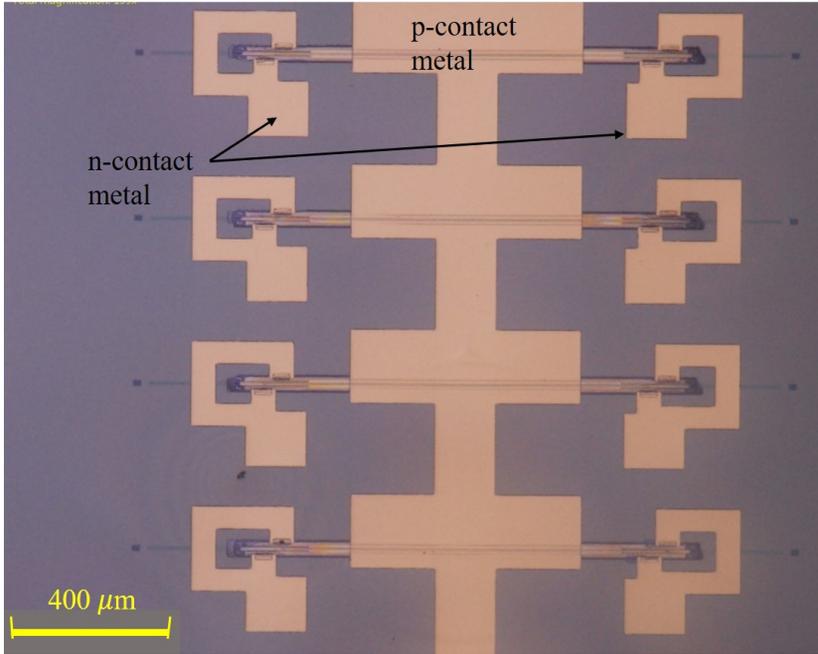


Figure 3.8: Microscope image after contact metal deposition on the SOI.

etch process. After the complete removal, the DVS-BCB bonding layer is fully-cured by ramping the temperature from room temperature to 270 °C and later it is cooled down slowly to room temperature. The coupons are then passivated with a thick layer of DVS-BCB, which is fully cured. This is followed by etching the DVS-BCB and SiN (in case of n-metal) to expose the p-contact metal and n-contact metal. Finally, with a lift-off process a thick layer of Ti/Au is deposited to make electrical contacts to the SOA devices. The final look of the device is shown in Fig. 3.8.

3.4 Device characterization

The III-V-on-Si PIC is placed on a temperature-controlled stage at 20 °C for the measurements. The PIC is optically probed with cleaved standard single mode fibers using a fiber stage. Grating couplers are used to interface with the optical fibers. The grating couplers that couple light into the PIC have a wavelength dependent transmission response. Therefore, it is necessary to characterize grating couplers as a function of wavelength to measure the on-chip gain of the amplifiers accurately. In order to do this,

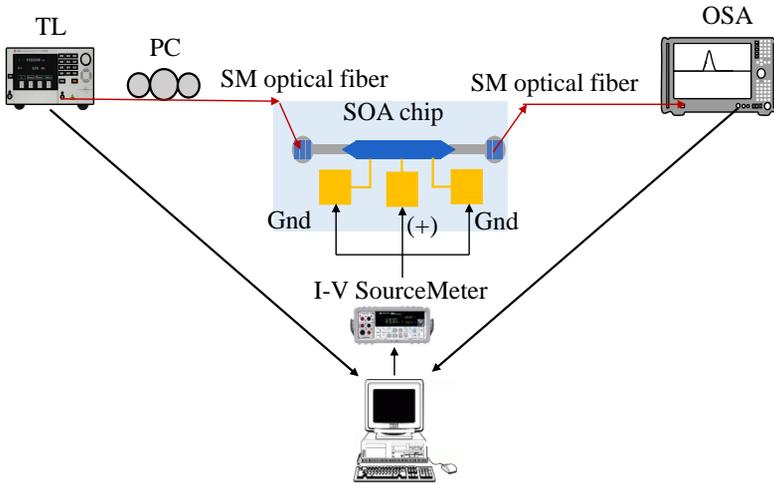


Figure 3.9: The measurement setup used to characterize the SOAs, which includes a tunable laser (TL), polarization controller (PC), optical spectrum analyzer (OSA), and current-voltage source-meter. The computer is used to control the instruments and to process the measured data.

reference passive Si waveguides are also fabricated along with amplifiers on the same chip and they undergo the same processing steps as the grating couplers used for interfacing with the SOAs. The wavelength-dependent transmission response of the grating coupler is measured using a tunable laser (Santec TSL-510) and an optical spectrum analyzer (OSA, Advantest Q8381A). The angle of the fiber holders is optimized to align the maximum transmission wavelength of the grating couplers with the gain peak of the two discussed SOAs. At this angle and at a wavelength of 1560 nm, the coupling loss per grating coupler is 12 dB. Since the III-V SOAs printed on both SOI designs are nominally the same, the differential resistance is also nominally the same, 10.0Ω at 80 mA bias current or 1.8 kA/cm^2 current density. The measurement setup shown in Fig. 3.9 is used for optical characterization. The CW input signal generated by a tunable laser is polarization-controlled and coupled into the SOA chip through the grating couplers. At the other end of the SOA, the output power is coupled from the grating coupler to a single mode optical fiber connected to the OSA (Advantest Q8381A), used to measure the spectrum with 1 nm resolution. The sourcemeter (Keithley 2400) controls the input bias current and probe needles are used to electrically contact the SOA.

In the first experiment, the bias current of the amplifiers is varied and the output power is measured for different wavelengths. The output and input

power are then normalized with the loss of the reference waveguide and the SOA gain is calculated. This measurement is performed for two values of on-chip optical input powers, a low one of -24 dBm, and a high one of 0 dBm, where the SOAs are saturated. Net on-chip gain is observed above 44 mA and 58 mA for the full-coupling and the partial-coupling SOA at 1548 nm and 1565 nm respectively. The 1548 nm wavelength corresponds to the maximum gain wavelength for the partial coupling SOA at 160 mA bias current. The full-coupling SOA exhibits parasitic lasing at higher bias currents (> 140 mA). It is deduced from the free spectral range of the lasing modes that the lasing is due to the reflections between the two grating couplers. Therefore, for the full-coupling SOA all the measurements are performed at lower bias currents and at 1565 nm, slightly off the gain peak of 1557 nm, where parasitic lasing occurs. The full-coupling SOA was only biased till 140 mA (3.17 kA/cm²) as no improvement is seen in the gain beyond 140 mA. However, the partial-coupling SOA could be biased until 180 mA due to better heat conduction through the Si waveguide. It can be seen in Fig. 3.10 that at the high input power of 0 dBm the gain reduces to 10 dB at 140 mA and 12 dB at 180 mA for the full-coupling and partial-coupling SOA, respectively. In the unsaturated regime, when the input power is -24 dBm, the full coupling SOA exhibits higher gain for a particular bias current.

In order to measure the variation of on-chip gain for both SOAs with on-chip input power, the tunable laser's optical power is varied and the SOA output power at the signal wavelength is recorded using the OSA and gain is calculated, as shown in Fig. 3.11. The maximum output power at 140 mA is 10.8 dBm (at 1565 nm) and 11.3 dBm at 160 mA (at 1548 nm) for the full-coupling and partial-coupling SOA, respectively. The measurement is repeated for several bias currents. The on-chip gain of the SOA doesn't increase beyond 140 mA in the case of full-coupling at 1565 nm wavelength and 160 mA at 1548 nm wavelength for the partial-coupling SOA. This is attributed to the self-heating of the devices. The measured data is then fitted with an expression that relates the gain G to the input power P_{in} to estimate the gain saturation power P_{sat} and small signal gain G_0 [19, 20]:

$$G(P_{in}) = G_0 \frac{1 + \frac{P_{in}}{P_{sat}}}{1 + G_0 \frac{P_{in}}{P_{sat}}} \quad (3.1)$$

The result of the fitting is shown with solid lines in Fig. 3.11.

The values of P_{sat} and G_0 extracted from the fitting procedure are then plotted against the bias current as shown in Fig. 3.12. P_{sat} increases with

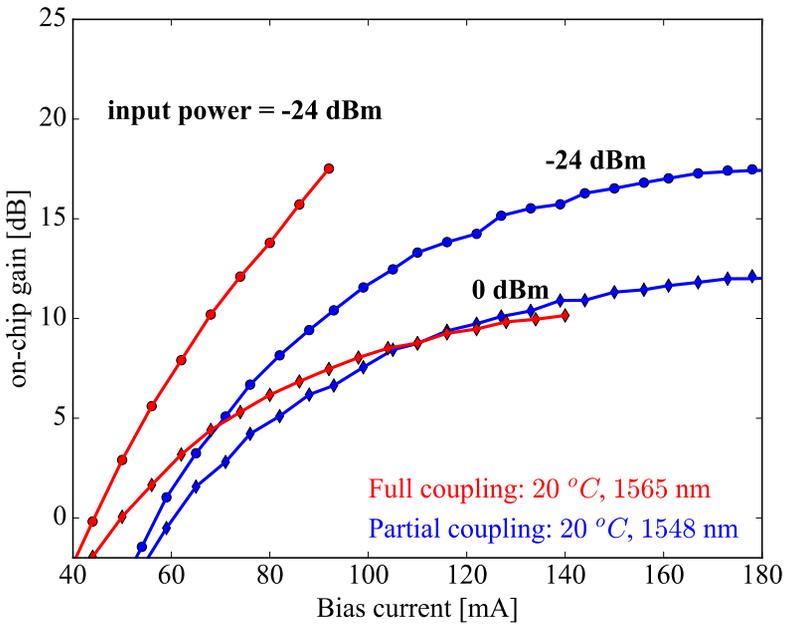


Figure 3.10: The variation of on-chip gain with the bias current at lower on-chip input power of -24 dBm and higher on-chip input power of 0 dBm for both the full-coupling (in red) and partial-coupling (in blue) SOA design.

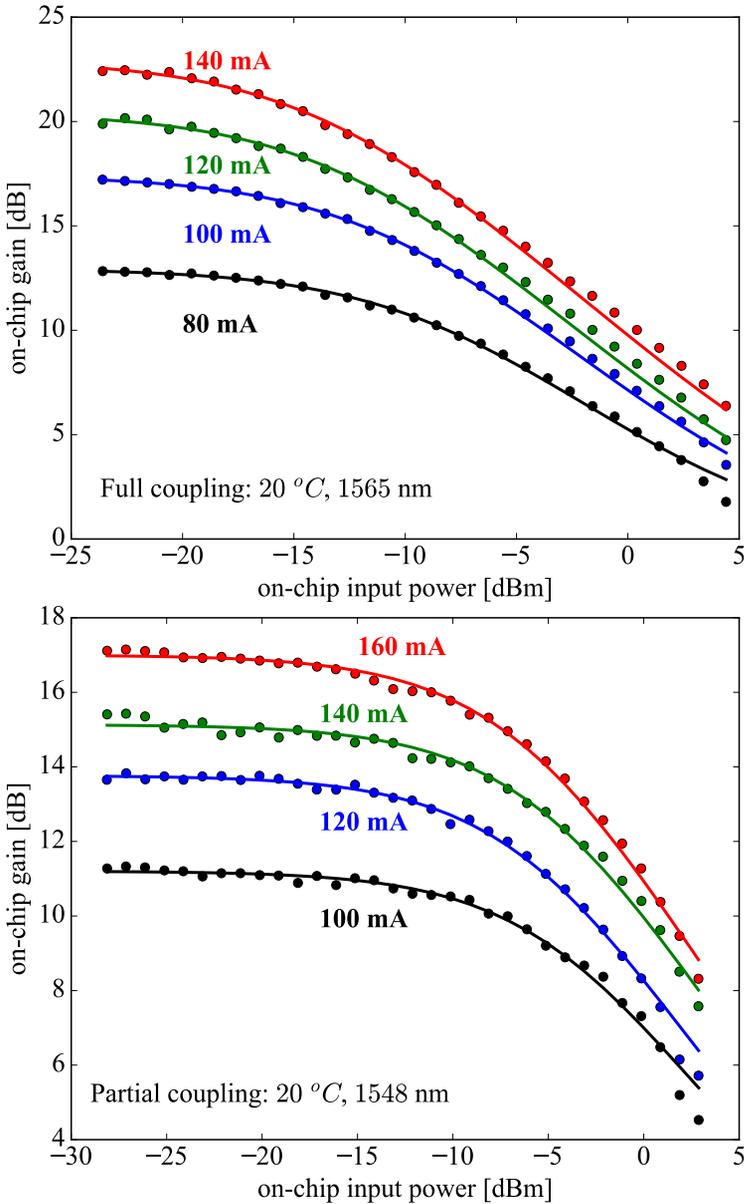


Figure 3.11: Variation of the on-chip gain with the on-chip input power for various bias currents, (top) for the full-coupling design at 1565 nm, (bottom) for the partial-coupling design at 1548 nm. Data points represent the measured values and the solid lines are a fitting with Eq. (3.1).

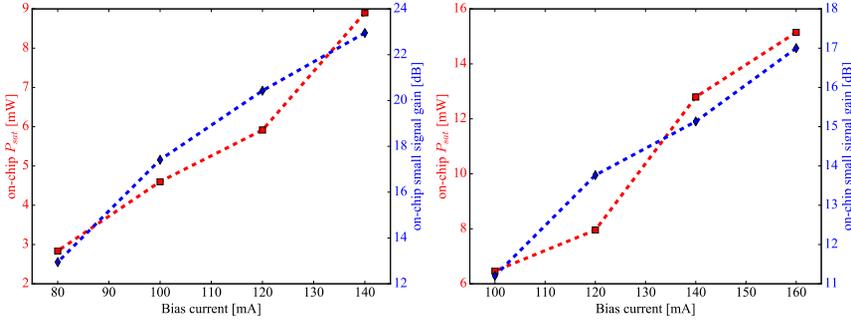


Figure 3.12: The markers represent the fitted values for P_{sat} and for the small-signal gain G_0 for the full-coupling design (left) and partial-coupling design (right).

the bias current and is described by [20]:

$$P_{sat} = \frac{hc \sigma_{xy}}{\Gamma a \tau \lambda} \quad (3.2)$$

where σ_{xy} is the quantum well cross sectional area, λ is the wavelength, a is the differential gain, Γ is the confinement factor in the pumped region of the quantum wells, h is Planck's constant, τ is the carrier lifetime and c is the speed of light in vacuum. When operating the SOA at high bias current, a and τ reduces, which increases P_{sat} [20]. At 140 mA P_{sat} is 12.8 mW and 9.0 mW for the partial and full-coupling SOA, respectively. The partial-coupling SOA (lower confinement in the QWs) has a maximum P_{sat} of 15 mW at 160 mA bias current (417 mW power dissipation) and a small-signal gain of 17 dB. In comparison, the full-coupling SOA (higher confinement factor in the QWs) has a maximum P_{sat} of 9.2 mW at 140 mA bias current (336 mW power dissipation) and a small-signal gain of 23 dB. Hence, the SOA with higher optical confinement factor can provide more gain, but however, has lower saturation power and vice versa.

In order to measure the wavelength-dependent small-signal gain of the SOA and the bandwidth, the wavelength of the input light is swept while the on-chip input power is kept at -24 dBm and the output spectrum is observed on the OSA. The output power at the input wavelength is recorded and normalized with the transmission spectrum of the grating coupler to calculate the on-chip gain, shown in Fig. 3.13 for the case of the full-coupling SOA. The measurements were recorded for three different bias currents. The dot markers represent the measured values, the solid line represents the curves obtained by fitting the formula [21]

$$G(\lambda) = G_p \exp[-A(\lambda - \lambda_p)^2] \quad (3.3)$$

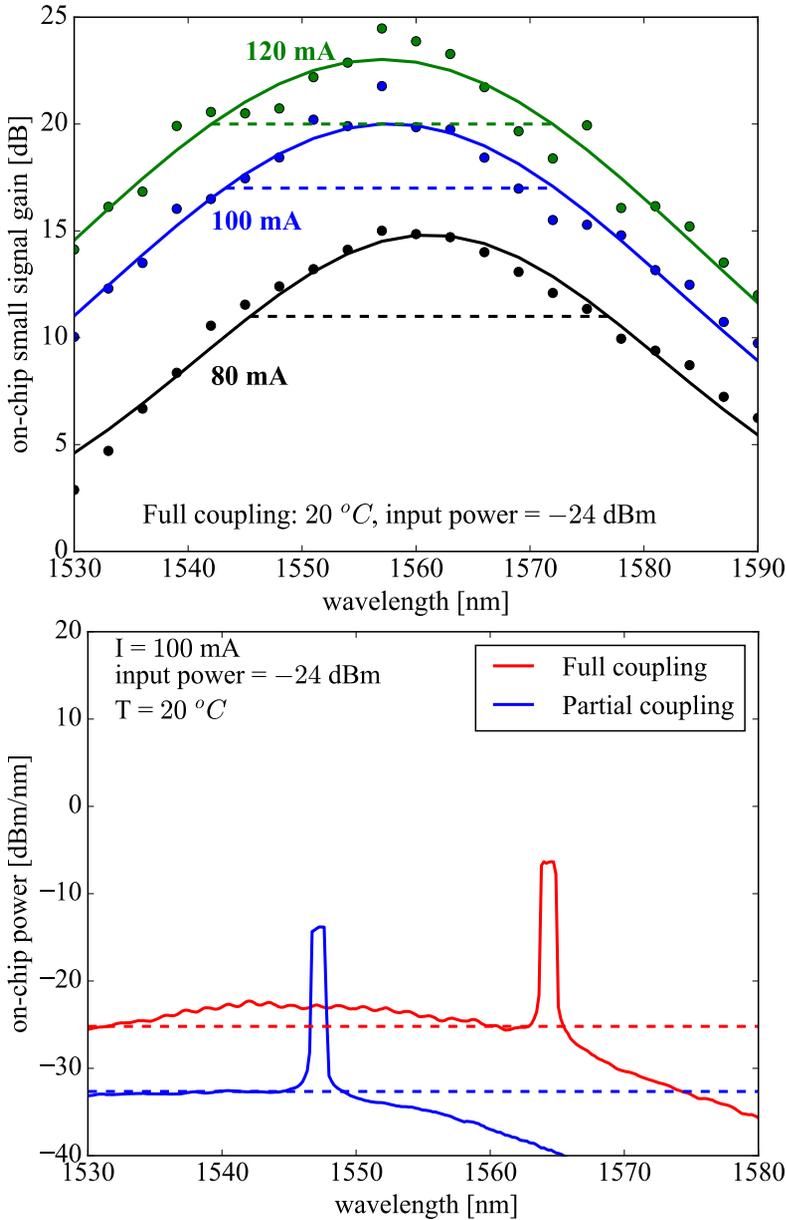


Figure 3.13: On-chip gain measured as a function of wavelength and fitted with Eq. (3.3) for (top) full-coupling SOA and (bottom) SOA output spectrum measured with a 0 dBm input power at 100 mA. The red and blue dotted lines indicates the ASE level involved in the computation of the noise figure.

where $G_p \equiv \exp[g_{net}(\lambda_p)L]$ is the peak gain, λ_p is the wavelength at which the maximum gain occurs and A is related to the gain bandwidth. The 3-dB gain bandwidth of the SOA increases with the bias current and it is 30 nm at 120 mA (2.71 kA/cm²). Similar gain bandwidth is obtained for the partial-coupling device.

Finally, the on-chip noise figure (NF) which determines the degradation of the signal-to-noise ratio as a signal propagates through the SOA, is estimated. There are two main noise contributors: the shot noise and the excess noise $F_{sig-ASE}$ produced by the beating of the signal and the ASE [21]. The shot noise is given by $1/G$, where G is the gain and the excess noise can be written as [21]:

$$F_{sig-ASE} = \frac{2\lambda^3}{Gc^2h} \frac{P_{ASE}}{\delta\lambda} \quad (3.4)$$

where λ is the signal wavelength and G is the on-chip gain. The on-chip P_{ASE} is measured in a wavelength range of $\delta\lambda$ for a given input power using the OSA. We calculate the $F_{sig-ASE}$ for higher on-chip input powers (> 0 dBm) and lower on-chip input powers (< -15 dBm) for the full-coupling SOA and partial-coupling SOA. At 100 mA and 1565 nm, $F_{sig-ASE} \approx 8.6$ dB for an on-chip input power of -24 dBm and $F_{sig-ASE} \approx 9.54$ dB at 0 dBm on-chip input power. Similarly, at 1548 nm the partial-coupling SOA has $F_{sig-ASE} \approx 7.0$ dB at -24 dBm on-chip input power and $F_{sig-ASE} \approx 8.6$ dB at 0 dBm on-chip input power. Figure 3.13 shows the spectrum used in the calculation of the noise figure at -24 dBm on-chip input power. The noise figure values are comparable to the values previously reported in the literature for III-V-on-Si SOA [19, 22].

3.5 Conclusion

In this chapter, we demonstrated micro-transfer-printed SOAs on silicon photonic integrated circuits, operating in the C-band. The design and processing of the SOAs is described. Two designs are presented, with a trade off in small-signal gain and output saturation power. An alignment tolerant taper structure is designed that can cope with 1.0-1.5 μm lateral misalignment, which is a typical alignment accuracy that can be obtained when printing arrays of III-V devices. This showcases the potential of the micro-transfer-printing technique for the scalable integration of III-V semiconductor optical amplifiers and other waveguide-coupled III-V devices (such as laser diodes, modulators, photodetectors) on a Si photonic wafer. While the current demonstration is carried out on a passive Si photonic wafer,

comprising only Si passive waveguide structures, the same integration approach can be used on full-platform Si PICs comprising high-speed Si/Ge photonic components, by locally opening the back-end and micro-transfer printing the III-V components in the formed recess. Such an integration would complete the toolkit for advanced photonic systems-on-a-chip based on a silicon photonics platform. The SOAs show performance comparable to the devices made using other heterogeneous integration technologies such as die-to-wafer bonding.

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4

Micro-transfer-printed DFB lasers

4.1 Introduction

Photonic integrated circuits (PICs) are currently being utilized mostly in telecom and datacom markets [1]. Recently, various sensing products based on PICs have also been introduced in the market. The realization of aforementioned products are based on the smaller form-factor, the lower fabrication cost due to wafer-level high-volume production, and the wide range of functionalities PICs can offer [2, 3]. Silicon photonics (SiPh) offers an added advantage as it can utilize the acquired knowledge and massive infrastructure developed for electronic IC fabrication over the last decades. Today, there are several CMOS-fabs around the world with a mature process flow for SiPh PICs. However, integration of a laser source in these foundry process flows is still a bottleneck. As mentioned in the previous chapter, micro-transfer printing is promising for such a task. It only requires opening of a window above the Si waveguides for the heterogeneous integration of the III-V material stack. This can allow the development of various types of light sources.

A distributed feedback laser is one of the most widely used light sources in applications including telecommunication and sensing. It is an essential component of an optical transmitter. They can have wide-modulation bandwidth and therefore avoid needing an external modulator in a transmitter, which reduces the component count and the overall insertion loss.

Moreover, the distributed-feedback (DFB) laser emission wavelength can be continuously tuned up to 2-3 nm by tuning the bias current. This is particularly useful for tunable-diode absorption spectroscopy (TDLAS) [4]. In the literature, several demonstration of DFBs can be found based on III-V/Si die-to-wafer bonding with good static and dynamic characteristics [5]. State-of-the-art devices have threshold currents as low as 10 mA and a waveguide-coupled output power of tens of mW [6]. In the previous section, we demonstrated the heterogeneous integration of processed III-V SOAs on a silicon-on-insulator (SOI) platform. In this chapter, we integrate distributed feedback (DFB) lasers on silicon photonic integrated circuits based on the micro-transfer printing of processed III-V SOA coupons on quarter-wave shifted gratings.

4.2 Gen 1 micro-transfer-printed DFB lasers

4.2.1 Design of DFB laser

The SOA design has been discussed in the previous chapter. We use the same pre-processed SOAs as the gain region. The silicon device layer is 400 nm thick and it is etched 180 nm to define the waveguides. The feedback in a DFB laser is provided by a Bragg grating. The grating is etched on the surface of the waveguide. In order to have a longitudinal mode at the Bragg wavelength λ_B , a bidirectional π phase shift is added to break the modal degeneracy, in other words, a quarter-wave shift in the middle of the grating. The period of the grating can be calculated for a DFB laser emission wavelength λ_0 by [6]

$$\Lambda = \frac{m\lambda_0}{2n_{\text{eff}}} \quad (4.1)$$

where n_{eff} is the effective index of the fundamental mode and m is the order of the grating. A grating period Λ of 244 nm corresponds in our design to an emission wavelength λ_0 of 1570 nm. It will be discussed later that in our full-chip design several DFB lasers with a range of different grating periods are included.

The grating coupling coefficient κ represents the strength of coupling between forward and backward propagating waves in the grating and is a measure of reflection per unit length (cm^{-1}). For a weakly-coupled uniform rectangular grating, κ can be approximated by: [7]

$$\kappa = \frac{2(n_{\text{Si}} - n_{\text{etchSi}})}{\lambda_0} \sin(m\pi D) \quad (4.2)$$

where n_{Si} and n_{etchSi} is the effective index of the III-V/Si fundamental mode in the unetched part and etched part of the grating, respectively. D is the duty cycle of the grating. For a first order grating ($m = 1$) and second order grating ($m = 2$), κ is maximum when duty cycle is 50% and 25% (or 75%), respectively. In all of the designs, we will opt for the first order grating as it results in the most compact devices. The optical properties such as effective indices of the modes are calculated using Lumerical Mode Solutions [8].

Figure 4.1 shows the map of κ calculated in cm^{-1} and the overlap of the III-V/Si optical mode in the etched and unetched part of the grating.

The BCB layer thickness is 60 nm for this calculation. It can be seen that increasing etch depth or the width of the Si waveguide increases κ (the III-V waveguide width in the gain section is $3.2 \mu\text{m}$). The overlap also has a similar dependence on the grating width and etch depth.

The etch depth and the grating width is chosen to be 25 nm and $3.0 \mu\text{m}$, respectively. The III-V waveguide width in the gain section is $3.2 \mu\text{m}$ and the DFB grating is defined in a $3.0 \mu\text{m}$ wide waveguide and it is $500 \mu\text{m}$ long, with a quarter wave shift in the middle. The III-V SOA is $950 \mu\text{m}$ long including a $500 \mu\text{m}$ gain section and two $225 \mu\text{m}$ III-V alignment-tolerant adiabatic tapers on both sides of the SOA. The $3.0 \mu\text{m}$ wide waveguide ensures high coupling efficiency in case of misalignment between the III-V SOA and Si waveguide. The complete design is shown in Fig. 4.2

4.2.2 SOI lithography mask layout

It is a good practice to design a layout keeping in mind its use case. As mentioned earlier, DFB lasers can be tuned without mode-hopping which makes them a good candidate for TDLAS measurements. Therefore, we decided to develop sources for TDLAS measurements of CO_2 , CO , NH_3 and HCN in the context of the INTERREG SAFESIDE project. For CO_2 and CO absorption lines around 1570 nm are set as a target, whereas, for NH_3 and HCN the absorption lines are around 1540 nm.

Figure 4.3 shows the designed layout of the SOI chip for the development of the DFB lasers. The design is overlaid on a grid with a cell size of $500 \mu\text{m}^2$, which represents a write field of the e-beam. As we know, at the boundary of each write field the patterning is susceptible to stitching errors, when using the normal writing mode. In order to avoid that, the waveguides are written in FBMS writing mode, whereas, gratings and markers are written in the normal writing mode. We use a $3.0 \mu\text{m}$ wide, 25 nm etched grating ($500 \mu\text{m}$ long). The $500 \mu\text{m}$ long gratings are placed inside a write field.

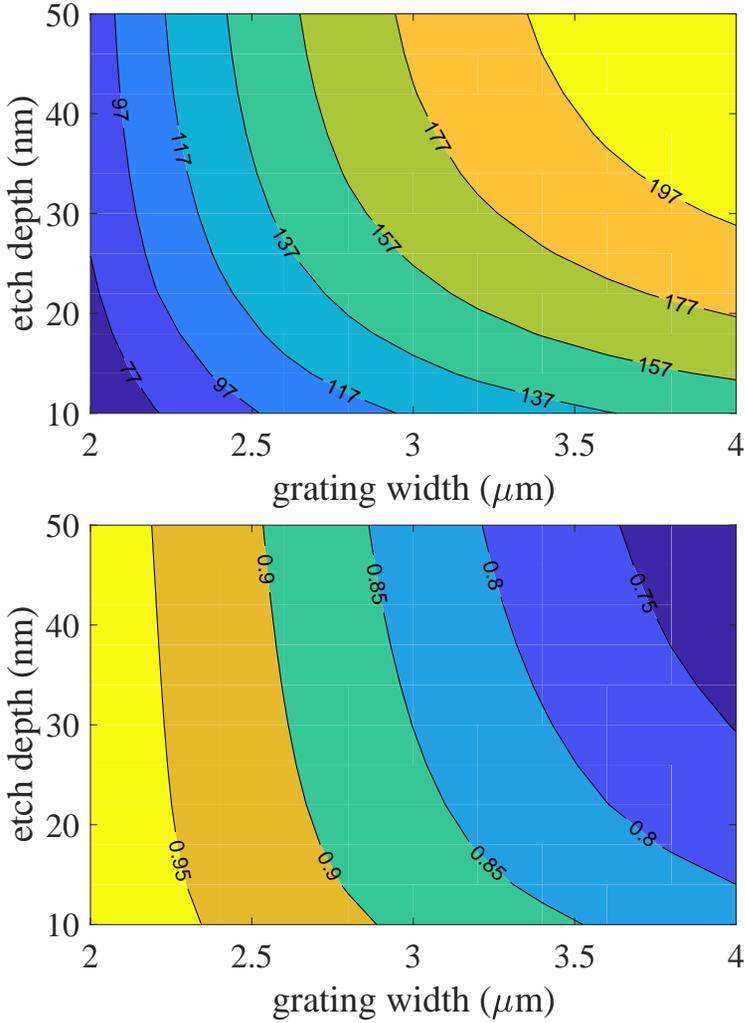


Figure 4.1: (top) Calculated map of κ in cm^{-1} for different widths and etch depths of the grating, (bottom) Calculated map of modal overlap between etched and unetched section of the grating for various grating widths and etch depths.

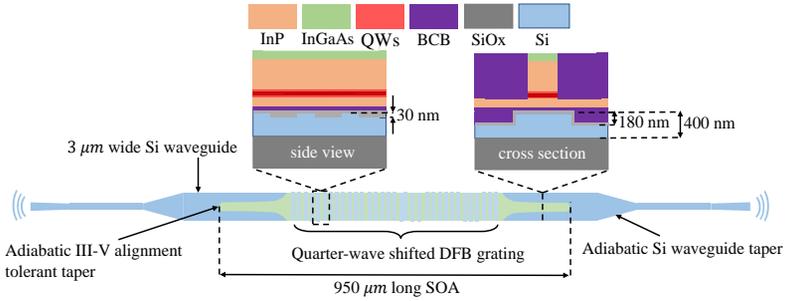


Figure 4.2: Schematic illustrating the design of the DFB laser, the cross-section view of the adiabatic taper and the side view of the DFB grating.

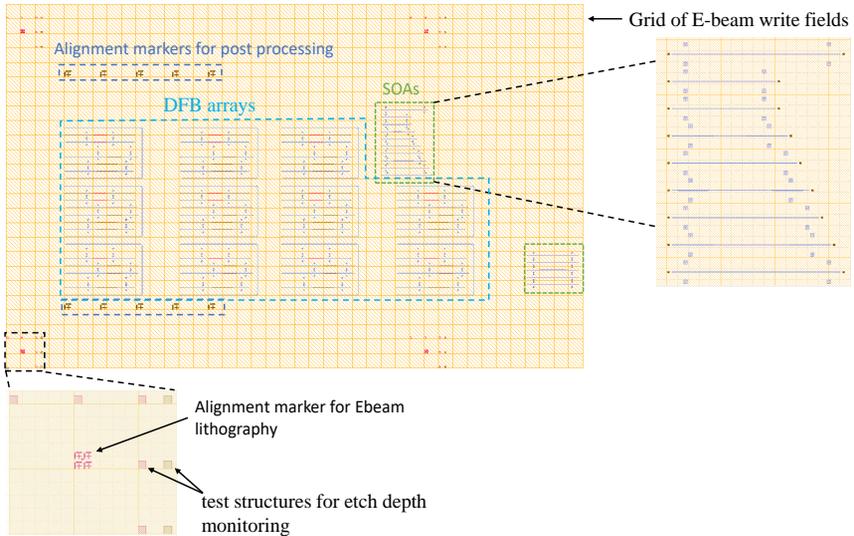


Figure 4.3: Schematic illustrating the DFB SOI layout designed for processing with e-beam.

This allows the edge of write field to overlap with the quarter-phase shift, thus, preventing a stitching error in the period of the grating. At the top and bottom of the design, alignment markers for post-processing of the micro-transfer-printed coupons are also included. Since there are two different etching steps (25 nm and 180 nm), the e-beam lithography has to be performed twice. At the edge of the grid, alignment markers for aligning subsequent lithography steps can be seen. These markers are surrounded by $60 \mu\text{m}^2$ squares to monitor the etching of the gratings and waveguides. The red squares and brown squares are for 25 nm etch and 180 nm etch step measurement using the Filmetrics tool, respectively. In the next section, we will discuss the fabrication of the DFB lasers. We will first describe the fabrication of the SOI sample using e-beam. Then micro-transfer printing and post-processing of the printed SOAs will be discussed.

4.2.3 Fabrication

The development of DFB lasers through micro-transfer-printing requires preprocessed SOAs and SOI waveguide circuits with DFB gratings and grating couplers to probe the light. We use the same SOAs discussed in the previous chapter. The development of the SOI photonic circuit will be described in the following section.

4.2.3.1 SOI processing

The development of a single-etch-step SOI circuit using e-beam has been described in chapter 3. However, as mentioned in the section 4.2.1 one of the DFB grating designs is etched 25 nm and the Si waveguides, grating couplers and alignment markers are etched 180 nm. In order to define two etch depths, the e-beam lithography has to be performed twice. The process flow is illustrated in Fig. 4.4. The process starts with cleaving a Si sample from 400 nm thick Si wafer. These wafers are covered with a protective resist layer that is removed with acetone, IPA and 10 mins of oxygen plasma in a Tepla barrel etcher. It is then spin-coated with ARP-6200.09 e-beam resist and a charge reduction layer Electra-92 and baked at 150 °C and 90 °C, respectively. The sample is now ready to be loaded in the e-beam lithography tool for exposure. First, the layer in the GDSII layout with shallow grating and the overlay markers are written in normal writing mode. The exposed sample is then developed by immersing the sample in water, n-amylacetate, IPA for 30 s, 1 min and 30 s, respectively. The sample is then dried with a nitrogen gun. The thickness of the Si is measured on test structures shown in Fig. 4.3. The dry etching process described in chapter 3

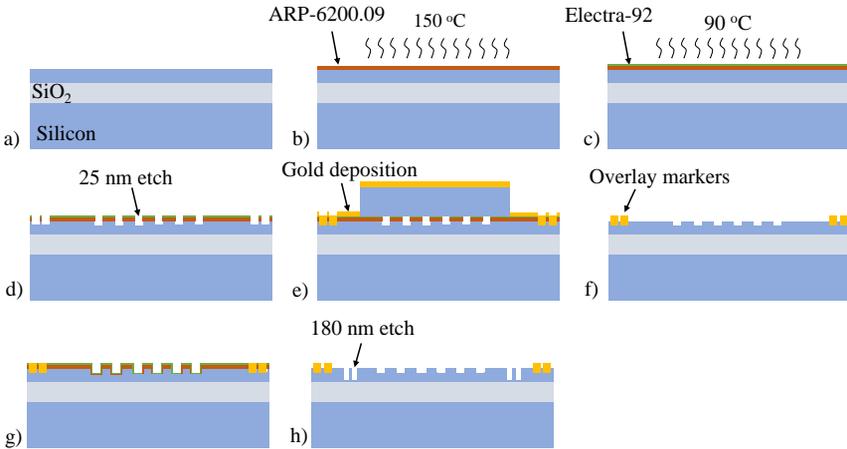


Figure 4.4: a) 400 nm SOI wafer, b) Spin coating of ARP-6200.09 e-beam resist and baking at 150 °C, c) Spin coating of charge reduction layer Electra-92 at 90 °C, d) Development of the e-beam resist and etching in RIE, e) Ti/Au deposition after covering the chip with a Si piece, f) Lift-off and resist removal, g) Repeat step (a-d), h) Final look at the SOI sample with two etching steps.

is used to etch Si using RIE. A mixture of CF_4 , H_2 and SF_6 is used (210 W, a pressure of 20 mTorr and 100 sccm CF_4 , 7 sccm H_2 and 3 sccm SF_6). After each etch cycle, the etch-depth is measured on the test structures using the Filmetrics tool and the etch rate is calculated to set the etching time for the next cycle. Once the targeted etch-depth is reached, the resist is removed with oxygen plasma in a barrel etcher.

The process of alignment between consecutive lithography steps in e-beam is called overlay. The e-beam tool provides the functionality of manual detection of alignment markers as well as automatic detection using pattern recognition. The overlay accuracy is dependent upon the clarity (sharpness and contrast) of alignment markers and the detection technique. The automatic detection allows for better alignment (few ten's of nm) and with the manual detection 100-200 nm alignment accuracy can be achieved. DFB gratings are not alignment critical structures, moreover, in the layout, the width of gratings is designed wider than the waveguide to have better alignment tolerance. Therefore, we use the manual alignment detection scheme.

In order to improve the clarity and visibility of the alignment markers patterned in the first lithography, a thin layer of Ti/Au is deposited on the sample. However, before the deposition, the central part which contains the main structures is covered by a piece of Si clamped on top of the sam-

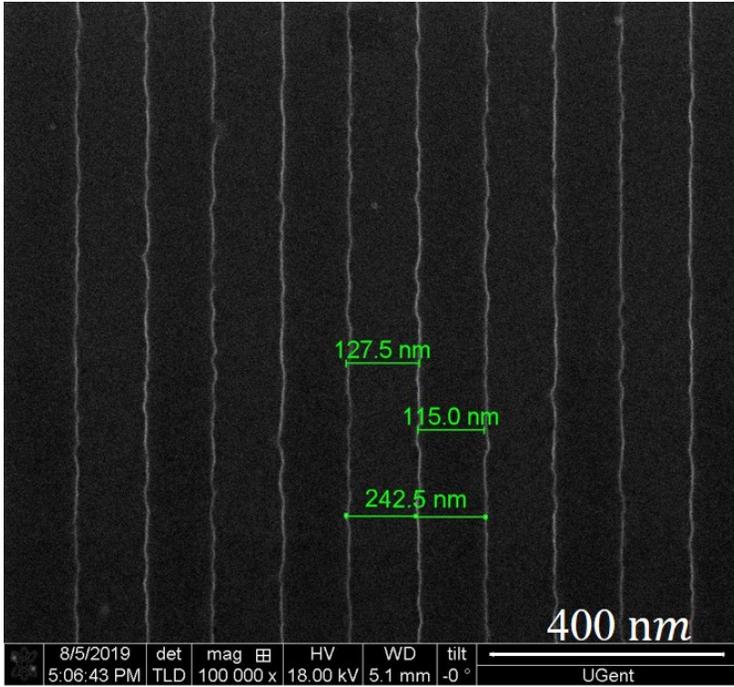


Figure 4.5: SEM image of shallow etched grating

ple. This prevents the deposition of metal on the actual structures and only the alignment markers at the edges are covered with metal. After the deposition, the sample is immersed in AR 600-71 to remove the resist and lift-off the metal from the edges. To thoroughly remove the resist, the sample is also etched with oxygen plasma in a Tepla barrel etcher for 10 mins. At this step, the shallow-etch gratings and the overlay markers have been patterned.

The sample can now be prepared for the second lithography step. Using the same recipe, the ARP-6200.09 e-beam resist and charge reduction layer Electra-92 are spin-coated and baked. The sample is then loaded into the e-beam lithography tool for exposure. After the overlay of markers, waveguides are written using the FBMS writing mode. Subsequently, grating couplers, post-processing markers and transfer-printing alignment markers are written. After the completion of the exposure, the sample is developed with a similar recipe and dried. It is then etched in RIE with the aforementioned recipe. The resist is removed in the end with oxygen plasma. The fabrication of the sample is now complete. Figure 4.5 shows the SEM image of fabricated shallow-etch grating. The duty cycle of partial-etch

grating is close to 50%. The period of all the gratings is consistent with the designed value. In the next section, the micro-transfer-printing process will be discussed.

4.2.3.2 III-V processing on InP

The processing of SOA coupons has been described in detail in Chapter 2. Nonetheless, for the sake of completeness it will be discussed briefly in this section. SOA coupons are fabricated in a dense array on the III-V source wafer with a vertical pitch of 90 μm and are 45 μm wide. The first step in the SOA processing is the etching of the protective thin InP layer on top of the p-InGaAs contact. It is removed by wet-etching in HCl. This is followed by the deposition of a SiN hardmask and standard i-line optical lithography is used to pattern the hardmask. The mesa is formed with a dry etching process and it is also briefly etched in the diluted HCl to make it V-shaped, as shown in Fig. 4.6. After this, SiN is deposited again to passivate the side-walls of the mesa. The active region is then etched using both dry and wet-etching. Subsequently, a lift-off process is used to deposit the Ni/Ge/Au/Ti/Au n-contact and the device is passivated with SiN and BCB. With a similar lift-off process Ti/Au is deposited for the p-contact. The coupon boundary is then patterned and etched using a dry etching process. This ends the processing of the III-V SOA, however, for under-etching the device so that it can be picked-up by the PDMS stamp, the release layer is patterned and the tethers are formed on the InP substrate as shown in Fig. 4.6(b-c). An aqueous FeCl_3 solution at 7 $^\circ\text{C}$ is used to under-etch the AlInAs release layer. It takes 45 mins to release the 45 μm wide coupons. The coupons during and after the release layer etch are supported by the photoresist tethers anchored to the InP substrate, as shown in Fig. 4.6(d).

4.2.4 Micro-transfer printing process

The micro-transfer-printing process is illustrated in Fig. 4.6(e-i). The SiPh sample is first prepared for the micro-transfer printing. A 37 nm thick SiO_2 is deposited to achieve the designed gap between the Si waveguide and III-V waveguide. This allows to control the gap better as BCB thickness changes during printing due to applied force. Subsequently, 1:4 DVS-BCB-35:Mesitylene is spin coated on the sample. A single-post PDMS stamp appropriate to the size of coupon is used for the micro-transfer printing. The SOA coupons are picked individually from the III-V source sample using an X-Celeprint μTP -100 tool and pattern recognition is used to align them to the Si target waveguide structure. There are alignment markers on SOA

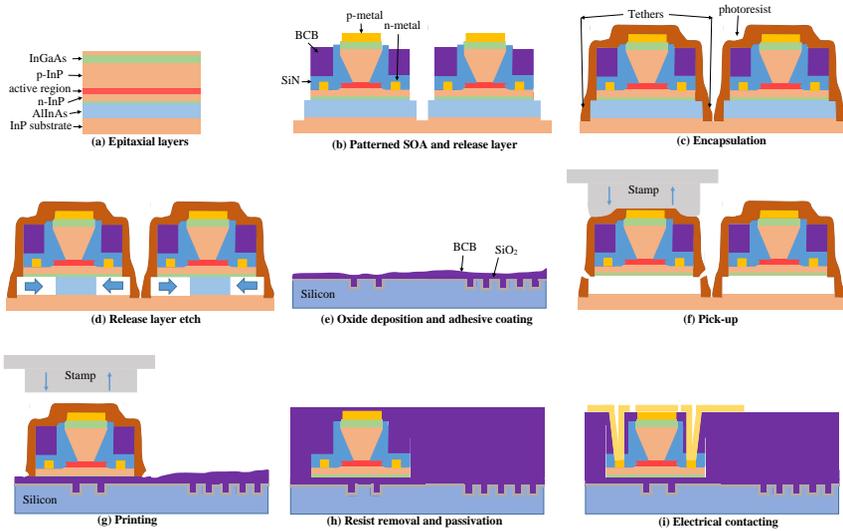


Figure 4.6: Schematic micro-transfer-printing process flow of DFB lasers, (a-d) depicts the processing of SOAs on the InP substrate, (e) illustrates the preparation of the patterned SiPh sample prior to micro-transfer-printing, (f-g) illustrates the picking and printing of the SOAs on the SiPh sample, (h-i) illustrates the post-processing steps on the SiPh sample, which includes passivation and electrical contacting.

coupons and on the side of the Si waveguides. The μ TP-100 tool software recognizes the markers and finds their center, which is then aligned in the lateral and vertical directions by moving the SiPh target sample. After the alignment process is completed, the SOA coupon is laminated to the target sample and shear force is applied to detach the laminated coupon from the stamp. The stamp then slowly moves upwards from the target leaving the SOA attached to the silicon photonic target waveguide structure.

After printing all the SOA coupons, a dry etching process is used to remove the photoresist encapsulation and the DVS-BCB is fully cured by baking it at 270 °C. The SiPh chips are then passivated with a thick DVS-BCB layer as shown in Fig. 4.6(h). Vias are patterned with i-line optical lithography and are defined using dry etching. Finally, 40nm/700nm TiAu is deposited using a lift-off process to define contact pads as illustrated in Fig. 4.6(i). Figure 4.7 shows microscope pictures during the device processing. Figure 4.7(a) shows six coupons printed on DFB gratings on the SOI. Figure 4.7(b) shows a microscope image of a micro-transfer-printed coupon on the SiPh waveguide circuit, showing the clean breaking of the tethers. Figure 4.7(c) illustrates the coupon after removal of the encapsulation layer and Figure 4.7(d) shows a microscope image after the etching of the n-metal Via on the coupon to make electrical connection. Finally, Fig. 4.7(e) depicts the DFB lasers after contact metal deposition.

4.3 Characterization

The DFB laser is characterized on a temperature-controlled stage. Grating couplers on both sides of the DFB grating couple light out of the chip into single-mode optical fiber (SMF). DC probes are used to bias the lasers. These are connected to a Keithley2400 sourcemeter. A HP 8513A power meter measures the optical power coupled into the single-mode optical fiber. Reference waveguides with grating couplers are also fabricated near the DFB circuit. These are used to measure the grating coupler loss and to calculate the on-chip power in the waveguide. The spectrum is measured using an optical spectrum analyzer.

Figure 4.8 illustrates the measured on-chip optical power against bias current of a shallow-etch DFB grating lasers with a period of 241 nm and 246 nm. Both the lasers have similar threshold current of 45 mA. The on-chip optical power is 1.8 mW and 1.1 mW for the grating period of 241 nm and 246 nm, respectively. The electrical resistance is 10 Ω at 65 mA bias current. The difference in the slope efficiency of the two lasers can be attributed to lateral misalignment inherent to the micro-transfer-printing tool. Figure 4.9(a) and (b) depicts the measured spectrum of the shallow etch

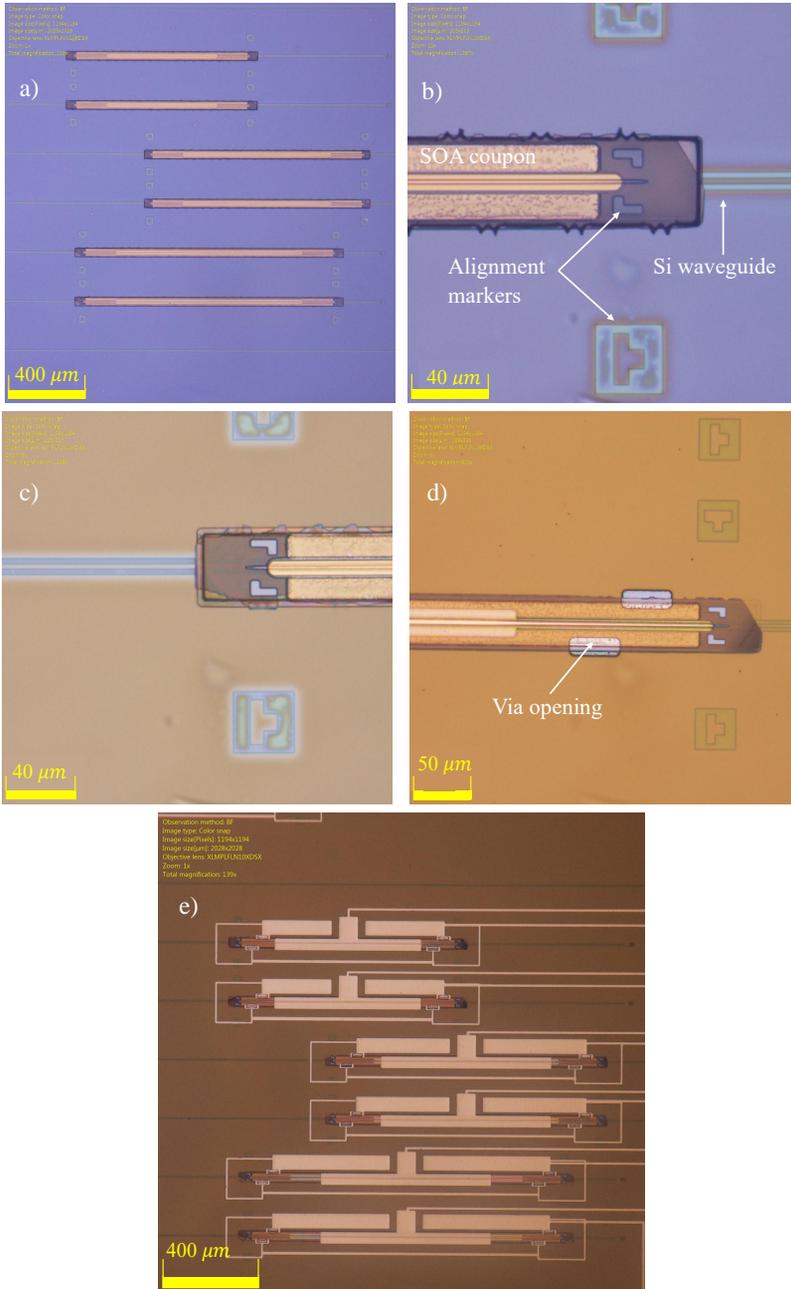


Figure 4.7: (a) Microscope image of SOA coupons micro-transfer printed on SOI, (b) Zoomed-in image (c) after encapsulation removal, (d) after Via opening for n-metal contact and (e) final look after contact metal deposition.

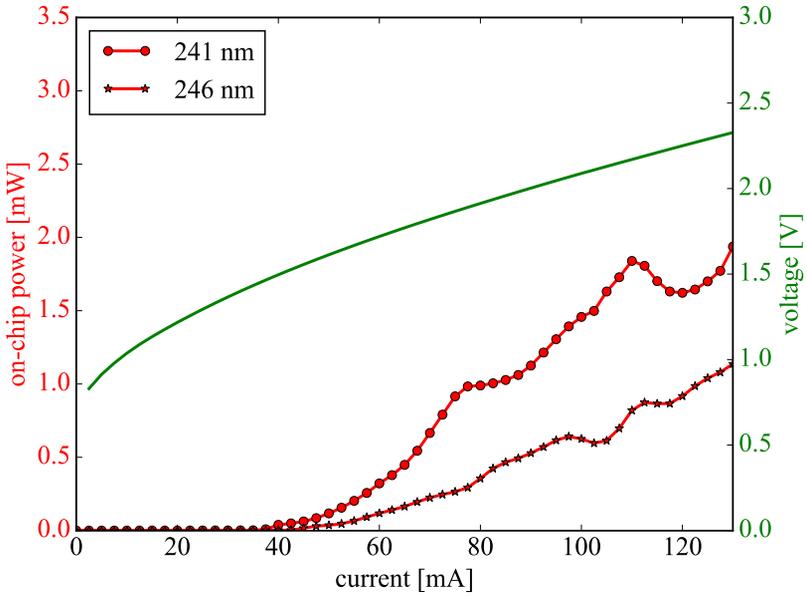


Figure 4.8: Measured on-chip optical power and voltage versus bias current at 20 °C for a grating period of 241 nm and 246 nm.

DFB lasers for various bias currents and grating period of 241 nm and 246 nm, respectively. Multiple stop-bands and lasing peaks can be seen. It is found from simulations that the multiple peaks correspond to higher order transverse modes in the gain section that have a similar and/or higher confinement factor in the active region as compared to the fundamental mode. Moreover, due to the misalignment between the SOA and Si waveguide and fabrication imperfections of the adiabatic taper higher order modes can couple into the fundamental mode of the Si waveguide resulting in multiple stop-bands and lasing peaks in the output spectrum. The stop-band is 3.4 nm wide which corresponds to a κL of 6.4 and calculated confinement factor in the active region is 6.78 percent.

One particular DFB laser in this sample depicted single-mode behavior. The LI curve and the spectrum of this laser is illustrated in Fig. 4.10. Single-mode lasing is observed at 1530 nm with SMSR of more than 33 dB. The higher order modes did not have sufficient modal gain to reach threshold as they lie at the edge of the gain spectrum. The DFB tunes over 1.4 nm in wavelength when the bias current is varied from 60 mA to 140 mA shown in the inset of Fig. 4.10(a). The single-sided laser output power at 130 mA is 3.75 mW. The threshold current of the laser is 62 mA.

In the next section, we will discuss another DFB laser design that could suppress higher-order modes in the gain section without significantly degrading the alignment tolerance of the adiabatic taper.

4.4 Gen 2 micro-transfer-printed DFB lasers

4.4.1 Design

The silicon waveguide platform consists of a 400 nm thick Si device layer on a 2 μm thick buried oxide (BOX). The Si waveguide in the gain section of the DFB laser is 2.0 μm wide and has a 20 nm etch depth. It is defined by etching 3.0 μm wide trenches. 50 nm PECVD SiN is deposited and etched periodically on the top of the Si waveguide to define the quarter-phase shift grating. The design schematic and the longitudinal cross-section are illustrated in Fig. 4.11. One of the major issues when micro-transfer-printing a processed SOA is the stringent alignment requirement between III-V and Si waveguide required for efficient coupling of light from the III-V to Si waveguide. Efficient coupling can be achieved by designing an alignment-tolerant adiabatic taper as discussed in Ch 2. 1 μm alignment tolerance is achieved, when the alignment tolerant adiabatic taper is micro-transfer-printed on a 3.0 μm wide silicon waveguide. Reducing the width of the III-V and Si waveguide has an adverse effect on the alignment tolerance of

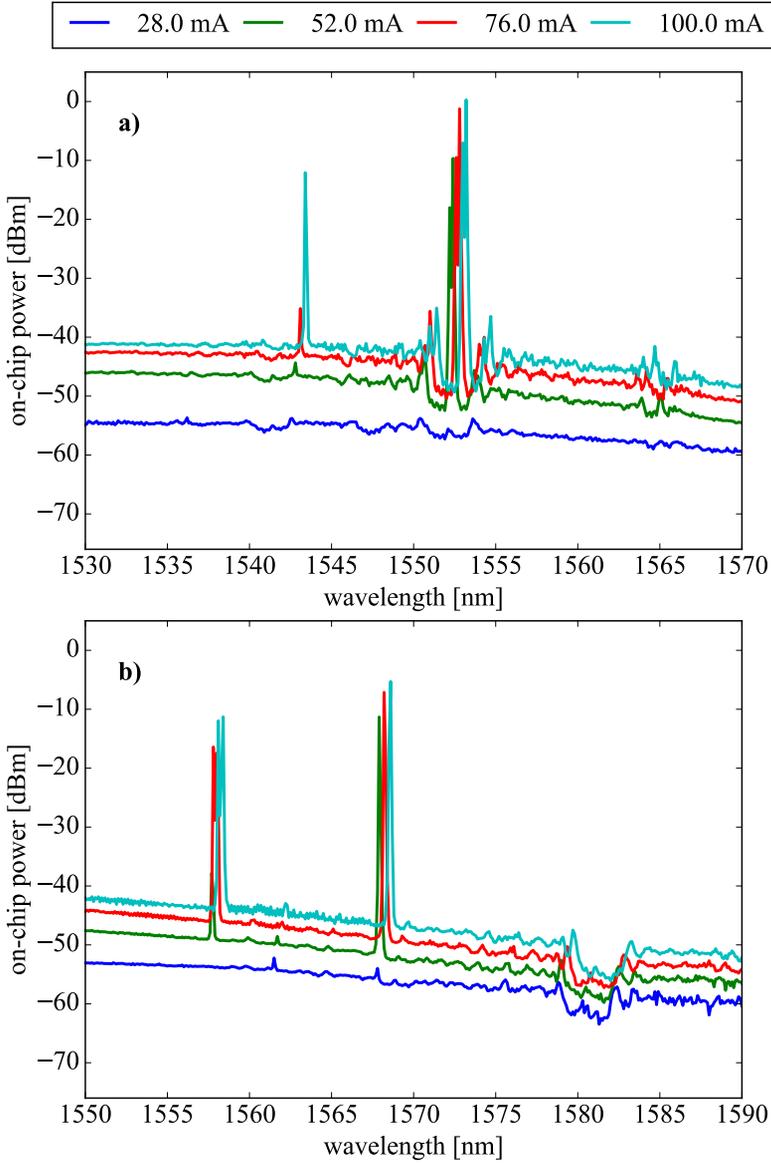


Figure 4.9: Measured spectrum of shallow etch DFB lasers with grating period of (a) 241 nm and (b) 246 nm for various bias currents.

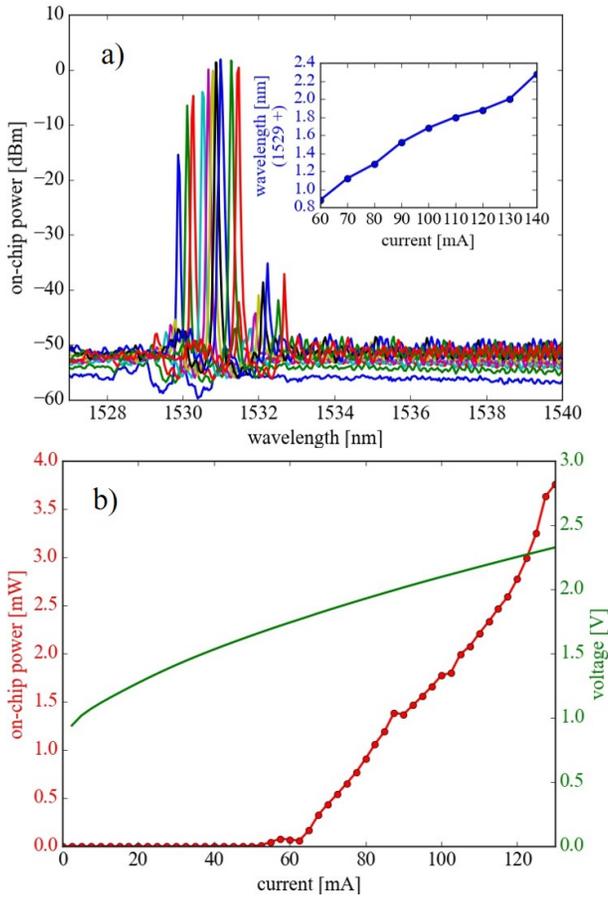


Figure 4.10: (a) Output spectrum at various bias currents, inset illustrates the bias current tuning characteristic of the DFB laser; (b) LI and IV characteristics of the DFB laser.

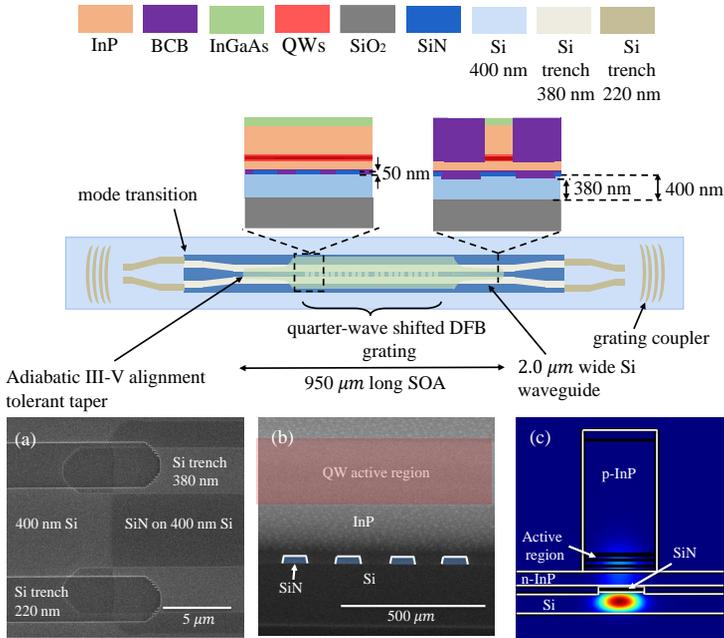


Figure 4.11: Schematic illustrating the design of the DFB laser with cross-section view of the adiabatic taper and the side view of the DFB grating. SEM images of a) mode transition, b) longitudinal cross-section of the DFB grating and c) the mode profile in the gain section are also shown.

the adiabatic taper and can result in a deterioration of the slope efficiency of the DFB laser. However, a 3.0 μm wide Si and III-V waveguide in the gain section supports multiple transverse modes that appear in the output spectrum of the DFB laser. One way to solve this multi-mode problem is to do ion implantation on the edges of III-V mesa during III-V SOA processing, as demonstrated by UCSB, Intel and Aurion [3, 9]. This results in a low resistance path in the center and high resistance path at the edges of the mesa, thus, increasing the overlap of the carriers with the fundamental mode and thereby suppressing higher order modes. However, in this work a different approach has been followed. The etch-depth and the width of the Si waveguide is set to 20 nm and 2.0 μm . This reduces the number of transverse modes in the gain section without adversely affecting the alignment tolerance of the adiabatic taper which is important for micro-transfer-printing of processed SOAs. Moreover, reducing the etch-depth of the Si waveguide to 20 nm in the gain section increases the confinement factor of the optical mode in the Si waveguide which improves the internal loss in the DFB laser. However, this also means that defining the grating in the Si will produce high κ gratings. In order to reduce κ , the grating is patterned on a 50 nm PECVD SiN layer deposited on the top of the Si waveguide. This can lower the internal loss in the DFB cavity without increasing the κL of the grating for the same length of the SOA. The slope efficiency of the DFB laser is inversely proportional to the internal loss for a given κL , therefore, lower internal loss can result in higher slope efficiency. The estimated absorption loss in the III-V/Si waveguide is 21 dB/cm. The simulated κ for 20 nm DVS-BCB thickness is 60.0 cm^{-1} . However, the fabricated DFB laser has a lower value of κ due to variation in the DVS-BCB thickness. The variation in κ with the DVS-BCB thickness is shown in Fig. 4.12 The mode profile is shown in Fig. 4.11(c). The confinement of the mode in the 6 quantum wells is calculated to be 2.1 percent. This is relatively low due to the higher refractive index of the shallow etch Si waveguide in the gain section. Lower confinement factor in QW means high threshold material gain per QW is required for lasing which is proportional to the threshold current density. Therefore, this laser design will have relatively higher threshold current. There are in total two modes in the gain section and the confinement factor of the fundamental mode is higher than the first order mode (1.7 percent in QWs). The SOA micro-transfer printed on the Si waveguide consists of two alignment-tolerant adiabatic tapers, discussed in detail in Chapter 2, that are 225 μm long and a straight gain waveguide section which is 3.2 μm wide and 500 μm long. The adiabatic taper narrows down from 3.2 μm to 0.5 μm width. It is designed to overcome the coupling losses due to the lateral misalignment of the III-V mesa with respect to the silicon waveguide,

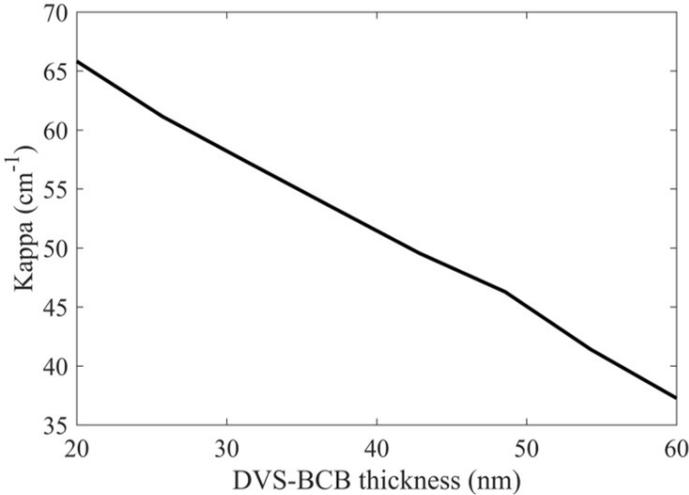
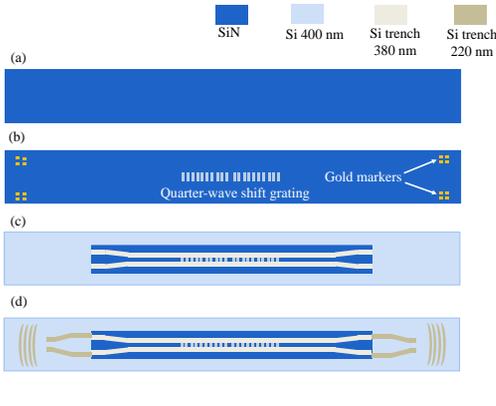


Figure 4.12: DVS-BCB variation with respect to change in κ

inherent to the transfer printing integration method. The calculated coupling loss is 0.2 dB at 0.6 μm misalignment, when micro-transfer-printed on a 2.0 μm wide Si waveguide. The DFB laser is interfaced with a single-mode optical fiber by coupling the optical mode from a 20 nm etch-depth Si waveguide to a 180 nm etch-depth Si waveguide using a mode converter, which is connected to a 180 nm etched grating coupler. The 20 nm etch-depth Si waveguide and 180 nm etch-depth Si waveguide is 5.0 μm wide in the mode converter. The calculated fundamental mode coupling efficiency in the mode converter is 99 percent.

4.4.2 Fabrication

The process flow is similar to the one described in section 4.2.3.1 with an addition of e-beam lithography and optical lithography step to pattern SiN, illustrated in Fig.4.13. As explained in detail in section 4.2.3.1, an SOI sample (400nm thick device layer) of appropriate size is cleaved and the protective resist coating is removed with Acetone, IPA and 10 mins O_2 plasma in a barrel etcher. It is immersed in a 1:1:20 Piranha solution for 10 s and immediately loaded into PECVD for 50 nm mixed-frequency SiN deposition. After the deposition, it is spin coated with ARP-6200.09 e-beam resist and charge reduction layer Electra-92 and baked at 150 $^\circ\text{C}$ and 90 $^\circ\text{C}$, respectively. The sample is then loaded into the e-beam lithography tool for exposure. An exposure dose of 165 $\mu\text{C}/\text{cm}^2$ is used for all the e-beam lithography steps. As shown in Fig.4.13(b), the DFB grating is



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Figure 4.13: DFB with SiN grating process flow: a) SiN deposition, b) patterning of DFB grating and gold marker deposition, c) patterning of 380 nm thick Si trench, d) patterning of 220 nm thick Si trench and grating couplers.

defined first on the SiN in the normal writing mode. The exposed sample is then developed by immersing the sample in water, n-amylacetate and IPA for 30 s, 1 min and 30 s, respectively. The sample is then dried with a nitrogen gun. RIE etching with CF_4 , SF_6 and H_2 is used to etch 50 nm of SiN. The aforementioned etching recipe can also etch the Si underneath with 2:1 SiN to Si selectivity. Therefore, this etch has to be performed in multiple steps and after each step the SiN thickness is measured. After the etching is complete, the gold markers are deposited, for better contrast and alignment, as described in the section 4.2.3.1.

The sample is then prepared by spin-coating ARP-6200.09 e-beam resist and charge reduction layer Electra-92 for the second exposure. In this lithography, the 3.0 μm wide trenches are defined to develop a 2.0 μm Si waveguide, depicted in Fig.4.13 (c). Following e-beam exposure and development, 50 nm SiN and 20 nm Si is etched with RIE. After the waveguide definition, SiN islands are formed with standard i-line contact lithography. Low-resolution photoresist Ti35 is used for this purpose. Finally, the sample is prepared again for another E-beam lithography step. In this step, the 180 nm etched Si trenches and grating couplers are defined with aforementioned development and RIE recipes. This is illustrated in Fig.4.13.

The SOI DFB sample is now complete and is ready for micro-transfer printing. The SEM top-image of the mode transition and the longitudinal cross-section is shown in Fig.4.11(a-b). The micro-transfer-printing process used for the 2nd generation DFB is similar to the one described in section 4.2.4. The only exception in the process is that SiO_x is not de-

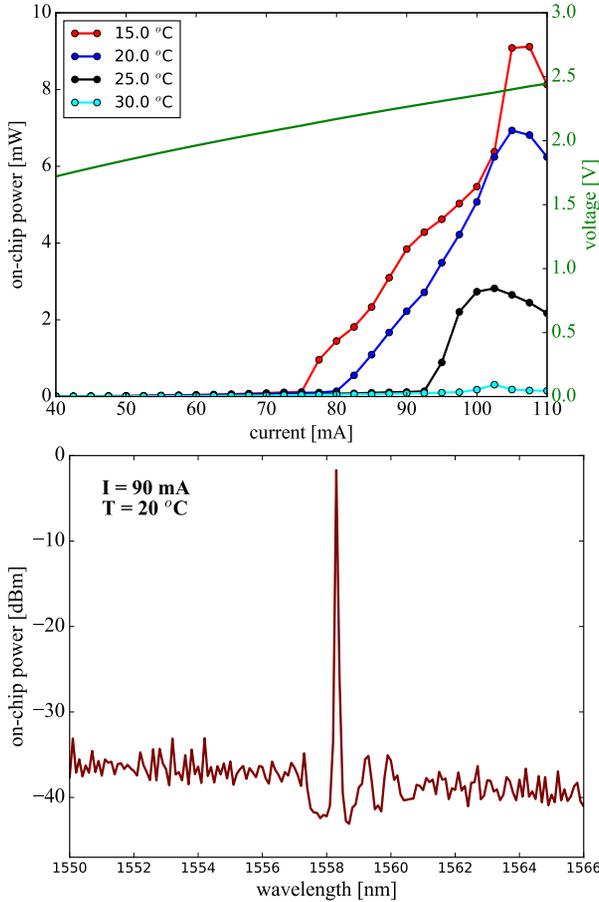


Figure 4.14: (top) Waveguide-coupled output power (single-sided) as a function of bias current for various operating temperatures and the current-voltage characteristic, (bottom) Measured spectrum at 0.05 nm resolution, at 90 mA and at 20 °C operating temperature.

posited on the SOI circuit for this design and 1:4 DVS-BCB-35:Mesitylene is directly spin coated on the sample.

4.4.3 Characterization

The DFB characterized in this work has a 490 μm long grating. The grating period and duty cycle is 242 nm and 50 percent, respectively. The DFB sample is placed on a temperature-controlled stage to characterize it. Single-mode cleaved fibers are used as an optical interface. Optical

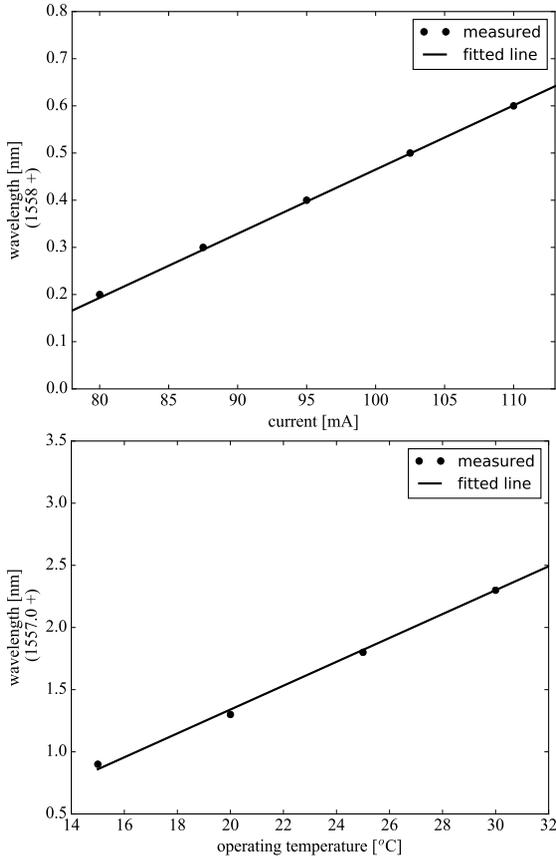


Figure 4.15: DFB output-wavelength-tuning characteristics (top) with changing bias current at 20 °C and (bottom) with changing operating temperature at 90 mA.

power couples through a grating coupler to a single-mode optical fiber which is connected to an optical spectrum analyzer and to an optical power meter. A Keithley 2400 Sourcemeter is used to bias the DFB laser. In order to calculate the on-chip optical power, reference waveguides with waveguide transitions and grating couplers are also fabricated on the same sample. The loss from the grating coupler and the mode transition is calibrated out to calculate the on-chip power. At 1558 nm, the PIC-to-fiber coupling loss is 12.3 dB. This is consistent with the grating coupler loss reported in Ch 3. The differential series resistance of the laser is 8.0 Ω . Figure. 4.14(left) shows the LI curve for the DFB laser at various operating temperatures. Single-side waveguide-coupled optical power of 9.1 mW,

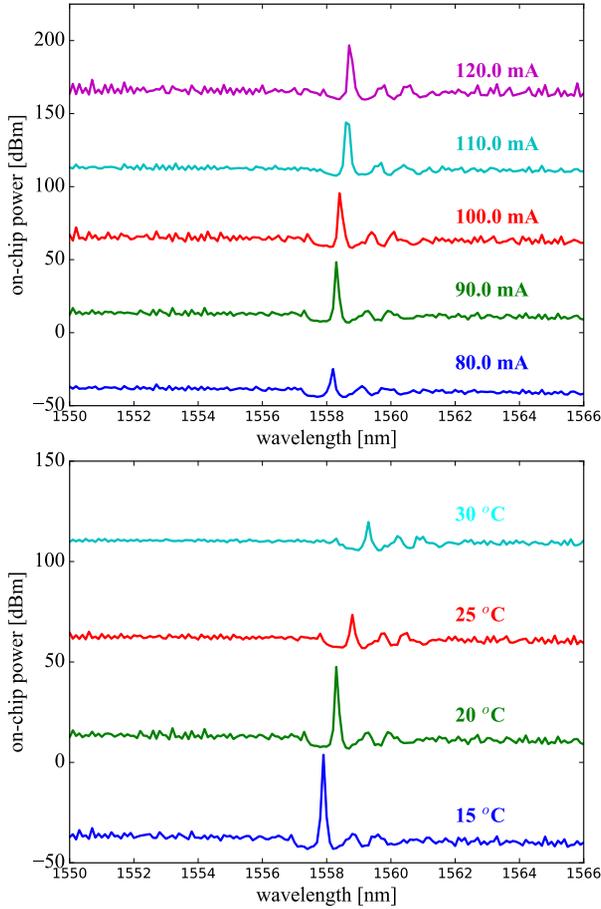


Figure 4.16: Measured laser spectra (top) for various bias currents at 20 °C and (bottom) for various operating temperatures at 90 mA bias current, plotted with a 50 dB offset in the y-direction.

6.9 mW and 2.8 mW are obtained at 15 °C, 20 °C and 25 °C, respectively. The threshold current at 20 °C is 80 mA (3.38 kA/cm²) and increases with the increase in operating temperature. The slope efficiency is calculated to be 0.27 W/A at 20 °C. Single mode operation at 1558.3 nm (resolution of 0.05 nm) with a side mode suppression better than 33 dB is obtained at 90 mA, shown in Fig. 4.14(right). The stop band is 2 nm wide, which corresponds to a κL of 2.6. Figure 4.15(left) shows the tunability of the DFB laser with changing bias current. It tunes up to 0.4 nm when the bias current is varied from 80 mA to 110 mA and has a tuning coefficient of 0.0135 nm/mA. 1.4 nm red shift is obtained in the emission wavelength

when the operating temperature increases from 15 °C to 30 °C, resulting in temperature coefficient of 0.09 nm/°C. The wall-plug efficiency of the laser at 15 °C and 20 °C is 7.2% and 5.6%, respectively. Due to relatively low confinement in the QWs and high thermal impedance, the maximum operating temperature of these lasers is relatively low. However, the thermal impedance of this design can be improved by incorporating thermal vias between the laser and silicon substrate (e.g. using amorphous silicon or metal). Alternatively, the chip can be mounted up-side down on a carrier that also acts as a good heat spreader (i.e. AlN carrier). In the current configuration the DFB laser is supposed to be used under cooled conditions, as the performance is only sufficient till 20 °C.

4.5 Conclusion

In this chapter, we demonstrated DFB lasers by micro-transfer printing SOAs developed in Ch 3. We developed two DFB laser designs. The first DFB design was very simple and had quarter-phase shift DFB grating patterned in a wide Si waveguide. Single-mode operation was observed only at the edge of the gain spectrum with a threshold current of 62 mA and single-sided on-chip output power of 3.75 mW. Features of the second generation DFB design were the shallow-etched waveguide and quarter-wave shift DFB grating defined in PECVD SiN deposited on the top of the Si waveguide. Higher confinement in the Si waveguide resulted in a higher slope efficiency of 0.27 W/A, higher threshold current of 80 mA, wall-plug efficiency of 7.2 % and single-sided output power of 6.9 mW.

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5

Micro-transfer-printed DBR lasers

5.1 Introduction

High-volume and high-throughput integration of semiconductor optical amplifiers (SOAs) and lasers is indispensable for the development of advanced photonic systems-on-chip. Many approaches are in development including pick-and-place of micro-packaged lasers, flip-chip integration, die-to-wafer or wafer-to-wafer bonding, hetero-epitaxial growth, each at a different technology readiness level [1–3]. Micro-transfer printing is an emerging heterogeneous integration technique promising wafer-level integration, versatility in terms of the type of devices that can be integrated in close proximity and flexibility to integrate the devices in a complex silicon photonics (SiPh) platform without altering the generic process flow. [4]

However, this technique has its own challenges. As mentioned before, one of the main challenges in the micro-transfer printing of fully-processed SOAs is the misalignment between the Si and the III-V waveguides. State-of-the-art transfer printing tools provide an alignment accuracy of $\pm 1.5 \mu\text{m}$ (3σ) [4, 5]. The micron-scale accuracy of the transfer printing tool requires good alignment tolerance of the adiabatic taper structure used to couple light from III-V to Si waveguide and vice versa as discussed in Chapter 2. In order to solve this problem, we designed an alignment-tolerant adiabatic taper which can provide high-coupling efficiency for up to $1.0 \mu\text{m}$ misalignment.

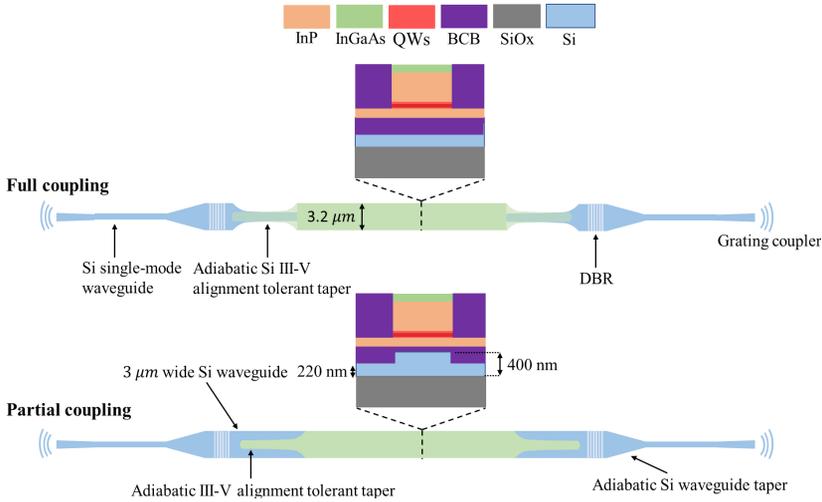


Figure 5.1: a) Design schematic of full-coupling and partial-coupling DBR lasers. The cross-section in the gain section is also illustrated.

In this chapter, the aim is to perform a small-scale study to determine the effect of micro-transfer-printing misalignment on the performance of evanescently coupled heterogeneously integrated devices. For this purpose, DBR lasers are developed by micro-transfer-printing of the SOAs developed in chapter 3, in a FP cavity. The FP cavity is formed with two DBR gratings etched in the Si waveguide. This design allows the coupling loss of the adiabatic alignment-tolerant tapers to directly influence the threshold current of the FP lasers. In order to relate the threshold current with the misalignment, high-resolution microscope images are digitally processed to calculate the misalignment between the SOA and the Si waveguide for each micro-transfer-printed laser.

5.2 Device Design

The design schematic of the DBR lasers is shown in Fig. 5.1. We integrate both full-coupling and partial-coupling III-V/Si structures developed in Chapter 3. The SOAs are 1.1 mm long with 700 μm straight gain section length and two adiabatic tapers at each end. The SOA waveguide width is 3.2 μm in the gain section and it tapers down to 0.5 μm . The full-coupling SOA doesn't have a Si waveguide below the gain section, whereas the partial-coupling SOA has 3.0 μm waveguide underneath the SOA straight waveguide section. For the full-coupling amplifier, the Si waveguide is adi-

abatically tapered from 3.0 μm to 0.2 μm before the SOA straight section. The design of these tapers is extensively discussed in Chapter 2. SOAs are enclosed by identical DBRs with a grating period of 258 nm and have 13 periods. The peak reflection is 72 percent at 1560 nm and the FWHM is 135 nm in reflection spectrum of the DBR. Since the DBRs at both ends are identical we expect same output power on each side. The FSR, which is the longitudinal mode spacing between the adjacent modes in the cavity, can be calculated by [6]:

$$FSR = \frac{\lambda^2}{2n_g L} \quad (5.1)$$

where L is the cavity length and n_g is the group index of the optical mode. The cavity length is the sum of the active and passive region length which is 1.31 mm. The grating is only 3.0 μm long and, therefore, can be ignored for the calculation of FSR. However, for longer gratings the effective grating length should be taken into account and is approximated by [6]:

$$L_{\text{eff}} = \frac{1}{2\kappa} \tanh(\kappa L_g) \quad (5.2)$$

where κ is the coupling strength and L_g is the length of the grating. The calculated FSR is 0.24 nm and the 3-dB gain bandwidth of the SOA measured in chapter 3 is 30 nm. Therefore, several longitudinal modes will have similar threshold modal gain and the output spectrum will have multiple modes. Nevertheless, our focus here is to study the effect of micro-transfer printing on the laser threshold and not to make a single-mode DBR laser. However, the requirements for a single-mode DBR laser design will be discussed in the next section.

5.2.1 Single-mode DBR laser design

The single-mode DBR laser design involves a narrow band DBR such that a single longitudinal mode can be filtered from the gain spectrum. This means that the bandwidth of the DBR should be less than the spacing of the longitudinal modes the cavity. The null bandwidth (that is the spacing between first zeros in the reflection spectrum of the DBR) can be calculated by [6]:

$$BW = \frac{\lambda_B^2}{\pi n_g} \sqrt{\kappa^2 + \frac{\pi^2}{L_g^2}} \quad (5.3)$$

A design of a narrow band and highly reflective DBR requires low coupling strength κ , and low waveguide loss. The first null bandwidth is plotted

against κL in Fig.5.2(top) and the corresponding FSR of the cavity is plotted for various grating lengths when κL equals 3 (assuming an SOA length of 1mm). It can be seen that longer grating lengths are required to fulfil the design criterium:

$$FSR > BW \quad (5.4)$$

for a highly reflective DBR (eg. $\kappa L = 3$). Equation 5.4 can be simplified for highly reflective DBR into:

$$L_g > 5.1 L_a \quad (5.5)$$

that is the length of the grating should be at least five times the length of the active region. This can also be observed from Fig. 5.2. In the FSR calculation, the length of the active region is chosen to be 1 mm. Thus, for a 5 mm grating length and κL equals 3, the FSR is equal to the null bandwidth of the grating. It is important to state that longer grating lengths also means high mirror loss because of the waveguide propagation loss, shown in Fig. 5.3 The fabrication of low-loss and several mm long grating is challenging with e-beam lithography because of stitching errors at the field boundaries and the higher waveguide loss.

5.3 Fabrication

The goal is to study the effect of micro-transfer printing pre-processed SOAs on the performance of the laser. The fabrication process of SOAs/silicon waveguides and micro-transfer printing is extensively described in Chapter 2. A similar process is used to develop DBR lasers. Figure 5.4 shows the SEM images of the fabricated devices. A Zoomed-in top image of the fabricated DBR is illustrated in Fig. 5.4(a), 3.0 μm wide Si waveguide in the gain section is depicted in Fig. 5.4(b), a cross-section taken in the gain section of the full-coupling DBR laser is shown in Fig. 5.4(c) and a top image after contact metal deposition of the laser is shown in Fig. 5.4(d).

5.3.1 Micro-transfer-printing process

To assess the effect of micro-transfer printing on the performance of the DBR laser, 20 identical SOA coupons are micro-transfer-printed individually on the SOI circuit, 10 representing each design (full coupling and partial coupling). The SOI sample is spin coated with DVS-BCB:mesitylene 1:4 prior to micro-transfer printing and no other spacer layer is deposited. Pattern recognition is used to align the fully-processed SOA with the Si

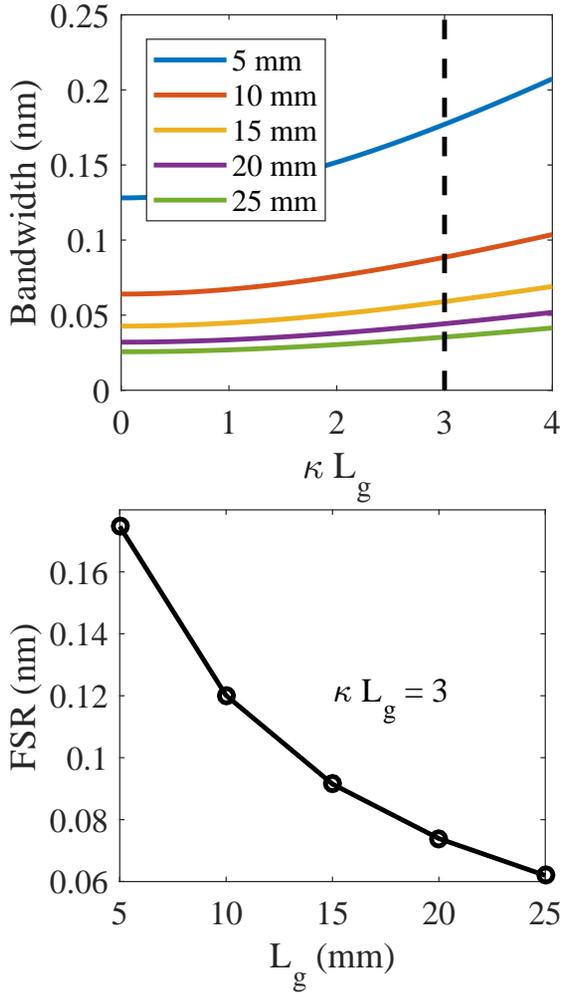


Figure 5.2: (top) Null bandwidth of the DBR is plotted against κL_g for different grating lengths, (bottom) The FSR of the FP cavity (assuming a 1mm long SOA) for different lengths of the highly reflective grating.

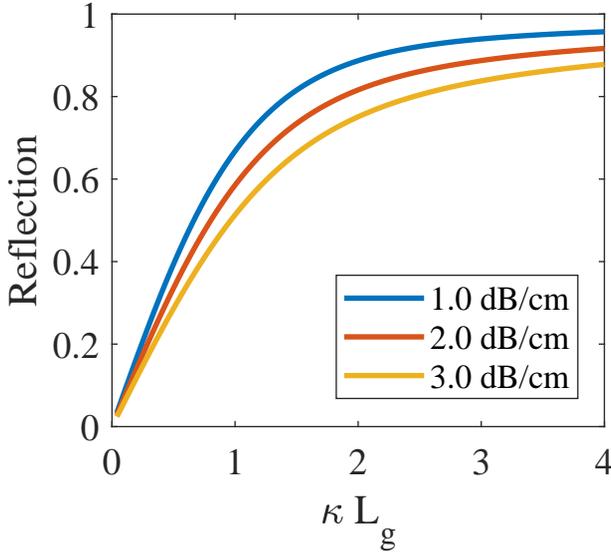


Figure 5.3: Fraction of power reflected is plotted against the grating strength for several values of waveguide loss.

waveguide circuit as described in Chapter 3. Figure 5.5 shows the microscope images of InP SOA source and target die. SOA coupons are fabricated in dense arrays on the InP die illustrated in Fig. 5.5(b). These coupons are then printed individually on the Si waveguide circuit. Images of a printed coupon on the Si waveguide and after etching of the n-metal vias are shown in Fig. 5.5(c-d). The array of DBR lasers fabricated are shown in Fig.5.6. There are in total 20 devices. In the next section, the characterization of these DBR lasers will be discussed.

5.4 Device characterization

A similar experimental setup as in Chapter 3 is used to characterize the DBR lasers. The III-V-on-silicon PIC is placed on a temperature-controlled stage for the measurements and kept at 20 °C. The PIC is optically probed with cleaved standard single mode fibers using a fiber stage. Grating couplers are used to interface with the optical fibers. To calibrate out the grating coupler response, reference passive silicon waveguides are also fabricated on the III-V-on-silicon PIC and they undergo the same processing steps as the grating couplers used for interfacing with the DBR laser. The DBR laser is electrically probed with needles and is biased through a Keithley 2400

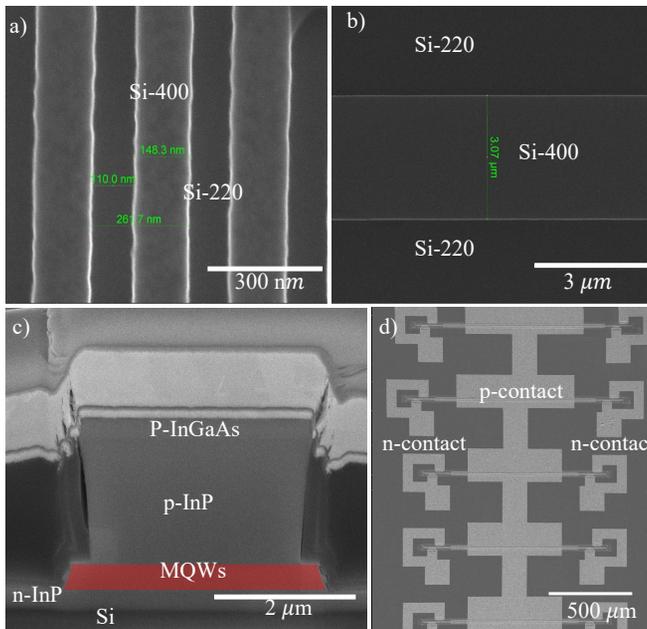


Figure 5.4: SEM images of the fabricated lasers: (a) Zoomed-in images of the DBR, (b) Si waveguide in the gain section for the partial coupling design, (c) Cross-section of the laser in the gain section for the full-coupling design and (d) Final look after contact metal deposition.

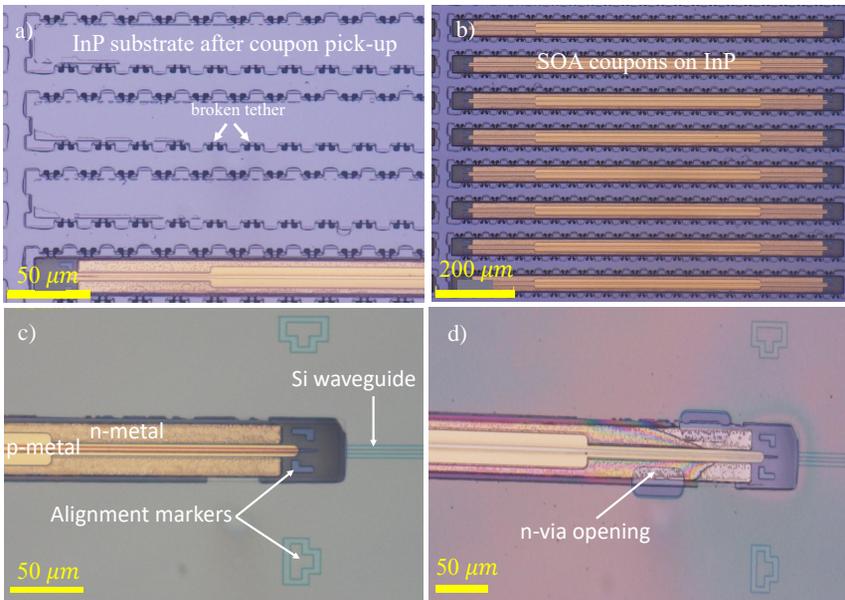


Figure 5.5: a) Image of the InP die after coupons have been picked for micro-transfer printing, b) array of SOA coupons fabricated on the InP die, c) Micro-transfer printed SOA coupon on a Si waveguide and d) opening of n-vias for n-metal deposition.

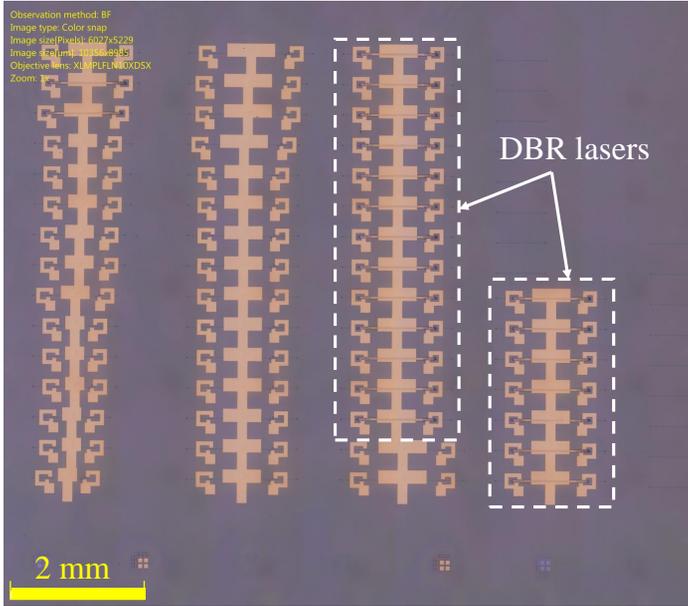


Figure 5.6: Array of DBR lasers on the III-V-on-silicon die.

source meter. Current-voltage characteristics for full-coupling and partial-coupling designs are illustrated in Fig.5.7. The I-V curves are nominally the same and the mean series resistance at 80 mA is 10Ω . This indicates similar DC electrical characteristics of all the micro-transfer-printed III-V SOA coupons. In order to compare the optical characteristics of the DBR lasers, the bias current is varied and the optical power coupled into the fiber is measured with an HP powermeter.

Figure 5.8 shows that the maximum single-sided on-chip output power varies between 0.1 mW to 1 mW and 0.18 mW to 0.6 mW for the partial-coupling and full-coupling design, respectively. Mean threshold current I_{th} is 60 mA and standard deviation is 5 mA for partial-coupling design. On the other hand, for the full-coupling design the mean I_{th} is 51 mA and standard deviation is 3 mA. In the case of partial coupling devices larger spread in the slope efficiency and threshold current can be attributed to the change in the confinement factor in the III-V waveguide due to the lateral misalignment of SOA and Si waveguide underneath. Micro-transfer-printing the SOA introduces an extra loss in the laser cavity due to the lateral misalignment of the III-V and Si waveguides. This extra loss can increase the modal threshold gain and hence the threshold current of the laser. However, to find the correlation between the misalignment and the threshold current,

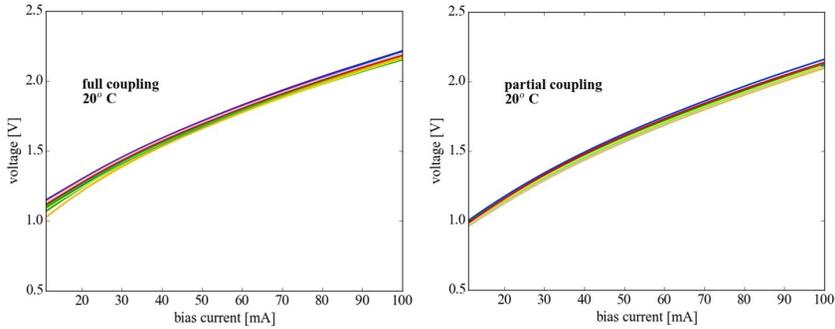


Figure 5.7: Voltage versus bias current for (left) full-coupling design and (right) partial-coupling design.

the misalignment has to be measured. In the next section we will discuss the procedure employed to measure the misalignment.

5.5 Misalignment measurement

In order to align the markers on the coupons and the markers on the target site, the micro-transfer-printing tool camera takes two images focused on the coupon markers and target markers, respectively. The images are then processed to calculate the center of the markers on the coupon and on the target. Once the x-y coordinates of the the markers center are known the displacement in the x and y direction is calculated. A similar procedure is used here to capture the images of the III-V and Si waveguides with the high-resolution Olympus DSX-500 microscope. It is possible to take a 1194x1194 pixel image representing a physical size of 51x51 μm with the Olympus DSX-500 microscope. This means that each pixel equals 42.7nm in the images. Figure 5.9 depicts the images captured with the Olympus DSX-500 microscope at 10x magnification while focusing on III-V and Si waveguide, respectively. The captured images are processed by a python script that uses an open source library called OpenCV. The first step is to crop the III-V waveguide part from the III-V waveguide focused image and the Si waveguide from the Si waveguide focused image, respectively. The cropped images are then converted into binary form with an edge detection function that assigns value of (255, 255, 255) to the pixels representing edges of the objects and 0 elsewhere, shown in Fig. 5.10. The set (255, 255, 255) is the 'rbg' color code for white and (0,0,0) is the color code for black. In simpler words, the edge detection assigns value of (255, 255, 255) to edges that are within a certain threshold. Therefore, depending on

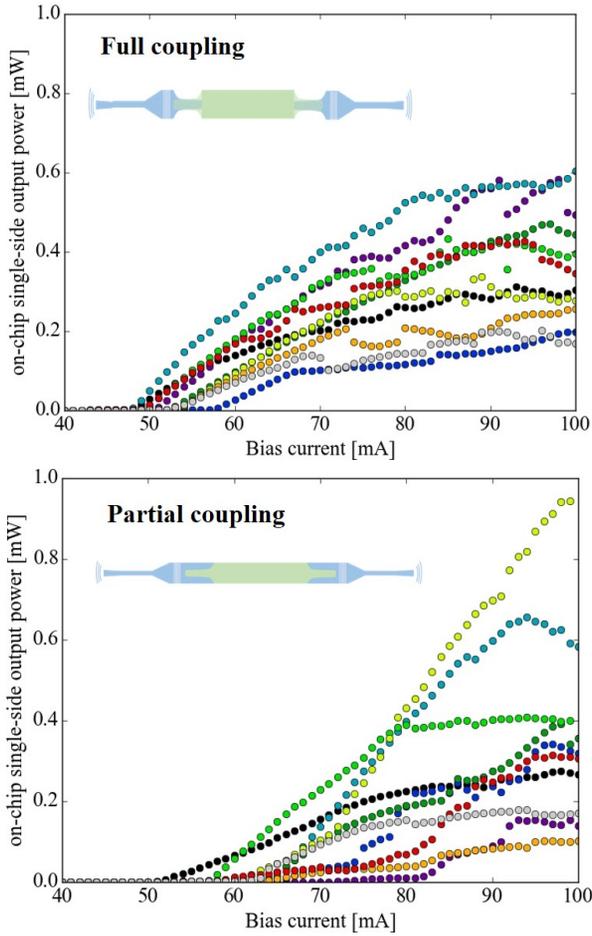


Figure 5.8: Single-sided on-chip output power plotted against bias current for (top) full-coupling and (bottom) partial-coupling design.

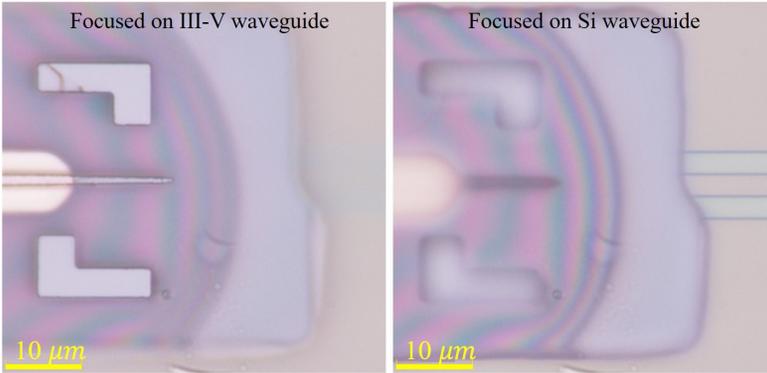


Figure 5.9: 10x magnification microscope images of III-V and Si waveguide.

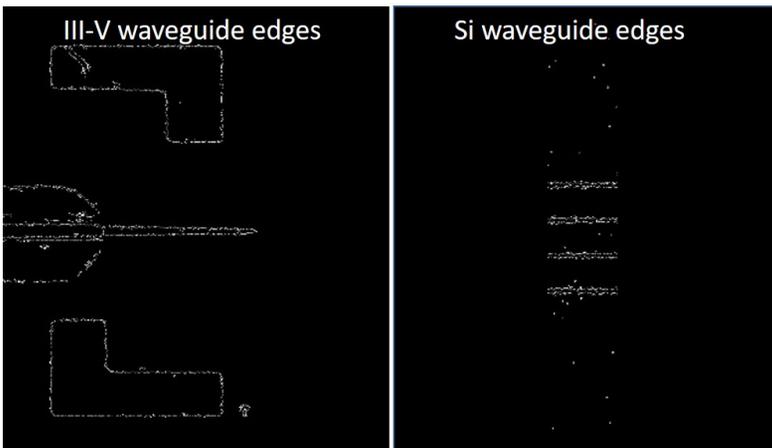


Figure 5.10: III-V and Si waveguide image after edge detection.

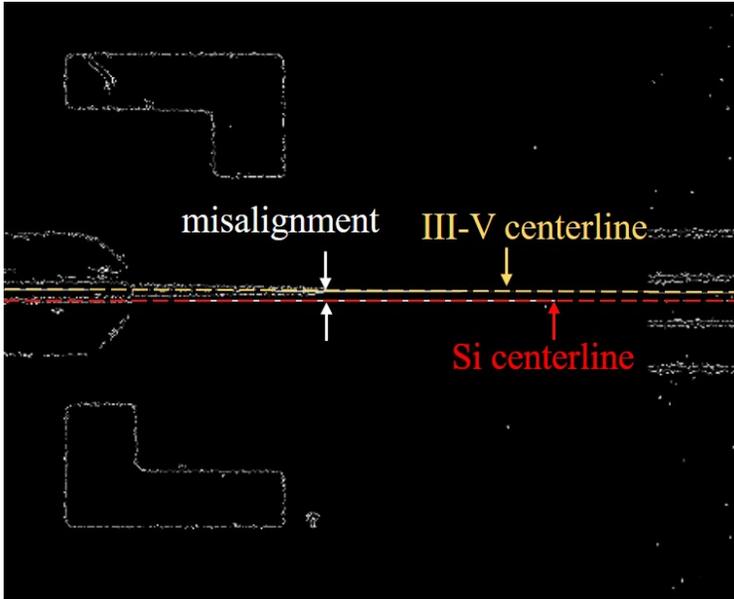


Figure 5.11: III-V and Si waveguide image with center lines and misalignment labeled.

the lighting, the quality of the image and the sharpness of the edges, the threshold range needs to be modified for images with different aforementioned characteristics. However, in our case all the images were taken with the same microscope settings and thus similar threshold values could be used for all the devices for edge detection. The next step is to replace the original images with their binary counterparts and stitch them together. The stitched image can now be utilized to calculate center points of the III-V and Si waveguides. To simplify the script, the range of rows and columns that enclose the III-V waveguide are manually entered into the code. These rows and columns are raster scanned to find the pixels that are exactly in the middle of the pixels at the edges and are assigned the value of (255, 255, 255) so that they appear white in the image. Moreover, the x and y location of all these aforementioned pixels are stored in an array. Next, a linear fit on the x and y locations in the image is carried out and a best fit line bisecting the III-V waveguide is drawn in the image. It is much easier to calculate the center point of the III-V waveguide because of the sharp image and less noisy edge detection, because of the gold cladding which enhances the contrast. In the case of the Si waveguide the edges are more noisy, hence a slightly different approach was applied.

As seen in Fig. 5.10, each boundary is represented by two white dotted

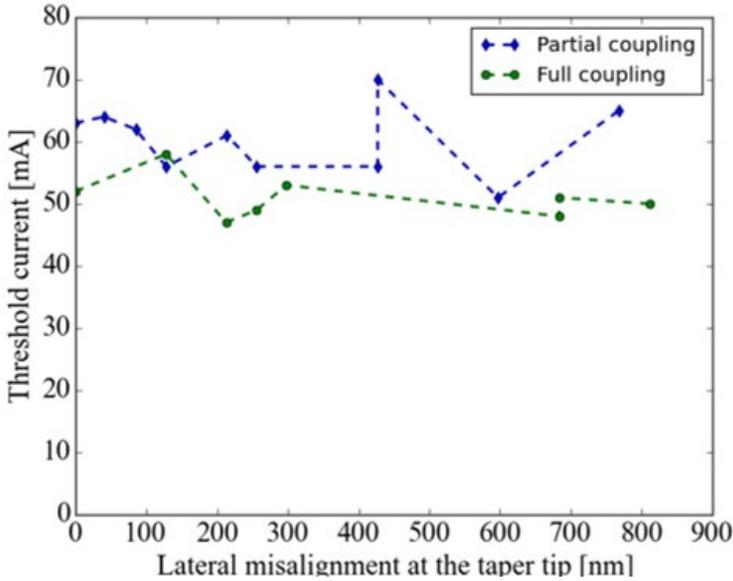


Figure 5.12: DBR lasers threshold current plotted against the lateral misalignment between III-V and Si waveguide.

lines and there are four boundaries in total in the Si waveguide binary image. In order to minimize the error, a linear polynomial is fitted to all the white dotted lines and the equation of these eight lines is used to calculate the equation of the center line. Figure 5.11 depicts the final image with the calculated center lines and the misalignment between the waveguides at the taper tip of the III-V waveguide. It is important to mention here that the indicated misalignment is at the opposite side of the coupon where the alignment through pattern recognition was performed in the transfer-printing tool. Therefore, these misalignment values are the worst between the two ends of the SOA. The misalignment measurement process is summarized in Fig. 5.13. The misalignment was measured for all the micro-transfer-printed DBR lasers and plotted against the threshold current as shown in Fig. 5.12. The calculated misalignment and the threshold current has no correlation.

5.6 Conclusion

In this chapter, we demonstrated arrays of micro-transfer-printed III-V-on-Si DBR lasers. We studied two different III-V/Si SOA designs: full-coupling and partial-coupling. The maximum single-sided on-chip output

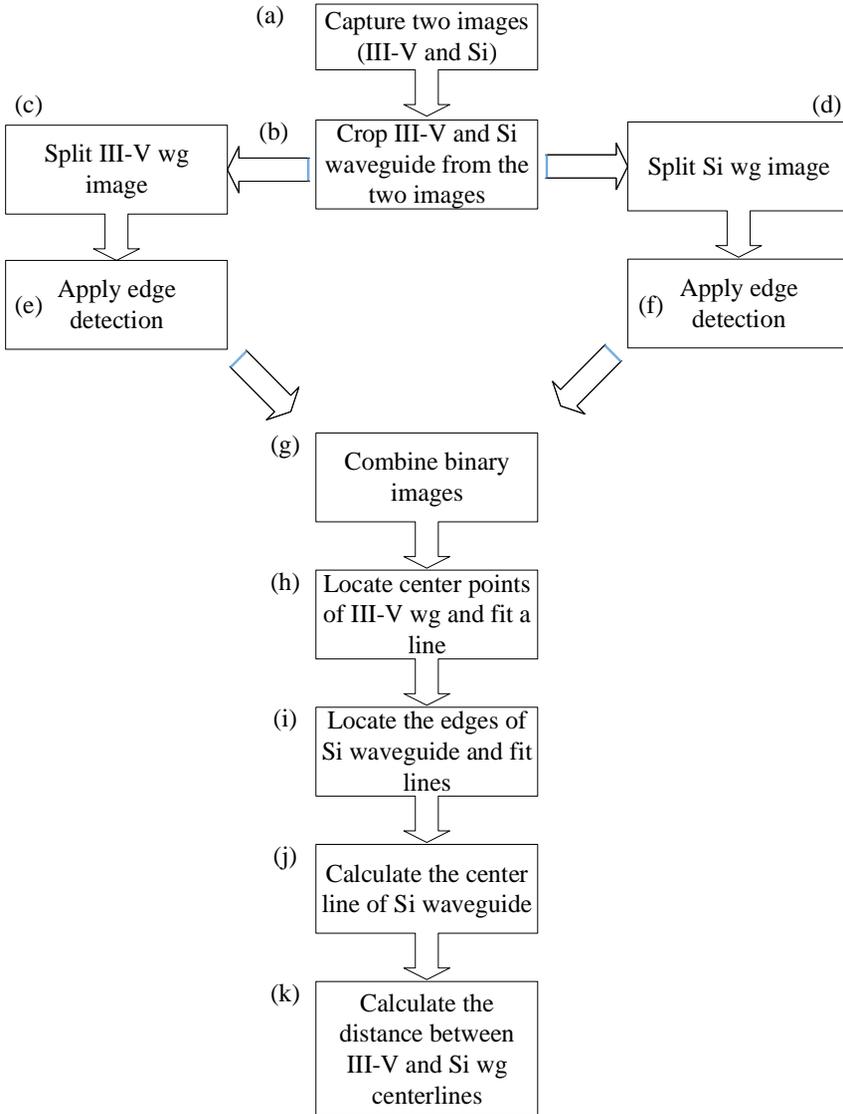


Figure 5.13: Process flow chart of misalignment measurement from the microscope images of micro-transfer printed SOAs.

power varied between 0.1 mW to 1 mW and 0.18 mW to 0.6 mW for the partial-coupling and full-coupling design, respectively. The mean threshold current I_{th} is 60 mA and the standard deviation is 5 mA for partial-coupling design. On the other hand, for the full-coupling design the mean I_{th} is 51 mA and the standard deviation is 3 mA. To investigate the effect of micro-transfer-printing SOAs on the performance of the lasers, we developed a methodology to measure misalignment of the micro-transfer-printed SOAs using microscope images. We found no correlation in the threshold current and the misalignment of III-V and Si waveguides (all below 1.0 μm).

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6

Conclusions and outlook

6.1 Conclusion

Throughout this book, we have highlighted the importance and applications of photonic integrated circuits. Photonics is in the list of disruptive technologies that will enable high-tech products in the future such as autonomous vehicles, quantum computers, mixed reality goggles/headsets etc. Furthermore, the benefits of heterogeneous integration such as integrating III-V semiconductor materials on Si has also been highlighted. We discussed that there is a need for a technology that can enable the integration of devices realized in other material platforms such as III-V materials, lithium niobate etc. on silicon photonic integrated circuits. Micro-transfer-printing of pre-processed devices is a powerful and enriching integration approach. It allows the integration of devices from multiple material systems to be integrated in close proximity. In this work, we mainly focused on developing micro-transfer-printing technology for integrating processed III-V semiconductor optical amplifiers (SOAs) on Si waveguide circuits. One of the challenges we circumvented was the coupling loss introduced by the micro-transfer-printing process due to the lateral misalignment between the devices. We developed an adiabatic alignment-tolerant taper that enabled high coupling efficiency up to $1.0\ \mu\text{m}$ of lateral misalignment. Furthermore, we developed the process and the design of SOA coupons that enable good micro-transfer-printing yield. The performance of the SOAs

demonstrated was comparable to more mature heterogeneous integration techniques such die-to-wafer bonding.

The development of high-performance micro-transfer-printable SOAs is a major milestone. These SOAs were micro-transfer printed not on just Si waveguide circuits but also on SiN waveguide circuits in the context of other PhD projects. By utilizing these SOAs, we developed DFB lasers and also investigated the effect of micro-transfer-printing on the performance of DBR lasers, particularly their threshold current.

6.2 Outlook

In this work, the foundation of micro-transfer printing pre-processed SOA coupons was laid. However, there is still a lot of work that is to be done to make such micro-transfer printed devices relevant for the industry.

1. **Improvement in coupon design:** In this work, coupons were encapsulated and held by resist tethers during the release process. However, in parallel in the micro-transfer-printing team SiN was also investigated to be used as tethers. SiN is a more stable material and can therefore produce more reliable released coupons (e.g. extending the shelf lifetime of suspended coupons). Furthermore, the coupons developed in this work required metal deposition for electrical contacting. Therefore, it is worth developing a coupon design with contact pads present on the device. This means that there would not be any post-processing required after micro-transfer-printing.
2. **Wafer-level array printing of SOAs:** The SOAs in this work have been micro-transfer-printed individually with a single-post stamp. However, one of the main advantages of micro-transfer printing is the wafer level array printing with multi-post stamps. When micro-transfer-printing arrays of devices, misalignment can be higher compared to printing devices individually. However, this needs to be further investigated. Additionally, the limit on the number of SOAs that can be micro-transfer printed with good alignment in a single print is yet to be found. First results indicate that the alignment within an array (of 15 devices) varies $\pm 0.5 \mu\text{m}$.
3. **Integration on complex Si/SiN foundry platforms** One of many advantages of micro-transfer printing is the ability to integrate processed SOAs on open access foundry platforms without changing their process flow. Potentially, this can lead to the development of

state-of-the-art high-performance photonic systems-on-chip. For example, integrating lasers by micro-transfer-printing SOAs on the imec iSIPP50G platform can allow us to develop high-speed next generation transceivers for data center applications. Similarly, integrating SOAs on a low-loss SiN platform is particularly useful in developing high-power and narrow line-width lasers that can be utilized for sensing applications.

4. **Integration of devices from various material systems:** Because of its modular nature, micro-transfer printing is an enriching integration technique. It enables the integration of the best-in-class devices from various material systems on the same Si / SiN photonic chip, e.g. the integration of SiN low-loss waveguides with Lithium niobate modulators and III-V-on-Si lasers altogether on a single-chip. This is particularly very exciting as state-of-the-art photonic systems-on-chip can this way be demonstrated using micro-transfer printing technology.

