Novel Geometry For An Integrated Channel Selector

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Abstract—A new reflective configuration for a monolithically integrated channel selector with power monitor is proposed. One star coupler, one arrayed waveguide grating, and a minimum number of SOA gates are used to achieve loss free transmission. A 32-channel device controlled by only 12 SOA-gates is realized in InP. Low on-chip losses result in strongly reduced bias currents and an improved signal to noise ratio compared to previously demonstrated devices. The use of SOAs allows for switching on a nanosecond time scale.

Index Terms—Arrayed waveguide grating, channel selector, InP, monolithic integration, tunable optical filter, WDM.

I. INTRODUCTION

THE efficient management of the optical channels in a WDM system requires wavelength-selective devices to operate on a single channel or on a subset of channels. A channel selector is a tunable drop filter that can extract one or a few channels from the WDM transmission line while blocking the others. This function is of fundamental importance in many transmission systems, especially for those with an architecture based on a broadcast-and-select scheme.

Channel selectors have been implemented in several forms and were fabricated mainly in silica [1], hybrid integrated [2], and with semiconductor technology [3][4][5]. So far only the latter has been able to provide fast switching, compactness, and loss free operation. The first InP-based channel selectors were realized by monolithically integrating a demultiplexer, an array of SOA gates, and a multiplexer in devices with up to 16 channels [3]. However, this approach requires one SOA per channel; the size of the device scales approximately linearly with the channel count while the fabrication yield rapidly drops. In [6], an alternative design using two AWGs and a power combiner was proposed. This geometry reduced the total number of gates to $2\sqrt{N}$ where *N* is the total number of channels.

Here, we demonstrate a novel approach, using a single AWG and a power splitter. As in [6], the number of gates scales proportionally to the square root of N. Further, the device works in a reflective mode and requires only one fiberchip connection, which makes the characterization and the packaging much easier. A 32-channel device is implemented in InP and loss free operation is achieved.

II. PRINCIPLE OF OPERATION

Our channel selector consists of a passive power splitter followed by an arrayed waveguide grating (AWG) whose input and output ports are controlled by optical shutters. After the shutters at the AWG's output side, the waveguides are terminated with a mirror in order to operate in a reflective mode as shown in Fig. 1. The device works as follows: The power of the incoming optical channels λ_k (k=1..N) is evenly split into P replicas by a $1 \times P$ power divider. These are connected, each one through a shutter, to the P AWG's input ports. By setting only one input shutter in the through state, we select the insert location into the AWG and only a subset of Q channels shall be diffracted into the output ports. The channel subsets are unique for each input port so that the union of the possible subsets contains all N channels. The output shutters decide whether the light should be stopped or allowed to continue to the back reflector. If only one shutter is in the through state, only one optical channel will propagate till the reflector and will then retrace its path back to the input of the device. The selected channel can be separated from the incident traffic by means of a circulator.



Fig. 1 Scheme of the channel selector.

By the proper choice of the pair of gates set in the through state, any optical channel can be independently selected from the others. The selectivity properties of the device arise from the wavelength routing characteristics of the AWG. For *N* optical channels λ_k (*k*=1..*N*), *P* and *Q* can be chosen so that there is unique input-output combination that allows transmitting each λ_k from one side of the AWG to the other. This is achieved by fulfilling

$$N \le N^+ \le P \times Q \tag{1}$$

where

$$N^* = \frac{Max\{\lambda_k\} - Min\{\lambda_k\}}{LCF\{\lambda_j - \lambda_l\}} + 1 \quad \forall k, j, l = 1...N$$
⁽²⁾

The function *Max* (*Min*) denotes the maximum (minimum) value of λ_k (*k*=1..*N*), and the *LCF* is the largest common factor among the differences $(\lambda_j - \lambda_l)$ for j, l = 1..N. For evenly spaced λ_k , we have $N=N^*$. The solution that minimizes the number of shutters and reduces the device's size is the one that minimizes P+Q and it can be easily proven that in such a case P+Q grows approximately as $2\sqrt{N^*}$. Once *P* and *Q* are determined, the geometric position of the AWG's input and output ports is calculated as described in [7]. An example of wavelength mapping is given in Table I for a 32-channel selector based on a 4×8 AWG. Obviously, the power loss at the power splitter is minimized by selecting $P \leq Q$.

TABLE 1. EXAMPLE OF CHANNEL MAPPING IN A 4×8 AWG

k	11	12	13	14	19	20	21	22
6	1	2	3	4	9	10	11	12
10	5	6	7	8	13	14	15	16
22	17	18	19	20	21	22	23	24
26	25	26	27	28	29	30	31	32

The channel mapping between the 4 input (vertical) and the 8 output (horizontal) ports is given for the index k (λ_k , k=1..32). The port numbering corresponds to the case shown in Fig. 2a.

In our configuration the AWG operates without using its periodic frequency response (or wrap-around), therefore it guarantees a better matching between the position of the filter passband and the ITU frequency grid [8]. As we shall motivate in the following, this approach intrinsically offers more homogeneous losses compared to other approaches [6].

The reflective configuration requires a double path through the AWG and the power splitter resulting in the double filtering of the AWG-induced cross-talk. On the other hand, additional losses are expected mainly due to the double transit through the power splitter. Note that the current configuration can also be unfolded by merging the AWG's output ports, after the shutters, into a power combiner.

III. IMPLEMENTATION

A monolithically integrated 32-channel selector was realized in InP. The 32×32 AWG was designed to support 32 optical channels arranged on a 100 GHz frequency grid. The two star couplers, whose radius is 1.60mm, are connected by 72 grating arms with an increasing path length difference of 25.7 μ m. The grating operates at a diffraction order *m*=54 corresponding to a free spectral range of 3.2 THz. Each channel can be selectively transmitted through the device by using only 4 input ports, placed at the virtual positions 6,16,22,26, and 8 output ports located at positions 11-14 and 19-22, as schematically shown in Fig. 2a. Note that only the central 2/3 of the Brillouin zone [9] is used, therefore an excellent loss uniformity is guaranteed.

The power splitting needed to feed the AWG's input ports is provided by a 2×4 star coupler [10] with radius 75.8 μ m and the input/output waveguides spaced by 3 μ m. Waveguide segmentation is used to reduce the excess loss and improve the power uniformity of the star coupler [11]. One of the access ports of the star coupler is used as the input/output port of the channel selector. The second port is connected to an active section, which serves as a power monitor as shown in Fig. 2b.



Fig. 2 (a) Schematic positioning of the input and output waveguides in a 4×8 AWG. (b) Schematic detail of the star coupler with the power monitor.

Semiconductor optical amplifiers (SOA) are used for the optical shutters because they provide both excellent extinction ratios and gain in the through state, thereby facilitating loss free operation. Furthermore, they can operate as power monitors when reverse biased.

The integration technology has been previously described in detail in [12]. The wafer is grown by low pressure-MOCVD and consists of a stack of a graded InGaAsP slab layer $(\lambda_g=0.97\mu m \text{ to } \lambda_g=1.3\mu m)$, a 105nm thick rib layer $(\lambda_g=1.3\mu m)$ and an active layer with 4 tensile strained InGaAsP quantum well layers separated by compressive strained ($\lambda_{p}=1.30\mu m$) barrier layers. In a first step, the active layer is removed everywhere except for the area that will be occupied by the shutters and the power monitor. Subsequently, the passive waveguides (AWG, star coupler and access waveguides) and the SOA mesa are etched. This is followed by the overgrowth of a current blocking layer, an isolation step, a second overgrowth, and a metallisation step. All SOAs are 950µm long and the minimum waveguide bend radius is 650µm. The access waveguide at the facet is angled by 7 degrees to suppress reflections but no AR-coating had been applied at the time of characterisation. The final device size is 13mm×5mm. The back reflector consists of a high-reflective coating applied to the end facet of the device.

IV. RESULTS

The peak transmittance through the device has been measured for all 32 channels separately, using an input power of -15dBm (fiber power). By driving the shutters at the input and output of the AWG with currents between 45mA and 55mA, thirty channels showed at least 2.5dB gain. The two remaining channels reached 0dB fiber-to-fiber gain but needed somewhat higher drive currents. The results are shown in Fig.

3 for TE polarized light and include a 2.2dB loss due to the circulator. For our current application, there was no need to correct for the grating birefringence ($\Delta\lambda_{\text{TE-TM}} = 5$ nm) and the polarization dependent gain in the SOAs. Nevertheless, such polarization dependence can be eliminated by proper design and device processing (e.g. see [5]). The passive waveguide loss is 1.5dB/cm and the excess loss of the AWG is estimated to be approx. 4.5dB. Because of this low on-chip loss, no booster amplifier is needed to further amplify the output power, resulting in a very good suppression of the out-of-band ASE-noise (>40dB).



Fig. 3 Fiber-to-fiber transmission of the 32-channel selector for TE polarized light measured with a resolution bandwidth of 0.1 nm.

Although the access waveguide is angled at the facet, the residual reflections are high enough to start laser oscillations for some channels at drive currents as low as 50mA per amplifier. This limits the drive currents and thus the total fiber-to-fiber gain. With an AR-coating at the input facet the reflections shall be further reduced, thereby not only allowing for higher drive currents but also reducing the Fresnel losses at the fiber interface by approx. 3dB.

Fig. 4 shows the performance of the on-chip monitor for a typical channel. The power measured at the output of the circulator is compared with the values obtained from the power monitor for a reverse bias voltage of -3V. The curves show the signal power without ASE noise. This is done by measuring the output power with an optical spectrum analyzer and calibrating the power monitor by subtracting the current generated by the ASE noise in the absence of the signal. Fig. 4 also gives an estimate of the level of the saturation power for different bias conditions. When the SOAs at the input and at the output of the AWG are driven with I_1 =66mA and I_2 =48mA respectively, the saturation input power for the device gain is -20dBm. By increasing I_2 to 58mA, the saturation input power increases to almost -15dBm. As mentioned before, an ARcoating at the input facet will allow increasing the drive

currents and therefore we anticipate the saturation power to increase further. In a future device, the quantum well active layer might be replaced by a bulk active layer, which is expected to have a higher saturation output power [13].

The dynamics of the SOA gates were measured by driving the gates with sharp current pulses and, depending on the bias currents, response times between 5ns and 10ns were observed. Therefore, we estimate the switching time of the channel selector to be on the same nanosecond scale, consistently with previously published results [14][15].



Fig. 4 Output power vs. input power for a selected channel of the 32-channel tunable filter for TE polarized light measured with an optical spectrum analyzer (closed symbols) and using the on-chip monitor for a reverse bias voltage of -3V (open symbols).

V. CONCLUSION

We have proposed a novel scheme for a *N*-channel digitally tunable filter in InP with a monolithically integrated power monitor. A minimum number ($\sim 2\sqrt{N}$) of fast switching SOA gates in combination with a single *N*×*N* AWG have been used to achieve the desired wavelength selectivity. We fabricated a 32-channel device in which we could show an average gain of 2.5dB per channel. The low losses allowed operating the SOA gates at drive currents of typically 50mA only. The SOAs showed response times in the nanosecond range.

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