Integration of InP/InGaAsP photodetectors onto silicon-on-insulator waveguide circuits

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Abstract: The integration of optical functionalities on a chip has been a long standing goal in the optical community. Given the call for more integration, Silicon-on-Insulator (SOI) is a material system of great interest. Although mature CMOS technology can be used for the fabrication of passive optical functionality, particular photonic functions like efficient light emission still require III-V semiconductors. We present the technology for heterogeneous integration of III-V semiconductor optical components and SOI passive optical components using benzocyclobutene (BCB) die to wafer bonding. InP/InGaAsP photodetectors on SOI waveguide circuits were fabricated. The developed process is compatible with the fabrication of InP/InGaAsP light emitters on SOI.

OCIS codes: (130.0130) Integrated Optics; (220.4610) Optical fabrication

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1. Introduction

Integration of optical functionalities on chip has the same advantages as the ultra large scale integration of electronic functionalities. Besides the economy of scale, the performance and reliability increase. Following the trend of micro-electronics, Silicon is becoming nowadays an important candidate for optical functionalities. Silicon-on-Insulator (SOI) passive optical waveguide circuits can be fabricated using standard CMOS technology [1] and the high index contrast of these waveguides enable compact optical circuits [2]. For particular photonic functions like efficient light emission Silicon has never been a suitable material however. As III-V semiconductors are the workhorse of telecommunication industry there is a need to develop technologies to heterogeneously integrate functions based upon other materials onto Silicon, which may contain electronic circuitry or passive photonic circuitry. This integration process should be done as much as possible using wafer scale technologies.

The integration of different material systems can be done using wafer bonding or epitaxial growth. Due to the difference in lattice constants between III-V semiconductors and Silicon, epitaxial growth results in a large defect density thereby reducing the optical quality of the layers. This can be solved by using an intermediate buffer ceramic layer for GaAs growth on Silicon [3] or by epitaxial lateral overgrowth (ELOG)[4]. Epitaxial growth of Germanium onto Silicon can be used to fabricate efficient photodetectors on Silicon [5], but for light emission one still has to rely on III-V semiconductor materials – although significant effort is put into Silicon light emission [6]. Different wafer bonding technologies exist, where direct molecular bonding using a SiO_2 intermediate layer [7] and bonding using a polymer bonding agent [8] are most common. Because direct molecular bonding requires very high quality flat surfaces, CMP technology has to be used to planarize the waveguide topography. As spin coating a polymer bonding layer onto the waveguide topography can already give sufficient planarization, this process is easier.

The proposed process flow for heterogeneous integration is depicted in Fig. 1. In a first step, unprocessed opto-electronic dies are bonded to the processed SOI waveguide circuitry. The technology used for this bonding step can be both direct molecular bonding or bonding by means of a polymer bonding agent. As the opto-electronic dies are still unprocessed, positioning accuracy is not stringent and a fast pick-and-place machine can be used. After bonding, the III-V semiconductor substrate is removed by mechanical grinding and chemical etching until the epitaxial layer stack is reached. After substrate removal, active opto-electronic components can be fabricated lithographically aligned to the underlying SOI waveguide features.
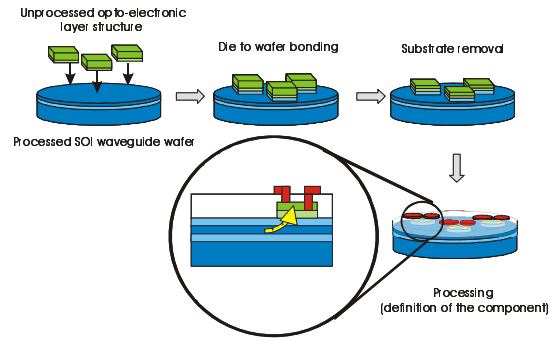
Fig. 1. Proposed process flow for heterogeneous integration of III-V semiconductors and SOI waveguide circuitry

2. Light coupling schemes

As light has to be coupled from the SOI waveguide layer into the III-V opto-electronic component and vice versa efficient coupling schemes need to be designed. Depending on the type of active opto-electronic component a different coupling scheme may be needed. The coupling of light from a membrane photonic crystal laser to an SOI waveguide was already studied in [9]. Light was coupled evanescently from the laser cavity into the SOI waveguide requiring thin bonding layers (~300nm). The coupling of light from a side emitting bonded laser diode into an SOI waveguide was studied in [10], both for the case of thin bonding layers (~300nm) and thick bonding layers (~3μm). In this case adiabatic tapers were used to transform the waveguide modes reducing the influence of bonding layer thickness variation. As bonding yield depends on bonding layer thickness due to the imperfectness of the mated surfaces thick bonding layers are preferred. As the coupling of light from a light emitting device into an SOI waveguide was already studied, we will focus on the coupling of light from an SOI waveguide to an InP/InGaAsP photodetector bonded on top of the waveguide circuit. These photodetectors can be fabricated together with the III-V light sources. To allow thick bonding layers, a grating coupler is used to diffract light from the SOI waveguide into the photodetector. A schematic cross-section is shown in Fig.2. A benzocyclobutene (BCB) polymer bonding layer is assumed.
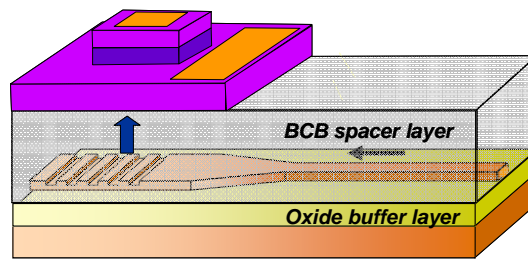

Fig. 2. Coupling scheme for III-V photodetectors bonded to SOI waveguide circuitry

CAMFR [11], a two dimensional fully vectorial simulation tool based on eigenmode expansion, was used to assess the achievable efficiency of the proposed device. TE polarization was assumed. To overcome the polarization sensitivity of the device a polarization diversity scheme can be used [12] which allows to restrict the analysis to transverse electric polarization.

The Silicon waveguide layer is 220nm thick and a second order grating with a grating period of 610nm, a duty cycle of 50% and an etch depth of 50nm is assumed. The device efficiency is assessed by calculating the fraction of the incident power on the grating that is absorbed in the photodetector. A 2μm InGaAs absorbing layer surrounded by n-type and p-

type cladding layers is assumed, being a compromise between device speed and efficiency. Device optimization can be done by optimizing the thickness of the SiO_2 buffer layer and the BCB bonding layer thickness as a cavity is formed caused by the reflection at the BCB/InP interface and the SiO_2/Silicon substrate interface as is shown in Fig. 3. Light is incident from the SOI waveguide on the left side and is diffracted towards the photodetector and the Silicon substrate.

The exact location of the SOI grating inside the cavity determines its directionality (being the fraction of the power coupled upwards) and its coupling strength (determining the length of the grating). Simulation results showing the influence of BCB bonding layer thickness and SiO_2 buffer layer thickness on the fraction of absorbed power for a 50µm long detector are shown in Fig. 4(a). A wavelength of 1.55µm is assumed. Optimal device operation is achieved for a BCB bonding layer thickness of 3µm and a SiO_2 buffer layer of 1.4µm thick. The influence of device length on absorbed power in the photodetector for these optimal parameters is shown in Fig. 4(b).
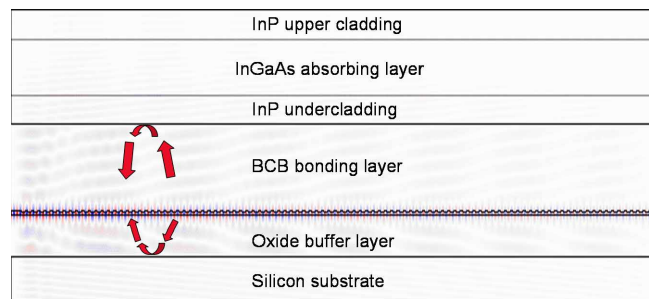

Fig. 3. Simulation of the light diffraction from the SOI waveguide towards the III-V photodetector

The wavelength dependence of the absorbed power fraction for the optimal device parameters depends both on the wavelength dependent properties of the grating coupler used to diffract the light as on the wavelength dependence of the absorption coefficient of the InGaAs absorption layer. The absorbed power fraction, the spurious reflection back into the SOI waveguide and the wavelength dependence of the absorption coefficient are shown in Fig. 5. A strong reflection peak around 1650nm is visible. This is due to the second order Bragg reflection of the grating. Efficient detection up to 1600nm wavelength is achieved.
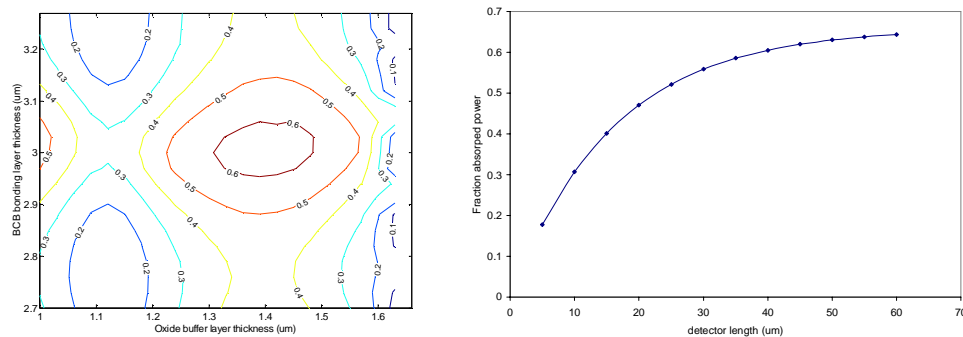

Fig. 4. Influence of BCB bonding layer thickness and SiO_2 buffer layer thickness on detector efficiency (a) and the influence of device length in the optimum parameter case (b)
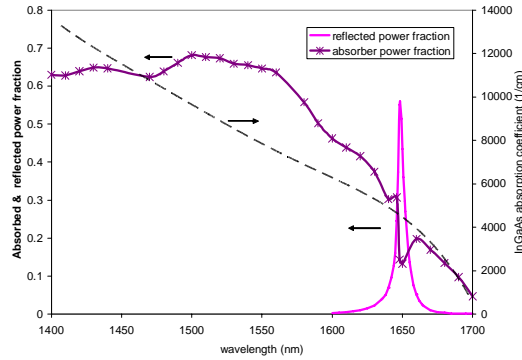
Fig. 5. Wavelength dependence of the absorbed power fraction in the detector and reflected power back into the SOI waveguide. A 50µm long device and optimum SiO_2 buffer layer thickness and BCB bonding layer thickness are assumed. The wavelength dependence of the InGaAs absorption coefficient is also shown.

3. Device fabrication

To validate the integration process, InP/InGaAsP photodetectors were bonded onto functional SOI waveguide components. The SOI substrate consisted of a 220nm Silicon guiding layer and a 1µm thick SiO_2 buffer layer. A 10µm long grating (grating period 610nm, duty cycle 50% and 50nm etch depth) was defined in the Silicon waveguide layer using 248nm deep UV lithography.

An InP/InGaAsP die of $1cm^2$, containing a p-i-n diode layer structure with a 120nm InGaAsP absorbing layer (bandgap wavelength 1.55µm) was bonded to the SOI waveguide structure. A 3µm thick BCB bonding layer was used. After curing the BCB at 250C for 1 hour the InP substrate is removed by a combination of mechanical grinding and chemical etching using $3HCl:1H_2O$ until an InGaAs etch stop layer is reached [13]. The remaining III-V layer stack consists of a 1µm thick n-doped InP undercladding and a 1.8µm p-doped topcladding layer. After substrate removal the detector mesa is etched through the absorbing layer and a AuGeNi n-type contact is deposited. After applying a BCB isolation layer, top windows are opened and a TiAu p-type contact is deposited and annealed. A top view of the fabricated devices before top contact definition is shown in Fig. 6.
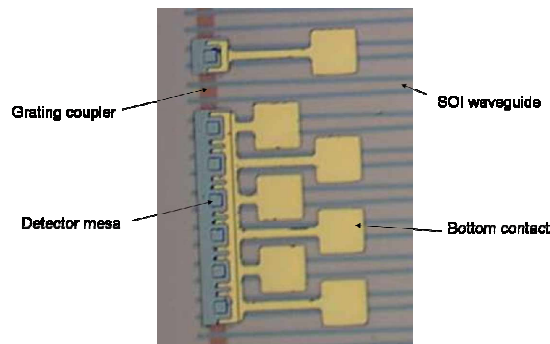

Fig. 6. Top view of the fabricated structure before top contact definition. Grating couplers, detector mesas, SOI waveguides and bottom contacts are visible.

4. Device measurements

10µm x 10µm photodetectors were bonded onto an SOI waveguide grating and light was injected from a single mode optical fiber into the SOI waveguide using the same type of grating coupler. The dark current of the 10µm x 10µm device was 0.3nA at a reverse bias of

1V. The responsivity of the photodetectors was measured to be 0.02A/W at 1550nm referenced to power injected into the SOI waveguide. This low value is due to the non-optimized absorbing layer thickness and device length and is in good agreement with simulation results. Simulation of the absorbed power fraction in the fabricated devices is shown in Fig. 7. Comparison of Fig. 7 and Fig. 4(b) shows that nearly a twenty fold increase in responsivity can be achieved by increasing the absorption layer thickness.

Photodetectors were bonded to wavelength selective filters fabricated in the SOI waveguide layer. The response from the different photodiodes bonded on a 4 racetrack resonator filter acting as a wavelength demultiplexer is shown in Fig. 8(a). The resonance wavelength of the various racetrack resonators was modified by linearly increasing the racetrack bend radius by 15nm. The nominal racetrack bend radius is 4µm. An SEM view of the wavelength demultiplexer filter is shown in Fig. 8(b). By reducing the increase in bend radius, the resonance peaks of the various resonators were made to overlap resulting in a bandpass/bandstop filter. The measured photocurrent from a 6 racetrack resonator device is shown in Fig. 9. 13dB suppression in the stopband is achieved. These results validate the functionality of the SOI waveguide circuits after III-V die bonding.
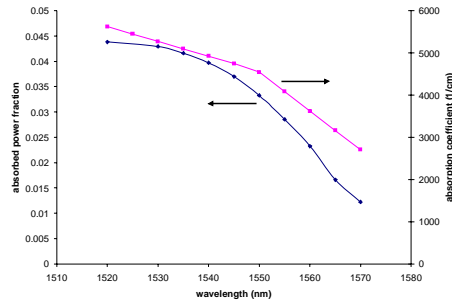

Fig. 7. Simulated absorbed power fraction in the fabricated devices (120nm InGaAsP absorbing layer, 10µm device length, 1µm SiO_2 buried oxide layer thickness and 3µm BCB bonding layer thickness)
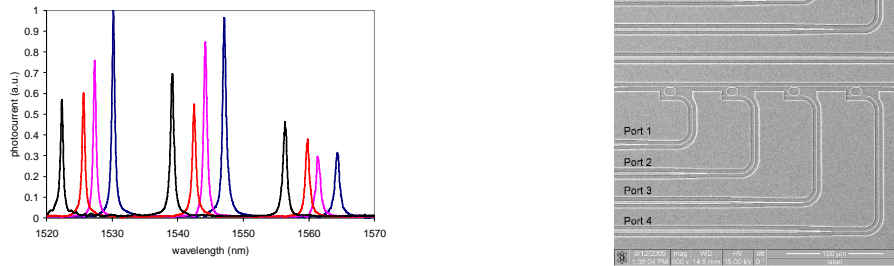

Fig. 8. Response of 4 photodiodes integrated onto a 4 racetrack resonator filter (a) and an SEM view of the fabricated SOI waveguide structure (b)
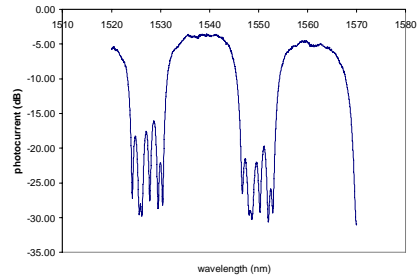
Fig. 9. Measured photocurrent from a 6 resonator device acting as a bandpass/bandstop filter

5. Conclusions

As a demonstration of the integration of optical functionalities on a photonic IC, we fabricated InP/InGaAsP photodetectors on top of SOI waveguide circuits. Compact wavelength selective filter functions with integrated photodetectors were fabricated using standard deep UV lithography and back-end III-V processes. This technology development opens the way to the integration of III-V light sources, modulators, amplifiers and detectors on high density passive Silicon-on-Insulator optical waveguide circuits.

Acknowledgments