A nanophotonic 4x4 wavelength router in Silicon-on-insulator

P. Dumon, W. Bogaerts, D. Van Thourhout, G. Morthier and R. Baets
Department of Information Technology (INTEC), Ghent University-IMEC, Sint-Pietersnieuwstraat 41, 9000, Gent, Belgium
Pieter.Dumon@intec.UGent.be

P. Jaenen, S. Beckx and J. Wouters
Interuniversity MicroElectronics Center (IMEC) vzw, Kapeldreef 75, 3001 Leuven, Belgium

T. Farrell and N. Ryan
Intune Technologies, 9c Beckett Way, Park West, Dublin 12, Ireland

E. Grivas, E. Kyriakis-Bitzaros and G. Halkias
Institute for Microelectronics (IMEL), NCSR 'Demokritos', 15310 Agia Paraskevi, Greece

I. McKenzie
European Space Agency - TEC-MME, ESTEC, Keplerlaan 1, 2201 AZ Noordwijk, The Netherlands

Abstract: We demonstrate a 400x150μm^2 Silicon-on-insulator 4x4 arrayed waveguide grating with 3.5dB insertion loss, fabricated with CMOS technology. The device was pigtailed and used as a wavelength router in a 10 Gb/s reconfigurable optical backplane interconnect.

OCIS codes: (130.1750) Integrated Optics Components (230.3120) Integrated Optics Devices

1. Introduction

Integration of a high functionality in the telecom wavelength range on a die size of a few mm^2 opens up perspectives in a wide range of potential application fields, definitely if it is combined with volume fabrication methods. Here we demonstrate a passive 4x4 wavelength router based on an arrayed waveguide grating (AWG) in high index contrast, submicron Silicon-on-insulator (SOI) 'photonic wire' technology, fabricated using waferscale CMOS based technology. Currently, SOI AWG devices that can act as wavelength routers have been demonstrated [1,2], however still showing considerable insertion losses and/or high crosstalk. In this paper, we show reduced insertion losses by applying a two-step processing technique, allowing for a slightly lower index contrast in the star couplers of the AWG.

The AWG device was pigtailed using vertical fiber coupling and a fiber array connector, and used as the core of a wavelength routed optical backplane interconnect demonstrator in order to get an idea of the performance in an actual potential application case.

2. Silicon-on-insulator AWG

Structures are etched in 200mm SOI wafers with a 220nm thick Si top layer and a 1μm buried oxide, following definition of the patterns in resist using 248nm deep UV lithography [3]. To create high-index contrast waveguides, the Si layer is etched through. These waveguides support a TE mode with propagation losses of about 2.5dB/cm for a 500nm wide wire [3]. Bends used in the AWG have a 3μm radius, with a measured excess loss lower than 0.01dB for a 90° bend. By using a more shallow etch (70nm deep) for the star couplers, a slightly lower index contrast is obtained and insertion losses in the star couplers are strongly reduced.
In order to couple to fiber, grating couplers are used [4]. These couplers convert the mode between a broad access waveguide and the fiber mounted under an angle of 9° from the vertical axis. The gratings are created using the shallow etch process also used for the star couplers. Currently a simple linear taper connnects the access waveguides and the narrow wires. After etching, the die is covered with a 750nm thick top silica layer. This enhances the fiber coupler transmission and serves as a passivating and protective cover. Additionally, fiber coupler transmission is enhanced by applying an index matching material (glue) between fiber and chip. Note that the inputs of the device

must be polarization controlled. A polarization diversity scheme can resolve this [5]. The fiber-to-chip insertion loss with an air gap between the fiber and top silica cladding is about 5dB (>30%) with a 3dB bandwidth of 30nm, estimated from the transmission of the shortest alignment waveguide on the chip.

Figure 1 shows the mask design, with a 300µm x 150µm AWG and 8 access waveguides with grating couplers. In the centre, additional fibre couplers and waveguides are used for alignment.

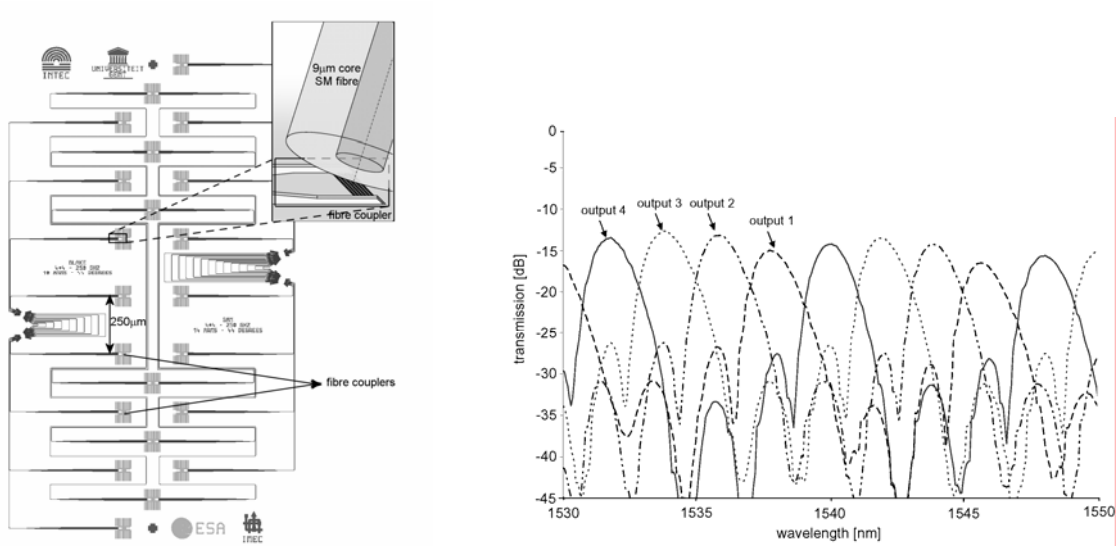

Fig. 1. (Left) Mask layout with AWG and fibre couplers. Spacing between the couplers is 250µm, compatible with a standard array connector. (Right) Fibre to fibre transmission of the pigtailed device, from input 3 to all outputs

3. Characterization and pigtailing

Characterization and final pigtailing of the device is done with a commercially available eight-fibre array connector. This assembly consists of single-mode fibres in Silicon V-grooves with a pyrex top lid. The fibre spacing is a standard 250µm. The facets are polished under an angle of 8° and the connector is mounted under a 9° angle. Because of the resulting 1° tilt between fibre facets and sample, the connector can rest on the sample without damaging the fibre cores (or the AWG, which is much smaller than the connector). The connector is first aligned to the chip visually using on-chip markers and then actively using alignment waveguides connecting fibres two by two. Due to the large alignment tolerances of the fibre couplers [3], this first alignment is very fast. In a next step, the in-plane rotational alignment and a possible tilt between connector and chip in the direction of the array are corrected for. The connector is then moved in-plane to align with the AWG access grating couplers and the connector is moved downwards. In this stadium the device can be characterized.
In order to obtain a packaged device, the connector is attached to the chip using UV-cureable glue, which also serves as an index-matching material. The connector with chip is mounted on an Aluminium plate on top of a Peltier element for temperature control. An Aluminium box serves as a housing for the component and as the thermal ground. The sample hangs in the air, with a highly conductive but still fairly long thermal path (Al+Si) between Peltier element and chip. For the next generation, a more compact packaging approach will be used.

4. Performance of the packaged AWG

The AWG has a channel spacing of 250GHz and a 1THz designed free spectral range (FSR). Figure 1 shows the fibre to fibre transmission spectra from input 3 to all outputs. The actual FSR is slightly larger (1.025THz). Fibre-to-fibre insertion losses are between 12.5 and 17dB depending on the route and wavelength channel. We measured the insertion loss of the actual AWG to be 3.5 dB for the best channel combination. The single fibre coupling loss is therefore about 4.5dB (compared to 5dB before gluing). The sidelobe level is around -12dB to -14dB.

Due to the strong light confinement and high index contrast, wavelength filters in SOI are rather sensitive to temperature. On the other hand, we tuned the AWG for over 1nm with a 10°C temperature change.

5. Crosstalk and bit error rate measurements

The packaged component was tested in a high-speed reconfigurable optical backplane interconnect demonstrator. This interconnect network used passive wavelength routing with tunable lasers and fixed receivers. By choosing the proper wavelength from a routing table, transmitting nodes choose the destination node. The setup consisted of 4 nodes. Two of the nodes where equiped with a tunable laser and an Avanex transponder (modulator+receiver) and connected by two fibres (TX+RX) to the SOI component. The two other nodes had a receiver only. The nodes communicate at a speed of 10Gbps. Each node is equipped with an Altera Stratix-II FPGA, which takes care of the basic system control such as synchronizing the nodes, locking in on the data stream, driving the transponder, selecting the appropriate wavelength of the tunable laser and handling the data streams. A 2^{32}-1 PRBS generator implemented on the FPGA provides the transmitted data, while a bit by bit comparison of received and sent data streams is performed to specify bit error rate by counting the number of errors and the total number of bits received.
The SOI AWG was tested with one node and two nodes (with full transponder) in order to test the behaviour of the network without crosstalk and with single channel crosstalk (only one crosstalk-generating data stream). We monitored the optical power in the links in order to know the actual signal-to-crosstalk ratio incident on the receiver.
The SOI AWG has a 250GHz channel spacing, the widely tuneable lasers have their frequencies on a 50GHz spaced ITU grid. The best wavelengths with respect to the AWG passbands were chosen. The receivers had a specified sensitivity of -22dBm.
The actually measured signal-to-crosstalk ratio in front of the receiver (with a PRBS data stream) varied between 9dB and 26.7dB depending on the combination of inputs and outputs (and wavelengths). From the (CW) transmission spectra we expected a variation between 11.6 and 29.7dB, however for some paths the alignment between laser wavelengths and passbands was suboptimal. With a typical signal-to-crosstalk ratio of 19dB, the power penalty due to (single channel) crosstalk is only a few tenths of a dB for bit error rates of 10^{-9} to 10^{-11}. With a crosstalk level of -10dB, this power penalty rises to about 1 dB.

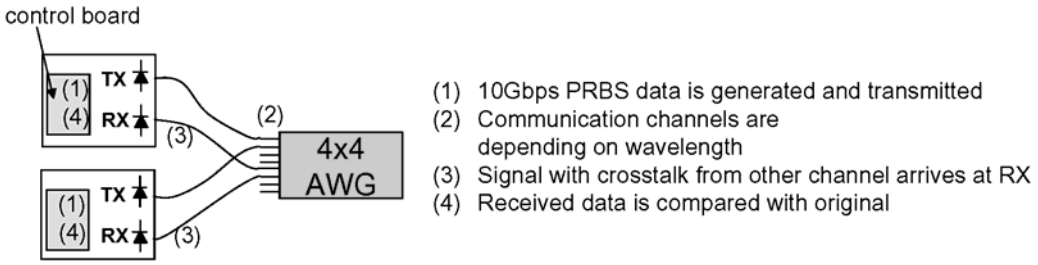

Fig. 2. Schematic of the high-speed wavelength-routed interconnect setup

6. Conclusions

We fabricated a 4x4 arrayed waveguide grating in Silicon-on-insulator photonic wires using CMOS based technology. A two-step processing technique was used in order to lower the device insertion losses, measured to be 3.5dB. The device was pigtailed with an 8-channel fiber array using vertical grating couplers. It was used as a wavelength router in a 10Gb/s reconfigurable optical backplane interconnect and showed single channel crosstalk low enough to give a power penalty of about 1dB for the worst communication path for bit error rates of 10^{-9} to 10^{-11}.

7. References

[1] K. Sasaki, F. Ohno, A. Motegi and T. Baba, "Arrayed waveguide grating of 70x60μm^2 size based on Si photonic wire waveguides", Electronics Letters **41**, 801-802 (2005).
[2] P. Dumon, W. Bogaerts, D. Van Thourhout, D. Taillaert, V. Wiaux, S. Beckx, J. Wouters and R. Baets, "Wavelength-selective components in SOI photonic wires fabricated with deep UV lithography", Group IV photonics 2004, Hong Kong, p. WB5 (2004)
[3] W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. Van Campemhout, P. Bienstman and D. Van Thourhout, "Nanophotonic Waveguides in Silicon-on-Insulator Fabricated with CMOS Technology", J. Lightwave Technology **23**, 401-412 (2005).
[4] D. Taillaert, P. Bienstman and R. Baets, "Compact Efficient Broadband Grating Coupler for Silicon-on-insulator waveguides", Optics Letters, **29**, 2749-2751 (2004).
[5] D. Taillaert, H. Chong, P. Borel, L. Frandsen, R. De La Rue and R. Baets, " A Compact Two-Dimensional Grating Couplers used as a polarization splitter", Photonics Technology Letters, **15**, 1249--1251 (2003).