

# Coupling mechanisms for a heterogeneous silicon nanowire platform

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## Abstract

We discuss different mechanisms for coupling light from nanophotonic silicon waveguides to different types of materials added on top of these waveguides for enhancing the functionality of these waveguides. We consider diffractive coupling, evanescent coupling, adiabatic coupling and coupling to an overlay and illustrate these with recent experimental and modelling results.

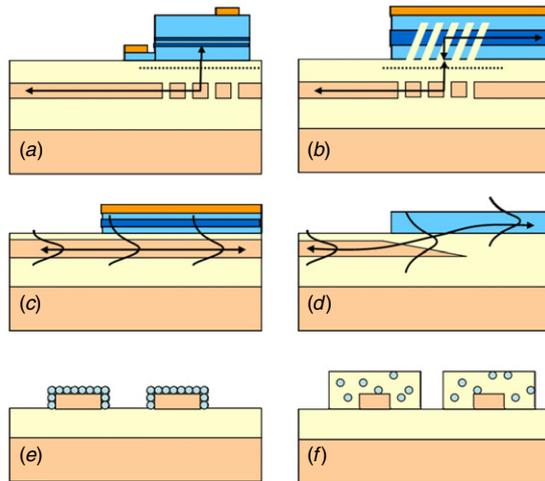
(Some figures in this article are in colour only in the electronic version)

## 1. Introduction

Over recent years, silicon has emerged as a very promising platform for building complex nanophotonic integrated circuits. Monocrystalline silicon has very low intrinsic material losses at telecom wavelengths (1.3  $\mu\text{m}$  and 1.55  $\mu\text{m}$ ) and its high dielectric constant allows for very compact structures such as short bends [1, 2] and high quality optical resonators with record low modal volume [3, 4]. The circuits are typically fabricated on silicon-on-insulator (SOI) substrates with a 200–400 nm thick top silicon layer and a 1–2  $\mu\text{m}$  thick  $\text{SiO}_2$  buried oxide layer. In most cases e-beam lithography is used for the definition of the structures, but the use of DUV-lithography has also been demonstrated [1, 5–7]. The latter is compatible with standard processes used for the fabrication of the most advanced electronic circuits and allows for mass-manufacturing. While silicon is very well suited for the realization of passive devices such as filters and optical multiplexers and also efficient modulation in silicon has been shown [8, 9] often coupling to other materials is necessary. These could be III–V or germanium, e.g. for light generation or detection, metals, e.g. for plasmon sensors, low-index overlays, e.g. for fibre–chip coupling, or metal or semiconductor nanoparticles, e.g. for sensing applications. In each case efficient coupling mechanisms need to be developed, which optimize the interaction of the light with these materials heterogeneously integrated with the silicon nanophotonic circuits. Figure 1 schematically shows different generic

coupling mechanisms that could be employed. In figures 1(a) and (b), the light is coupled vertically out of the plane of the silicon waveguide circuits, e.g. using a diffractive structure. The light can then be coupled to an out-of-plane operating device such as a VCSEL or a detector (figure 1(a)) or to an in-plane operating device such as a DFB laser (figure 1(b)). In the latter case, also a 90° turning mirror is needed in the optoelectronic device mounted on the top. This could be a slanted facet or again a diffractive structure such as the deeply etched slanted grating proposed in [10]. When the light is coupled vertically out of the silicon structures, either a classical solder bump bonding process whereby the distance between the SOI waveguide and the optoelectronic device is at least several micrometers or a wafer-bonding process (see below) can be used. A good modal overlap in the horizontal plane indicated by the dotted line in figures 1(a) and (b) and low back-reflections are essential for the performance of the integrated assembly.

If the active layer can be brought sufficiently close to the silicon layer, through direct deposition techniques or using wafer-bonding techniques, evanescent coupling schemes can also be used as suggested in figure 1(c). Depending on the mismatch between the modes of the uncoupled guides either a large fraction of the power can be coupled upwards as is the case in traditional directional coupler structures or only a small fraction as is often the case in vertically coupled ring resonator structures. Alternatively, an adiabatic taper can be



**Figure 1.** Different coupling scenarios: (a) vertical coupling to out-of-plane component, (b) vertical coupling to in-plane component, (c) evanescent coupling, (d) adiabatic coupling, (e) interaction with material covering waveguide.

used. The taper can either be defined vertically as suggested in figure 1(d) or more often, laterally.

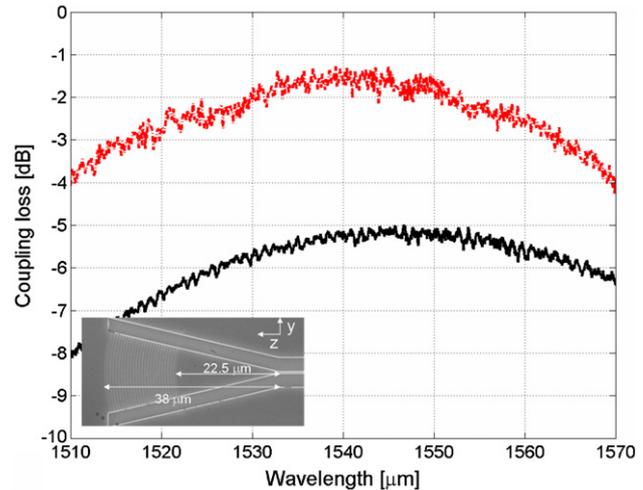
Figures 1(e) and (f), which now show a transversal cross-section of the waveguide, illustrate possible ways for coupling light to e.g. semiconductor nanocrystals or a thin adlayer for sensing applications. In figure 1(e), these form a thin layer on the surface of the waveguide while in figure 1(f) the nanocrystals are dispersed in a low-index overlay layer. The overlay layer in figure 1(f) could also be a liquid-crystal layer or an electro-optic polymer for tuning the waveguide effective index. In both cases, the confinement in the active material can be controlled by the waveguide dimensions and significantly enhanced by adapting the waveguide structure, e.g. through the use of slotted waveguides [11] or photonic crystal waveguides.

Below, we will illustrate the coupling mechanisms—introduced above through a review of recent developments in this domain.

## 2. Vertical coupling

### 2.1. Introduction

As illustrated in figures 1(a) and (b), the ability to efficiently couple light upwards from silicon nanophotonic waveguides through the use of a diffractive structure opens different routes for integrating the latter with optoelectronic devices integrated on the top. In most cases, a small footprint and a large bandwidth are required and therefore a strong grating should be used. In the past, we have demonstrated compact  $12 \times 12 \mu\text{m}^2$  grating couplers by etching 70 nm deep grooves with a period of 630 nm in the silicon layer [12]. The directionality of these gratings, denoting the ratio of the power coupled upwards to the total diffracted power, is 47% at a wavelength of 1550 nm. Due to the mode mismatch with the mode of standard single-mode fibres, the measured (calculated) fibre–chip coupling efficiency was 31% (37%) with a 1 dB bandwidth of 40 nm



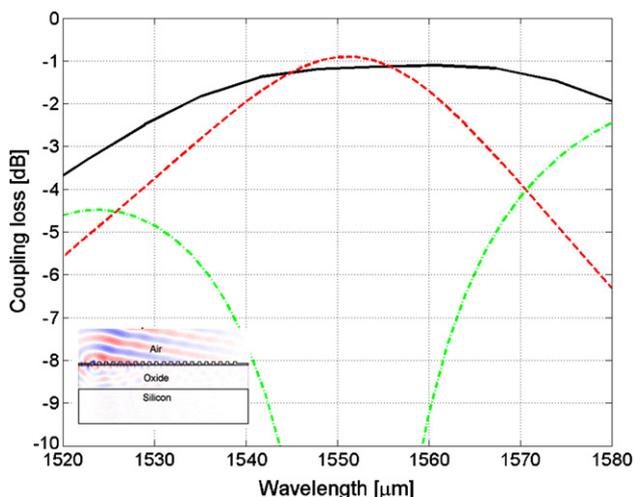
**Figure 2.** Measured fibre–chip coupling loss for standard grating (solid) and improved grating with gold bottom mirror (dashed). Inset: picture of curved grating from [14].

(the solid line in figure 2). An important factor influencing the directionality of these basic gratings is the thickness of the  $\text{SiO}_2$  box layer between the silicon-guiding layer and the silicon substrate. Due to the high index contrast between  $\text{SiO}_2$  and Si, an important fraction of the light coupled downwards will be reflected at the interface between the box layer and the Si-substrate and interferes either constructively or destructively with the light coupled directly upwards. As a result, the directionality for a basic grating coupler as described above may vary from 22% to 64% for a  $\text{SiO}_2$  box layer thickness varying between 900 nm and 1150 nm, respectively. This effect can be further enhanced by introducing a strong mirror below the grating. In [13] we demonstrated that by introducing a metal mirror below the grating the directionality could be increased to 100%, resulting in a measured fibre–chip coupling efficiency of 69% (the dashed line in figure 2). A further enhancement can be attained by curving the grating lines in such a way that the light is focused on the output of the silicon wire waveguide (see the inset of figure 2). Thereby, the length of the taper expanding the lateral size of the mode can be decreased from 100  $\mu\text{m}$  for an optimized parabolic taper in combination with the standard grating to  $<20 \mu\text{m}$  for the focusing grating [14].

Below, we describe recent improvements and alternatives to these previously reported diffractive couplers.

### 2.2. Gratings with improved directionality

As discussed above, introducing a mirror below the diffractive structure can increase the fraction of the power coupled upwards to almost 100%. However, introducing this mirror may complicate the technological process considerably. Therefore, we investigated the influence of the grating parameters and in particular the thickness of the waveguide layer on the directionality of the relevant grating Bloch mode [15]. For an optimized thickness of 370 nm and an etch depth of 220 nm, the directionality is increased to 88%. Next, we



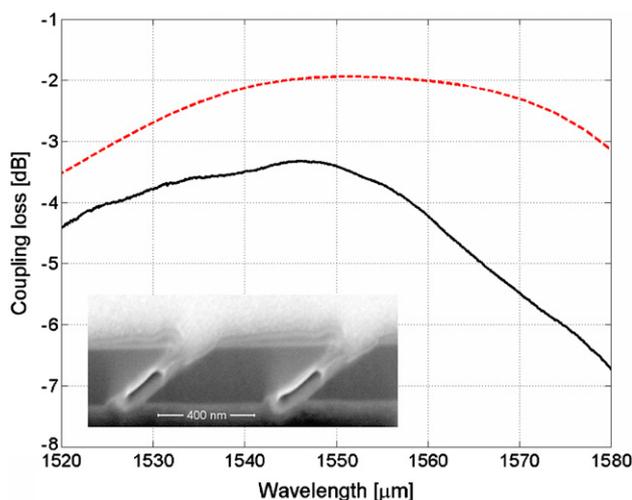
**Figure 3.** Simulated fibre–chip coupling efficiency for gratings with silicon overlay. Full line: optimized structure without slit, out coupling under  $10^\circ$  [15]. Dotted line: with single slit, vertical out coupling efficiency [16]. Dash dotted line: back reflection into waveguide. The inset shows the proposed structure.

calculated the optimized thickness of the waveguide exciting this Bloch mode. It turns out that this thickness is 220 nm, precisely the waveguide thickness we were using before. The resulting structure with a calculated fibre–chip coupling efficiency of 66% is sketched in the inset of figure 3. This structure can be improved further in several ways. The field coupled upwards from the standard diffractive structures is exponentially decaying, while in many cases the ground mode of the device we want to couple with is well approximated by a Gaussian function. Therefore, the coupling efficiency can be increased further by locally adapting the width of the individual grating teeth and slits in such a way that a more Gaussian-like output field is obtained. On the basis of this idea, the parameters of the grating described above were optimized using a genetic algorithm resulting in a 78% coupling efficiency to a standard single-mode fibre (the solid line in figure 3) [15].

In the examples described above, the fibre was always placed at a small angle ( $8\text{--}10^\circ$ ) with respect to the normal on the surface. In that way, a large second-order reflection back into the waveguide is avoided. This is not always required however, and in particular for coupling with certain optoelectronic devices perfectly vertical output coupling would be preferred. Therefore in [16] an additional slit was added to the 220 nm thick silicon waveguide layer. This slit serves as a partially reflecting mirror and cancels the second-order Bragg reflection through destructive interference over a limited wavelength range as can be seen in figure 3 (dash-dotted line). Introducing a second slit slightly increases the bandwidth.

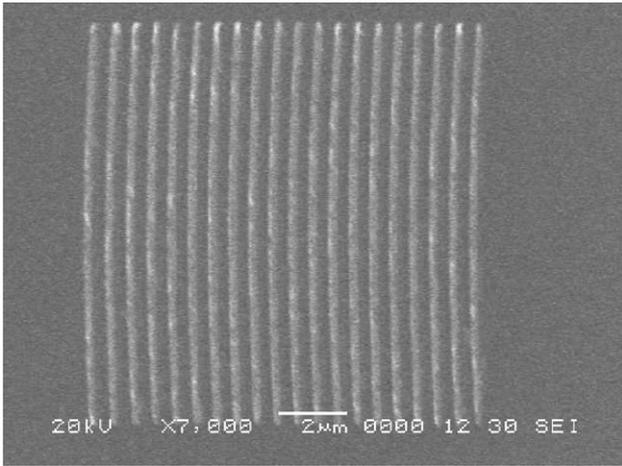
### 2.3. Slanted gratings fabricated using focused ion beam etching

All of the structures described above were defined using optical photolithography. Recently, we demonstrated the



**Figure 4.** Simulated (dashed) and measured (solid) fibre–chip coupling efficiency for slanted SOI-grating etched through FIB. The inset shows cross-section of the slanted grating (from [19]).

use of focused ion beam (FIB) etching for the definition of nanophotonic structures. FIB is a commonly used tool for device analysis and modification in electronics, but has thus far only found limited use in the domain of nanophotonics. Although it allows for the fabrication of complex three-dimensional structures and can be employed for the precise tuning of microcavities [17], the crystal damage induced by the impact of the ion-beam results in prohibitive losses [18]. Even low implantation doses already result in losses of  $0.2\text{--}2\text{ dB } \mu\text{m}^{-1}$ . Therefore, we have developed fabrication strategies to minimize optical losses in FIB-defined structures [18]. In the first step, a 50 nm layer of  $\text{Al}_2\text{O}_3$  is deposited through electron beam evaporation. This layer has negligible influence on the propagation of light in the silicon waveguides below, but it has a very low penetration depth for the incident gallium ions used for etching and hence protects the underlying structures. Next, the desired patterns are written by scanning the ion beam over the surface, in an iodine atmosphere. The latter enhances the silicon etch rate, thereby reducing the required etch doses and consequently the induced damage. Using this process, we demonstrated standard FIB-defined grating couplers with efficiency similar to that of lithographically defined gratings [18]. However, as mentioned above, FIB etching allows for the definition of complex three-dimensional structures. By mounting the sample to be etched at an angle with respect to the ion beam, it is possible to etch a slanted grating. The blazing effect then greatly enhances the directionality of the beam and simulations show such a grating in theory allows for a 60% coupling efficiency to optical fibre [19]. Figure 4 shows a cross-section view of the resulting structure. The slits were etched completely through the silicon layer, at an angle of  $58^\circ$  with the normal to obtain an outcoupling angle of  $10^\circ$ . The etching time for the full grating (15 slits) was 8 min. The measured coupling efficiency was 46%. We believe the discrepancy with simulations can be attributed to remaining damage in the silicon crystal.



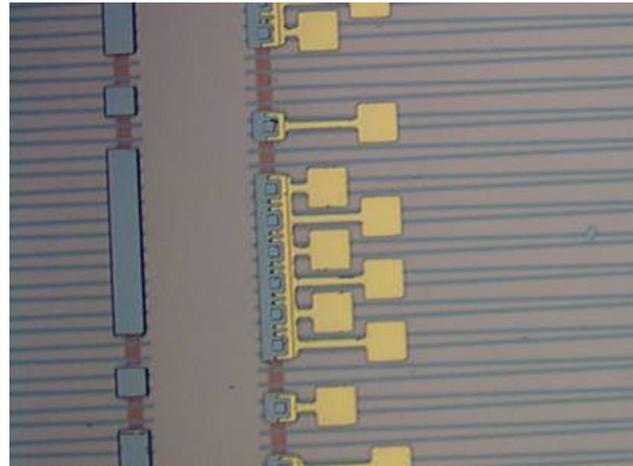
**Figure 5.** Focusing metal grating.

#### 2.4. Metal gratings

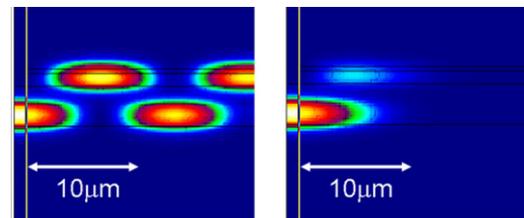
In [20], we demonstrated the use of a gold grating for efficiently coupling light to a silicon waveguide. Despite the high intrinsic losses of metals, the high contrast in dielectric constant with air still allows for very efficient coupling. First experiments showed a 34% coupling efficiency with optical fibre and from simulations we expect a reduction of the coupling loss to less than 2 dB for fully optimized gratings. Further simulations show that CMOS-compatible metals such as Cu and Al could also be used. The performance and coupling angle of the etched gratings are very much dependent on the exact etching depth and therefore require very good process control. To the contrary, the properties of the metal gratings are determined by the thickness of the metal film, which is often better controlled. Furthermore, in some cases even etching of waveguide structures is no longer required. Using a curved grating as shown in figure 5 the light, which is vertically guided in the silicon slab, can be directly focused on the structure under test.

#### 2.5. Integration with PIN detectors

In [21], grating couplers were used to couple light upwards to a PIN detector integrated on top using a heterogeneous integration process based on a combination of bonding and waferscale processing. In the first step, an InP-based die with suitable epitaxial layers is bonded on top of the SOI circuits using a benzo cyclo butene (BCB) adhesive layer. Subsequently, the InP substrate is removed using a combination of mechanical grinding and chemically etching down to an InGaAs etch stop layer, which is then also removed. Next, the mesa structures for the detectors are defined using a standard lithographic process, which ensures accurate alignment with respect to the underlying gratings. Finally, the mesa structures are etched and metal contacts are deposited. Figure 6 shows the fabricated devices right before the deposition of the top contact.



**Figure 6.** InP-InGaAs photodetectors heterogeneously integrated on top of SOI-grating couplers (before top level metallization) [21].

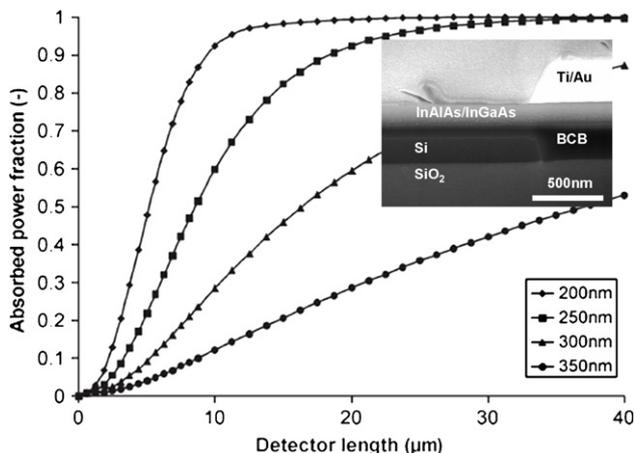


**Figure 7.** Cross-section of an evanescent detector structure.

### 3. Evanescent coupling

#### 3.1. Evanescent MSM-type photodetectors

Evanescent field coupling (figure 1(c)) forms an alternative for coupling light from the silicon nanophotonic waveguides to an absorbing detector layer. Contrary to what is described above, such a scheme requires that the detector layer is in close proximity to the passive waveguide layer. Figure 7(a) shows a cross-section of the simulated field pattern in an optimized detector structure. To obtain a short coupling distance, phase matching between the propagation coefficients of the uncoupled guides is required. In figure 7(a), the imaginary part of the refractive index of the absorbing InGaAs layer is set to zero. It is obvious that almost 100% of the optical power is coupled upwards with a coupling distance below 10  $\mu\text{m}$ . When turning on the absorption (figure 7(b)), all the power is absorbed within 10  $\mu\text{m}$ . Figure 8 shows the required detector length as a function of the bonding layer thickness. It is obvious that the distance between both guides has to be kept as small as possible to obtain structures with a compact footprint. Therefore, we optimized the die-to-wafer bonding process to allow for very thin bonding layers, through optimized cleaning processes and surface activation procedures [22]. The inset of figure 8 shows the cross-section of a completed detector. The detector layer consists of a 145 nm InGaAs detector layer, a 20 nm superlattice layer to decrease carrier trapping, and a 40 nm InAlAs Schottky barrier enhancement layer. The BCB-bonding layer had a thickness of 100 nm. Ti/Au Schottky

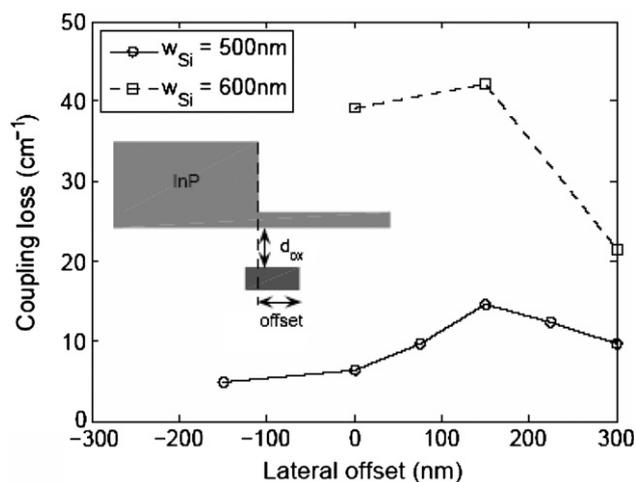


**Figure 8.** Absorption as a function of detector length for different bonding layer thicknesses (from [23, 24]).

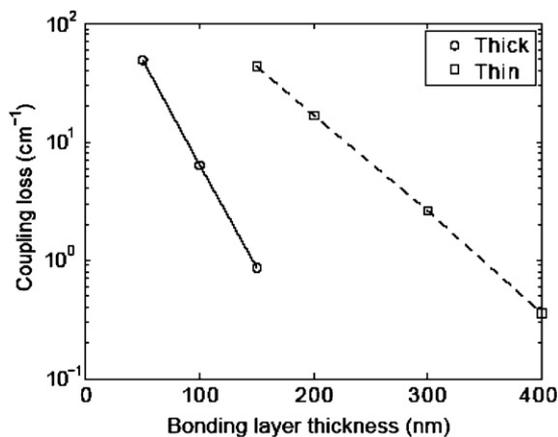
contacts were formed on the top through evaporation. The large dielectric index contrast between metal and air ensures lateral guiding of the light by the contacts in the detector structure. The fabricated detectors showed a responsivity of  $1 \text{ A W}^{-1}$  at  $1550 \text{ nm}$ , without including the fibre–chip coupling efficiency [23].

### 3.2. Coupling to microdisc lasers

In [25], we demonstrated for the first time an electrically injected microdisc laser coupled to a silicon wire waveguide. This device was fabricated using a heterogeneous integration process similar to that described above. Also in this case, the performance of the device is very strongly determined by the strength of the evanescent coupling between the whispering gallery-like laser mode and the underlying silicon wire waveguide. If the coupling is too strong, the cavity losses will be high, resulting in a prohibitively high threshold current. If the coupling is too low, no light will be directed to the silicon wire and the external efficiency will be low. In [26], we calculated the effect of alignment errors and the thickness of the bonding layer on the coupling efficiency using 3D-FDTD simulations. The inset of figure 9 shows a cross-section of the simulated structure, a  $7.5 \mu\text{m}$  diameter InP microdisc above a  $220 \text{ nm}$  high silicon wire waveguide. Figure 9 shows the effect of a lateral misalignment between the silicon wire and the edge of the microdisc. The height of the microdisc was fixed at  $1 \mu\text{m}$  and the bonding layer thickness  $d_{\text{ox}}$  was  $100 \text{ nm}$ . From this picture, it is clear that the highest coupling efficiency is obtained for a slight offset between disc and wire. Also increasing the width  $w_{\text{Si}}$  of the silicon waveguide increases the coupling efficiency considerably. However, it also makes the waveguide multimodal. Figure 10 shows the influence of the bonding layer thickness, for a thick ( $1 \mu\text{m}$  height) and thin ( $500 \text{ nm}$  height) microdisc on the coupling strength. It is obvious that the performance of the laser will be very sensitive to the exact bonding layer thickness (note the logarithmic scale). The thin microdisc structure allows for somewhat more relaxed bonding parameters compared to the thick one, but is more difficult to electrically contact.



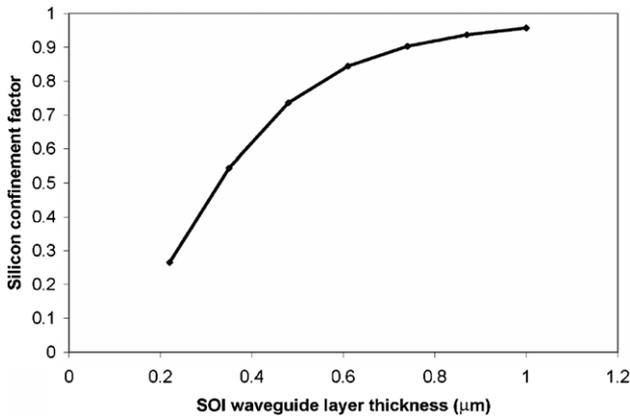
**Figure 9.** Influence of lateral offset on the distributed coupling loss for  $1 \mu\text{m}$  thick microdisc with  $7.5 \mu\text{m}$  diameter. The bonding layer thickness  $d_{\text{ox}}$  was fixed at  $100 \text{ nm}$ . The width of the silicon waveguide  $w_{\text{Si}}$  was varied.



**Figure 10.** Influence of the bonding layer thickness on the distributed coupling loss for thick ( $1 \mu\text{m}$ ) and thin ( $500 \text{ nm}$ ) microdisc. The offset was set to zero.

### 3.3. Evanescently coupled hybrid silicon/III–V laser

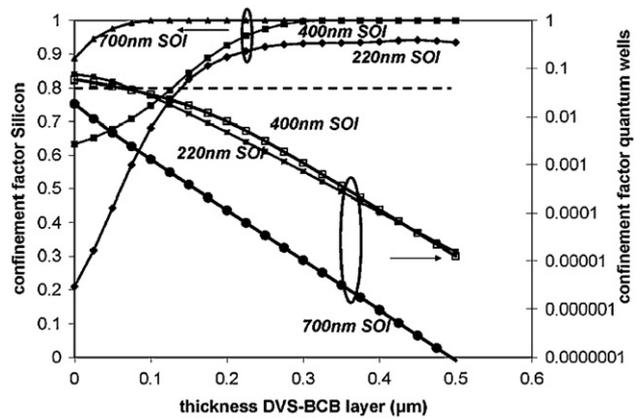
The authors of [27] demonstrated a hybrid silicon laser by directly bonding a III–V epitaxial layer on a silicon waveguide. In such a laser, there is a trade-off between confinement in the silicon layer and confinement in the III–V layer. A high confinement in the silicon layer is desired if one wants to make compact structures and have a good coupling with passive waveguides without III–V overlay. On the other hand, for lowering the threshold current, also sufficiently strong confinement in the III–V gain layer is required. Figure 11 shows the confinement factor of the fundamental mode in the silicon core layer as a function of the height of the silicon waveguide layer. For the  $220 \text{ nm}$  thick SOI waveguide layer, the confinement in the silicon layer is reduced to 26%, implying considerable losses due to the mode mismatch in the transition region between the loaded and unloaded regions. Decreasing the height of the InP layer increases



**Figure 11.** Influence of SOI-waveguide height on the confinement factor in the silicon waveguide.

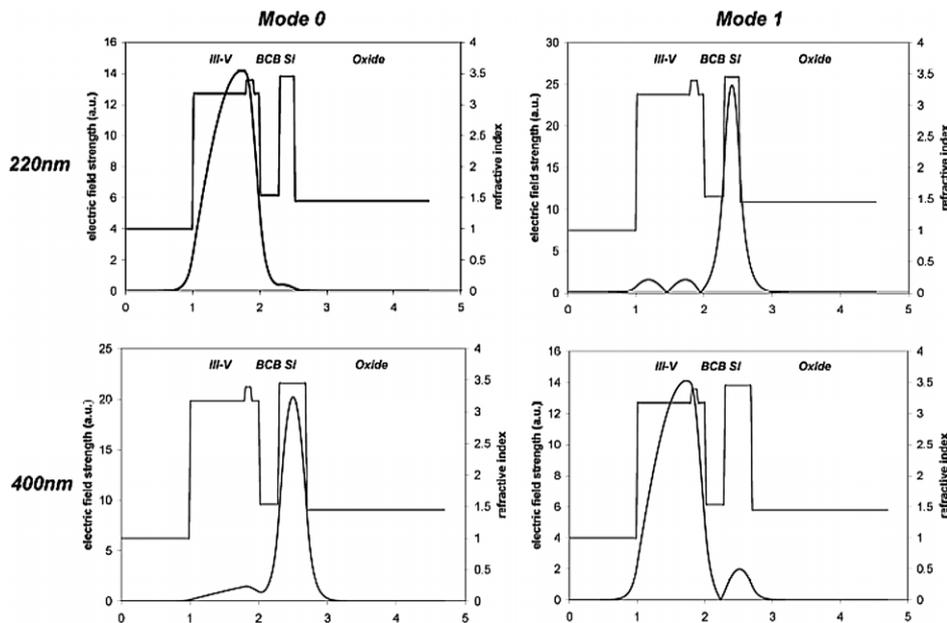
the confinement factor in the silicon layer somewhat—up to 40% for a 200 nm thick III–V layer—but makes the electrical injection difficult. Alternatively, a ridge can be etched in the InP waveguide. For a 200 nm wide ridge the confinement factor increases to 80%. This is also a technological non-trivial solution however.

Thus far, we only discussed the case where no intermediate low-index bonding layer is present between the silicon layer and the III–V layer. The presence of a low-index intermediate layer decouples both waveguides and increasing the thickness of this layer can both decrease or increase the confinement factor of the fundamental waveguide mode in the silicon waveguide, depending on the thickness of the silicon waveguide layer. As an illustration, figure 12 shows these modes for the case of a 220 nm and a 400 nm silicon waveguide

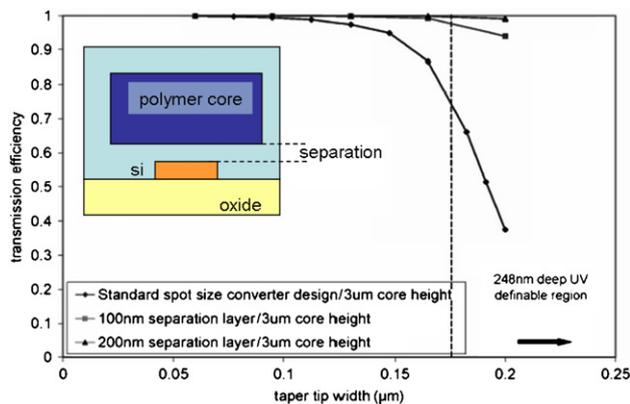


**Figure 13.** Influence of the low index bonding layer thickness on the confinement in the SOI waveguide and in the multiple quantum well region.

layer thickness, respectively. Figure 13 plots the confinement in an active layer consisting of five 10 nm wide quantum wells in the III–V layer and in the SOI core for 220 nm, 400 nm and 700 nm SOI waveguide thickness respectively, for different thicknesses of the low-index bonding layer (for the modes with high silicon waveguide confinement). From this simulation, it is clear that the bonding layer should be reduced to below 150 nm to obtain good confinement in the silicon (>80%) and in the quantum wells (>1%) at the same time. An interesting variation on this structure was proposed in [28], through the introduction of a high contrast distributed Bragg reflector mirror on the top of the active III–V layer, which circumvents this problem and ensures high confinement in both the silicon and the gain layers.



**Figure 12.** Hybrid waveguide modes in the case of a low index BCB bonding layer.



**Figure 14.** Transition loss at the end of the taper as a function of the taper tip width for different thicknesses of separation layers.

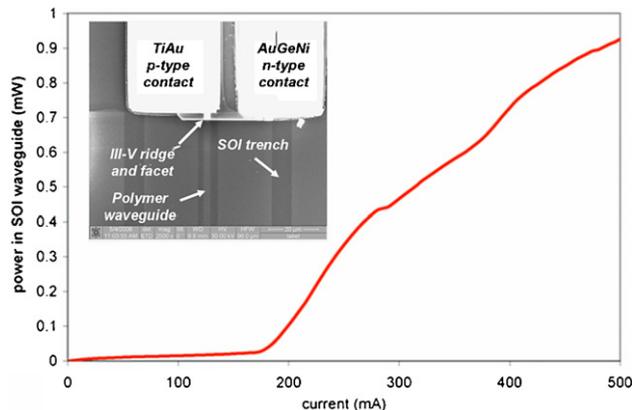
## 4. Adiabatic coupling

### 4.1. Inverted taper with relaxed lithographic requirement

Adiabatic tapers gradually transform a mode profile and if well designed they operate over a broad wavelength range and have low losses. These advantages may be offset by an increased footprint. In [29], a three-dimensional taper is used to increase the mode size of a nanophotonic waveguide. However, such tapers are technologically difficult to realize and are multi-modal at the exit. In addition, when used for fibre–chip coupling, they also feature a large reflection. A more popular approach is the inverted taper in which the waveguide core dimensions are decreased to a point whereby the mode is no longer strongly confined by the nanophotonic wire but pushed upwards to a lower index cladding layer, which is in most cases etched to form a waveguide [2, 30]. Such a taper requires feature sizes of 100 nm or lower, which are difficult to realize using optical lithography. Therefore, we proposed an alternative approach [31]. The narrow taper tips are required because the low-index waveguide and the silicon nanowire are strongly coupled. By introducing a thin spacer layer between both waveguide cores, the modes become partially decoupled and considerably wider taper tips are allowed without introducing additional losses. This is illustrated in figure 14, which shows that by introducing a 200 nm separation layer the minimum taper width can be increased to 200 nm, which is well within the capabilities of 248 nm DUV lithography. In [31], we demonstrated a coupling loss of 1.9 dB between a lensed optical fibre and a silicon waveguide, using a 175  $\mu\text{m}$  long adiabatic taper with a 175 nm wide taper tip.

### 4.2. Adiabatically coupled laser diode on silicon wires

Besides for fibre–chip coupling, the adiabatic taper described above can also be used for coupling to or from a waveguide defined in a III–V layer bonded on the top of the silicon. In [32], we demonstrated for the first time a Fabry–Pérot laser heterogeneously integrated on silicon and coupled to silicon

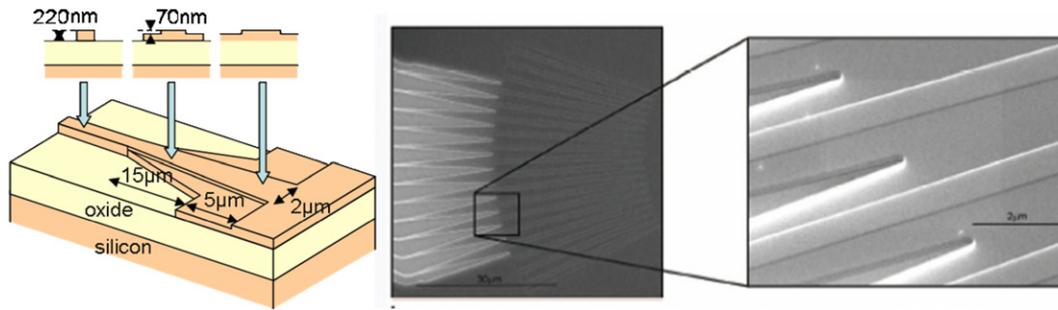


**Figure 15.** Power coupled to SOI waveguide (1% duty cycle, 500  $\mu\text{m}$  length, 2.8  $\mu\text{m}$  width) for heterogeneous laser (from [32]).

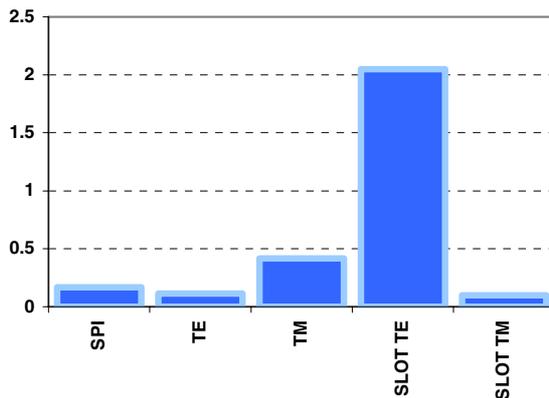
waveguides using the heterogeneous integration approach already described above in section 2.6. Following the die-bonding and substrate removal, islands were defined in the InP-based epitaxial film remaining on the silicon wafer. Subsequently, a polyimide film was spun over the whole surface and etched back on top of the InP islands. Then, in a single self-aligned step, the InP/InGaAsP laser ridges and the polyimide waveguides were lithographically defined and etched using several cycles of  $\text{CH}_4/\text{H}_2$  and  $\text{O}_2$  RIE respectively. The BCB bonding layer has a slightly lower index compared to the polyimide film and served as the intermediate layer described above. The inset of figure 15 shows a top SEM view of the completed laser, which, for a length of 500  $\mu\text{m}$ , had a threshold current density 10.4  $\text{kA cm}^{-2}$  under pulsed operation. At 200 mA, over 1 mW of power was coupled to the silicon nanowire waveguides. To decrease the thermal resistance, we added a heat sink structure to the device [33]. A similar but shorter structure was also tested as a detector. For a 2 V reverse bias voltage, a responsivity of 0.23  $\text{A W}^{-1}$  (not including fibre–chip coupling efficiency) was measured in a 50  $\mu\text{m}$  long structure.

### 4.3. Adiabatic transition between shallow and deep etch SOI nanowire waveguide

For compact bends and photonic crystal structures, one typically etches completely through the silicon layer. However, in some cases it may be advantageous to use shallowly etched waveguides. This is, for example, the case at the entrance of the star couplers used in arrayed waveguide grating demultiplexers (AWG), to avoid excess coupling losses, or if long low loss single mode waveguides are required. The transition between both waveguide types can be realized through an adiabatic taper as schematically shown in figure 16(a). Such a taper is very tolerant to misalignment errors between the two mask levels required for realizing this structure. Use of these tapers at the entrance of an AWG-star coupler (figures 16(b), (c)) lowers its insertion loss from 8 dB to less than 2.5 dB [1].



**Figure 16.** Adiabatic transition between the fully etched rib waveguide and the shallowly etched waveguide at the entrance of an AWG (from [34]).



**Figure 17.** Comparison of different waveguide geometries for sensing applications.  $\partial n_{\text{eff}}/\partial d_{\text{thickness}}$  ( $1/\mu\text{m}$ ) for surface plasmon modes (SPI), single modes SOI waveguides (TE and TM) and slotted single mode SOI waveguide (SLOT TE and SLOT TM).

## 5. Coupling to overlay

### 5.1. Adlayer sensitivity for different waveguide configurations

The silicon nanowire waveguides described above allow confining the propagating mode to a very small cross-section. In a simple stripe waveguide, the mode can be confined to an area of the order of a square wavelength. In a plasmonic structure, the field can be confined further to sub-wavelength dimensions. The same holds for slotted real-index waveguides where the low-index slot can have a very high confinement factor.

The strong confinement is not only important for passive functions such as bends, but also to optimize the efficiency or sensitivity of certain functions. In the case of active functions—functions whereby the mode propagation is influenced somehow by something over time—it can be of key importance that the active part of the structure is as small as possible. This allows active devices to be made power efficient and/or fast and it allows sensors—that sense the presence of an adlayer—to be sensitive.

As an illustration the potential of various high index contrast SOI waveguide structures for sensing applications is shown. In figure 17, we have plotted the change in effective index of the guided modes as a function of the thickness

of a thin adsorbed layer with refractive index ( $n = 1.45$ ) at the waveguide surface ( $\partial n_{\text{eff}}/\partial t_{\text{adlayer}}$  ( $1/\mu\text{m}$ )). By using different transduction principles (interference, resonance, mode coupling) the effective index of the guided modes can be read out as a power difference, thus enabling the sensing action. Comparison among three different waveguide geometries, the surface plasmon interferometer geometry on SOI [8] with an adsorbed layer on top, a single mode SOI waveguide (220 nm thick, 450 nm broad) with an adsorbed layer on top and a slotted waveguide (same single-mode waveguide but with a slot of 50 nm and the adsorbed layer on the slot walls) shows the enormous potential of the TE mode of slotted waveguides for sensing applications.

## 6. Conclusion

In this paper, we reviewed basic mechanisms for coupling light from silicon nanophotonic waveguides to different types of structures, which are added to improve the functionality of the basic waveguides. Methods based on diffractive structures, evanescent and adiabatic coupling and overlay layers were discussed. The method chosen for a given application will depend on the required coupling efficiency, the desired bandwidth, the available footprint and technological considerations.

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