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Strategies to increase the modal gain in heterogeneously integrated III–V amplifiers on silicon-on-insulator

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Abstract A novel waveguide shape is proposed to take advantage of the high index contrast in adhesively bonded III–V on silicon-on-insulator (SOI) waveguides for application in on-chip semiconductor optical amplifiers. By decreasing the effective index of the top contact layer, the confinement in the active region can be increased by 70 %, boosting the achievable modal gain and reducing the required device length to achieve a certain gain. This technique could reduce the footprint of amplifiers, lasers and other active devices integrated on the SOI platform.

Keywords Silicon photonics · Heterogeneous integration · Optical amplifier · Simulation

1 Introduction

Silicon-on-insulator (SOI) is an excellent platform to realize passive optical functions. Most applications however also require active components such as amplifiers, lasers and detectors. Due to silicon's indirect band gap, the realization of active components on SOI remains a challenge. One approach to circumvent this problem is the heterogeneous integration of an active III–V stack on the SOI waveguide circuit. This can be done by either direct (Augendre et al. 2010) or adhesive DVS-BCB die-to-wafer bonding (Roelkens et al. 2006). Using these techniques, several lasers and detectors have already been demonstrated (Roelkens et al. 2010; Jain et al. 2011). In these devices, one typically uses a III–V stack with a thick top p-InP cladding layer to avoid excessive absorption losses in the top contact layers. To optimize the confinement of the light in the active region for a fixed amount of quantum wells (QWs), extra optical confinement layers (OCLs) of a high index material are added around the active region. Although this leads to working devices, applications such as a low-threshold laser and amplifier would benefit from a higher confinement in the active region. This can be achieved by leveraging the high index contrast between the bonded III–V layers and the surrounding

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air and DVS-BCB/SiO_2 cladding. In this paper, we propose to etch narrow trenches in the top p-InP contact layer, to reduce its effective index. This pushes the mode down into the active region and away from the lossy contact layers. In the following, we will investigate the electrical, thermal and optical properties of such a waveguide structure by comparing it to a reference structure using the commercially available ATLAS (TM) package from SILVACO (R) International (Silvaco 2011b). For this purpose we will design and optimize a low power consumption amplifier at 1.55 μm using both waveguide structures, which can then be implemented in a resonant cavity to create a low threshold laser. For the sake of simplicity a single QW is used as an active region, however this analysis can readily be expanded to multiple QW active regions.

2 Optical design

2.1 Classical waveguide structure

The classical approach (Roelkens et al. 2011) to create a bonded amplifier is shown in Fig. 1a. It is a rib waveguide, which is etched through the active layers to expose the n-InP layer. The n-type contact can then be made on the sides, while the p-type contact is on top of the thicker center part of the waveguide. To avoid excessive losses of the mode due to the top contact layers, the active layers are surrounded by a high index OCL and the top p-InP layer is chosen thick enough. Furthermore, the active region is placed as close as possible to the interface with the DVS-BCB layer, to maximize the interaction with possible silicon structures below the III–V waveguide. This simplifies the coupling of the fundamental TE-mode to an underlying silicon waveguide (Ben Bakir et al. 2011) and in case of a laser allows for an adequate interaction with a distributed bragg reflector fabricated in the silicon waveguide layer (Roelkens et al. 2011). To find the optimal waveguide shape with a single QW, the structure is simulated and optimized to achieve a maximal net gain by varying the OCL and top p-InP contact layer thicknesses. All other structural parameters are fixed and are shown in Fig. 1a and the details on the material stack are given in Fig. 2a. The QW gain was assumed to be 1,000/cm and the associated loss due to free carrier absorption (FCA) in the OCLs was set at 12/cm. In Fig. 1b the profile of the fundamental TE-mode at 1.55 μm is shown for the optimal structure. Most of the light is confined by the OCL layers. However, there is still a significant mode tail extending towards the top contacting layers, which is the reason why the top p-InP layer needs to be at least 1.6 μm thick to avoid excessive losses. In this waveguide structure a confinement of 1.8 % is achieved in the 8 nm thick QW.

2.2 Gallery waveguide structure

The proposed gallery waveguide structure is shown in Fig. 3a. The waveguide has a similar structure as the classical design. The difference is that narrow trenches of less than 350 nm are etched in the top contacting layers, which are afterwards planarized by spin-coating DVS-BCB, a low-index polymer ($n(1.55\,\mu\text{m}) = 1.54$), and etching it back to the p-type contact layer. Because the trench dimensions are smaller than the wavelength, the top cladding behaves as a uniform material with effective index of 2.54. Therefore, a substantially higher index contrast is achieved between the surrounding cladding and the waveguide core. Furthermore, the planarized surface allows the use of a single metal stripe to create the top p-type contact, which can be easily connected to a bigger pad on the side for wire bonding. The gallery waveguide structure was optimized in the same way as the classical

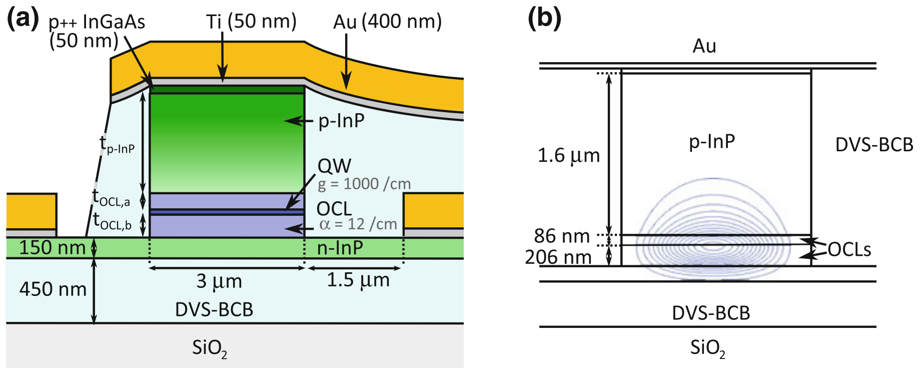

Fig. 1 **a** Waveguide structure in the classical design. **b** Corresponding mode-profile for the waveguide structure with the optimized parameters displayed in the figure. As can be seen, the mode-tail is still extending in the top p-InP contact layer, leading to a thickness of 1.6 µm to avoid excessive metalization losses

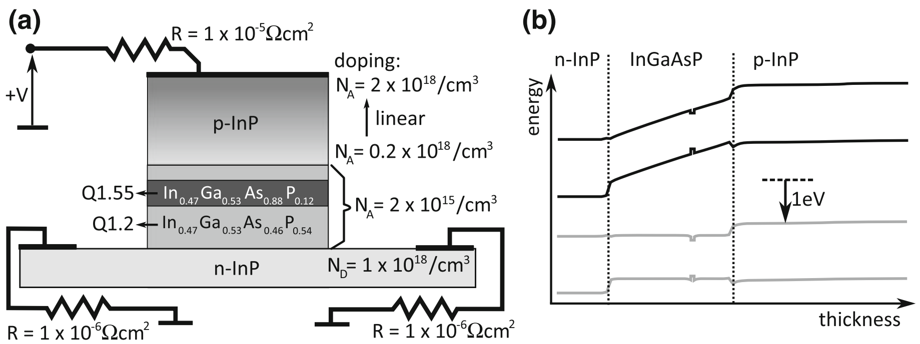

Fig. 2 **a** Material stack and doping profile used in the simulation. **b** Band diagram without applied bias (*black*) and band diagram with a bias of 1 V (*grey*)

design. The top trenches were set to a width of 350 nm, which is a feature size which is still easily achievable using e-beam lithography or deep UV lithography tools. In Fig. 3b the profile of the fundamental TE-mode at 1.55 µm for the optimal waveguide structure is shown. The high index contrast clearly keeps the mode well confined in the active region, leading to a confinement factor of 3.1 % in the QW, which is an increase of 70 % with respect to the classical laser cross section. Furthermore, the mode doesn't extend very far into the top cladding layers, allowing a reduction of the top cladding thickness to 700 nm.

3 Simulation description

The performance of both waveguide structures as an on-chip amplifier is simulated in ATLAS (TM), a commercial package capable of a full thermal, electrical and optical simulation of semiconductor devices. This package uses analytical models for each physical effect, which can be activated separately and for which the details can be found in the manual (Silvaco 2011a). In the simulation, first the band diagram of the device structure is calculated and is displayed in Fig. 2b. After this, an electrical bias is ramped and the effects on the carrier injection, thermal behaviour and optical properties are simulated.

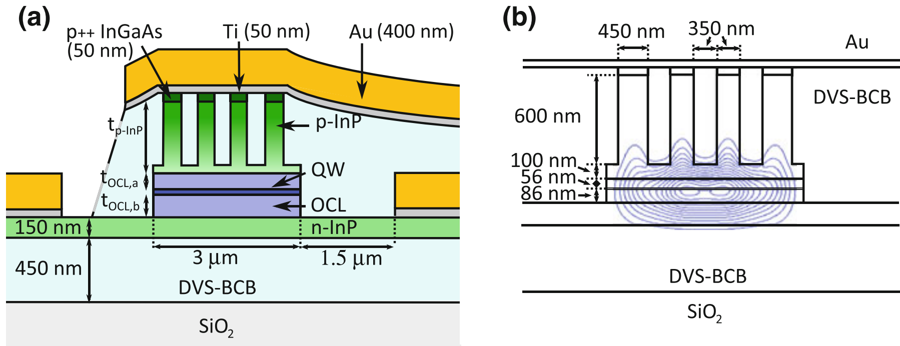

Fig. 3 **a** Waveguide structure in the gallery design. **b** Corresponding mode-profile for the optimized structure. Due to the narrow trenches in the top p-InP layer, the top cladding acts as if it were a low-index material

To realistically assess the performance of the waveguide structures, the following effects are taken into account. Electrically, Shockley-Read-Hall (SRH) recombination, surface recombination, auger recombination and radiative recombination terms are considered. To model carrier mobility saturation effects, the carrier mobility was modeled to depend on the local electric field. Fermi-Dirac statistics are everywhere used. The p-type and n-type semiconductor-metal interfaces are modeled as Ohmic contacts with a resistivity of 10^{-5} and 10^{-6} Ωcm^2 respectively. Optically, losses due to material absorption, sidewall scattering and FCA are taken into account. The sidewall scattering loss was estimated using the volume current method, which models the sidewall roughness as an equivalent current distribution (Ciminelli et al. 2009a). The fields generated by this current distribution can then be used to calculate the scattering loss. In this calculation an approximation is made to allow an analytical treatment of the problem: the medium surrounding the current distribution is considered homogeneous, which allows the use of the magnetic vector potential to derive an analytical expression for the scattering loss (Ciminelli et al. 2009b). Although the scattering estimation is not exact, the results obtained for the TE-mode in a 500 nm × 200 nm and a 300 nm × 300 nm high index contrast silicon wire match with an error margin of respectively only 4 % (Lee et al. 2000) and 20 % (Yamada et al. 2006) with the experimentally measured loss. In the simulation an rms sidewall roughness of 10 nm and rms surface roughness of 3 nm with correlation length of 50 nm was assumed, both prudent estimations for InP waveguides etched by inductively coupled plasma etching (Bae et al. 2003; Lee et al. 2006). Both spontaneous emission and stimulated emission are considered, where the gain is calculated using the QW model developed by Yan et al. (1990). Note that this calculated gain is everywhere the small signal gain for which no saturation effects have occurred. This optical calculation is performed for a broad wavelength range, but in the following only the achieved peak gain will be considered. The device temperature is calculated using a simple model in which the thermal conductivities of all materials are constant. Both joule heating and heating due to recombination of carriers are considered. For both waveguide designs it is assumed that the back of the SOI sample has a constant temperature of 20 °C and that furthermore the bonded III–V waveguides use the top contacting layer as a thermal shunt to avoid excessive heating because of the low thermal conductivity of the DVS-BCB bonding layer, as was proposed by Stankovic et al. (2008). In Fig. 4 the device layout for thermal simulation is shown. The resulting temperature is fed back to all electrical and optical models which are temperature dependent. This simulation is performed for a device of 200 μm long, using both the optimized classical and gallery waveguide structures.

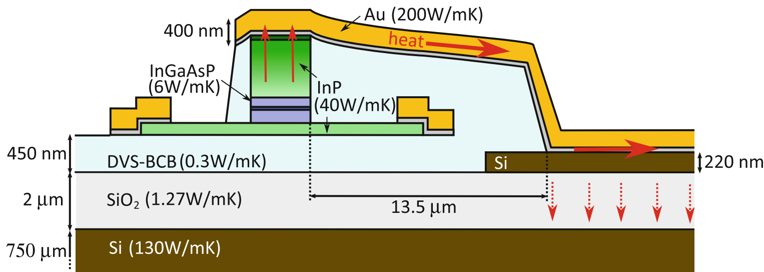

Fig. 4 Thermal design of the simulated amplifier

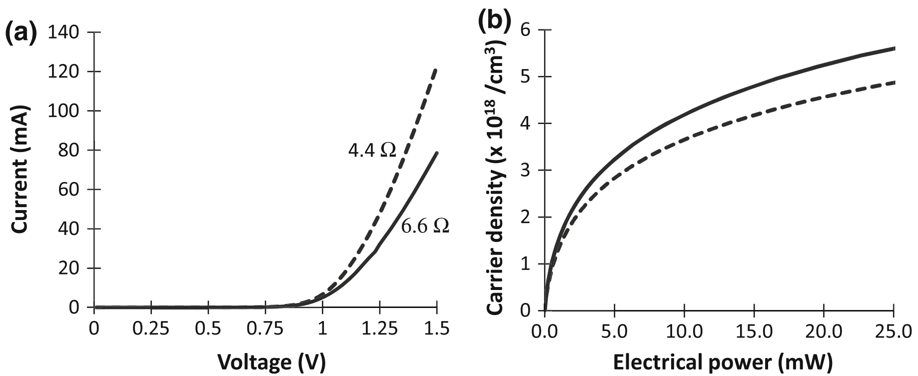

Fig. 5 **a** I(V) curve for the classical (*dashed line*) and gallery (*solid line*) design. The gallery has a higher series resistance, because of the reduced top contact area. **b** Achieved carrier concentration in the QWs as a function of electrical power for the classical (*dashed line*) and gallery (*solid line*) design

4 Results

4.1 Electrical performance

In Fig. 5a the current is plotted as a function of applied voltage. It seems that the gallery design has a differential resistance of 6.6 Ω for a 200 μm long device, 50 % higher than in the case of a classical structure. This increase is caused by the decreased top contacting surface in the gallery design. However, because the top p-InP layer is thinner, the increase is limited. In Fig. 5b the achieved carrier density in the QW is shown as a function of applied electrical power. Although the gallery structure has a higher series resistance, a higher carrier density is achieved in the QW than in the classical design. This is due to an increased carrier lifetime in the gallery structure, which is related to a lower surface recombination. The reason for this is that the InGaAsP OCL layers, which have a higher surface recombination rate (1×10^5 cm/s) than InP (8×10^3 cm/s), are thinner in the gallery structure.

4.2 Optical performance

To assess the optical performance of the device, the net small signal peak gain as a function of the carrier density is plotted in Fig. 6a. The net gain in the gallery design has more than doubled compared to the classical design. This improvement can be attributed to the higher optical confinement in the QWs, combined with a small reduction in FCA. Note that the

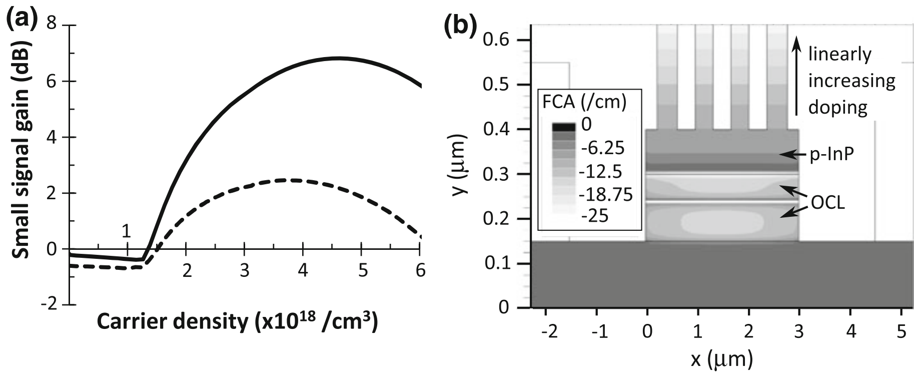

Fig. 6 **a** Achieved small signal net gain as a function of the carrier concentration in the QW for the classical (*dashed line*) and gallery (*solid line*) design. The improved design of the gallery waveguide structure leads to a net gain that is nearly two times higher than in the classical structure. **b** FCA in the gallery waveguide structure for an applied voltage of 1 V

apparent threshold in the curve is related to the fact that when the device has not reached transparency yet, the peak gain corresponds to the loss for light with a photon energy below the QW band gap. In Fig. 6b the FCA profile in the gallery waveguide is shown. From this it can be seen that the main contributions to the FCA are due to the high concentration of holes in the top p-InP layer and in the OCL layers. In the gallery waveguide, the mode tail is not extending as far in the top p-InP layer as in the classical waveguide. This leads to a lower FCA contribution from this layer, as the confinement in this p-InP layer in gallery structure is only 26 %, compared to 40 % in the classical structure. Furthermore, the confinement in the OCL layers is the same in both classical and gallery waveguide, leading to a net improvement in the FCA.

For higher carrier densities, the gain is saturating. This is because the number of free states in the QW is decreasing. This leads to a higher carrier density in the OCL layers, which in turn increases the FCA and through non-radiative recombination leads to a high heat dissipation. This results in an increased device temperature, leading to both a lower QW gain due to a smoothing of the Fermi-Dirac carrier distribution and an increase in the efficiency of non-radiative recombination processes. Eventually the increased losses and degraded QW gain lead to a decline in the gain curve.

A drawback of the gallery design is the higher scattering loss: when considering only the scattering due to the sidewalls a 32-fold increase of the loss is observed, from a simulated 0.19 to 6 dB/cm. Additionally, the vicinity of the bottom of the etched trenches to the optical mode adds an excess loss of 1.3 dB/cm, leading to a total scattering loss of 7.3 dB/cm. However, compared to the gain improvement, this has only minimal impact on the device performance.

5 Conclusion

In this paper, we have proposed a novel waveguide structure for application in the heterogeneously integrated III–V on SOI waveguide platform. Simulation shows that by etching trenches in the top contacting layer, the confinement in the active region can be increased by 70 % and the losses due to metalization and p-type doping can be reduced, leading to a

net gain improvement of more than a factor of 2. Furthermore, this technique reduces the total III–V layer thickness, which improves the manufacturability of the laser structure and its integration in a CMOS process flow. In future work, the proposed design will be used to create low-threshold lasers, using an e-beam lithography step to define the top trenches.

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