Ge-on-Si and Ge-on-SOI thermo-optic phase shifters for the mid-infrared

Aditya Malik,[1,2,*] **Sarvagya Dwivedi,**[1,2] **Liesbet Van Landschoot,**[1,2] **Muhammad Muneeb,**[1,2,3] **Yosuke Shimura,**[4,5] **Guy Lepage,**[4] **Joris Van Campenhout,**[4] **Wendy Vanherle,**[4] **Tinneke Van Opstal,**[4] **Roger Loo,**[4] **and Gunther Roelkens**[1,2,3]

[1] *Photonics Research Group, Ghent University-imec, Sint-Pietersnieuwstraat 41, 9000 Ghent, Belgium*
[2] *Center for Nano- and Biophotonics, Ghent University, Belgium*
[3] *COBRA Research Institute, Eindhoven University of Technology, P.O. Box 513, Eindhoven 5600 MB,The Netherlands*
[4] *imec, Kapeldreef 75, 3001 Leuven, Belgium*
[5] *Instituut voor Kern- en Stralingsfysica, KU Leuven, 3001 Leuven, Belgium*

[*] *aditya.malik@intec.ugent.be*

Abstract: Germanium-on-silicon thermo-optic phase shifters are demonstrated in the 5 μm wavelength range. Basic phase shifters require 700 mW of power for a 2π phase shift. The required power is brought down to 80 mW by complete undercut using focused ion beam. Finally an efficient thermo-optic phase shifter is demonstrated on the germanium on SOI platform. A tuning power (for a 2π phase shift) of 105 mW is achieved for a Ge-on-SOI structure which is lowered to 16 mW for a free standing phase shifter.

OCIS codes: (250.5300) Photonic integrated circuits; (160.6840) Thermo-optical materials; (250.7360) Waveguide modulators.

References and links

1. G. Roelkens, U. Dave, A. Gassenq, N. Hattasan, C. Hu, B. Kuyken, F. Leo, A. Malik, M. Muneeb, E. Ryckeboer, S. Uvin, Z. Hens, R. Baets, Y. Shimura, F. Gencarelli, B. Vincent, R. Loo, J.Van Campenhout, L. Cerutti, Jean-Baptiste Rodriguez, E. Tournie, X. Chen, M. Nedeljkovic, G. Mashanovich, L. Shen, N. Healy, A. C. Peacock, X. Liu, R. Osgood, and W. Green, “Silicon-based heterogeneous photonic integrated circuits for the mid-infrared,” Opt. Mater. Express **3**(9), 1523–1536 (2013).
2. G. Roelkens, U. Dave, A. Gassenq, N. Hattasan, C. Hu, B. Kuyken, F. Leo, A. Malik, M. Muneeb, E. Ryckeboer, D. Sanchez, S. Uvin, R. Wang, Z. Hens, R. Baets, Y. Shimura, F. Gencarelli, B. Vincent, R. Loo, J.Van Campenhout, L. Cerutti, Jean-Baptiste Rodriguez, E. Tournie, X. Chen, M. Nedeljkovic, G. Mashanovich, L. Shen, N. Healy, A. C. Peacock, X. Liu, R. Osgood, and W. Green, “Silicon-based photonic integration beyond the telecommunication wavelength range,” IEEE J. Sel. Top. Quantum Electronics **20**(4), 394–404 (2014).
3. H. Lin, L. Li, Y. Zou, S. Danto, J. D. Musgraves, K. Richardson, S. Kozacik, M. Murakowski, D. Prather, P. T. Lin, V. Singh, A. Agarwal, L. C. Kimerling, and J. Hu, “Demonstration of high-Q mid-infrared chalcogenide glass-on-silicon resonators,” Opt. Lett. **38**(9), 1470–1472 (2013).
4. Z. Cheng, X. Chen, C. Y. Wong, K. Xu, and, H. K. Tsang, “Mid-infrared suspended membrane waveguide and ring resonator on silicon-on-insulator,” IEEE Photon. J. **4**(5), 1510–1519 (2012).
5. Y. Chen, H. Lin, J. Hu, and M. Li, “Heterogeneously integrated silicon photonics for the mid-infrared and spectroscopic sensing,” ACS Nano **8**(7), 6955–6961 (2014).
6. A. Malik, M. Muneeb, Y. Shimura, J. Van Campenhout, R. Loo, and G. Roelkens, “Germanium-on-silicon mid-infrared waveguides and mach-zehnder interferometers,” in *Proc. of IEEE Photonics Conference 2013* (IEEE 2013) pp. 104–105.

#222405 - $15.00 USD Received 3 Sep 2014; revised 30 Oct 2014; accepted 31 Oct 2014; published 7 Nov 2014

7. A. Malik, M.Muneeb, S. Pathak, Y. Shimura, J. Van Campenhout, R. Loo, and G. Roelkens, “Germanium-on-silicon mid-infrared arrayed waveguide grating multiplexers,” IEEE Photon. Technol. Lett. **25** (18), 1805-1808 (2013).
8. A. Malik, M. Muneeb, Y. Shimura, J. Van Campenhout, R. Loo, and G. Roelkens, “Germanium-on-silicon planar concave grating wavelength (de)multiplexers in the mid-infrared,” Appl. Phys. Lett. **103**, 161119 (2013).
9. A. Masood, M. Pantouvaki, D. Goossens, G. Lepage, P. Verheyen, J. Van Campenhout, P. Absil, D. Van Thourhout, and W. Bogaerts, “Fabrication and characterization of CMOS-compatible integrated tungsten heaters for thermo-optic tuning in silicon photonics devices,” Opt. Mater. Express **4** (7), 1383–1388 (2014).
10. M. Nedeljkovic, S. Stankovic, C. J. Mitchell, A. Z. Khokhar, S. A. Reynolds, D. J. Thomson, F. Y. Gardes, C. G. Littlejohns, G. T. Reed, and G. Z. Mashanovich, “Mid-infrared thermo-optic modulators in SoI,” IEEE Phot. Technol. Lett. **26** (13), 1352–1355, (2014).
11. B. J. Frey, D. B. Leviton, and T. J. Madison, “Temperature-dependent refractive index of silicon and germanium,” Proc. SPIE **6273**, 62732 (2006).
12. R. Soref, “Mid-infrared photonics in silicon and germanium,” Nat. Photonics **4**(8), 495-497 (2010).
13. M. Meuris, S. Arnauts, I. Cornelissen, K. Kenis, M. Lux, S. Degendt, P. Mertens, I. Teerlinck, R. Vos, L. Loewenstein, M. M. Heyns, and K. Wolke, “Implementation of the IMEC-Clean in advanced CMOS manufacturing,” in Proc. IEEE Int. Symp. Semicond. Manuf.(IEEE 1999), pp. 157–160.

---

1. Introduction

The germanium-on-silicon waveguide platform is a strong candidate for mid-ir photonic integration [1–2]. Its CMOS compatibility, simple fabrication scheme and wide range transparency (germanium is transparent up to 14 μm) make it a compelling solution compared to other mid-ir integration platforms proposed so far [3–5]. Recent demonstrations of low loss waveguides and various photonic components such as Mach-Zehnder interferometers (MZIs) [6], arrayed waveguide gratings (AWGs) [7] and planar concave gratings (PCGs) [8] show the versatility of the Ge-on-Si waveguide platform.

Tuning of integrated optical components is of critical importance in many applications. This tuning can be achieved by utilizing thermo-optic phase shifters where heat is generated in the vicinity of the waveguide, which affects the effective index of the optical mode [9–10]. Thermo-optic phase tuning is achieved by either placing a heater on top of the waveguide, which requires the deposition of an insulating layer of sufficient thickness, which optically isolates the mode in the waveguide from the heater or by placing the heater on the side of the waveguide, which avoids deposition of any intermediate cladding. In this paper, we describe the realization of side-integrated thermo-optic phase shifters for mid-ir photonic integrated circuits.

2. General considerations

The heater structures were implemented on a germanium-on-silicon waveguide platform using a 2 μm thick germanium waveguide layer. The waveguides were etched through the germanium layer and were 2.2 μm wide, making them single mode in the 5 μm wavelength range. The details on the fabrication and measurement of Ge-on-Si PICs can be found in [7]. We designed the heaters in a side heating configuration as schematically shown in Fig. 1. The heater itself consisted of a 2 μm wide and 100 nm high metal stack (Ti/Au or Cr/Au) deposited on a 4 μm wide germanium strip. The distance between the waveguide and neighboring germanium heater was chosen to be 2 μm, as this is the limit of the lithography tool used in our experiments.

The thermal simulations were performed using COMSOL multiphysics. We performed steady state FEM 3-D simulations to calculate the temperature change as a function of dissipated power in the heater. In Fig. 1, a zoomed version of the simulation window is shown where the spatial distribution of the temperature in the waveguide and heater is shown for a specific power dissipated in the heater. In the COMSOL simulations, the substrate and the air top cladding were kept at a height of 200 μm and at a width of 400 μm. The length of the waveguide was always kept 400 μm additional to the length of the heater such that heat flow along the waveguide itself

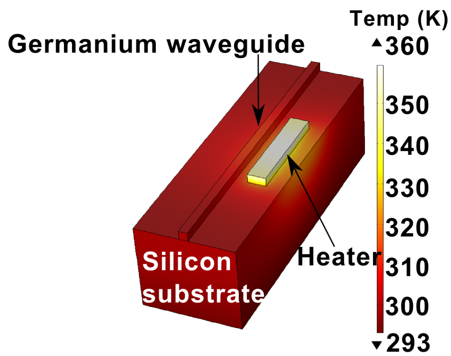

Fig. 1. (a) The 3-D simulation window showing the germanium waveguide and heater in a side heating configuration on a silicon substrate along with the spatial temperature distribution.

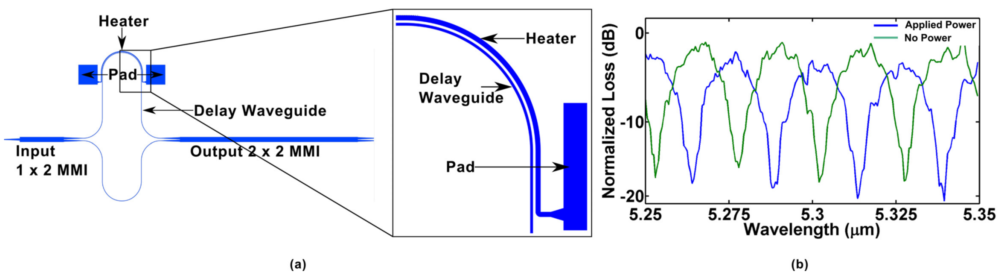

Fig. 2. (a) A schematic diagram showing the 1×2 MZI with heater in one of the arms along with the zoomed window showing the delay waveguide and the heater and (b) normalized spectra of the MZI with and without heater actuation.

can be taken into account. The temperature dependent thermo-optic coefficient of germanium was extracted from [11] for temperatures above 90 K as,

$$\frac{dn}{dT} = 8.2443.10^{-7}T + 0.00017234. \tag{1}$$

Since the optical confinement factor of the fundamental TM mode (the devices were designed for TM polarization for compatibility with quantum cascade laser integration) in the Ge waveguide core is 96%, only the thermo-optic effect in the Ge waveguide core is considered. To calculate the total phase shift introduced in the waveguide by dissipating a specific amount of power, we obtained the temperature profile as a line plot in the center of waveguide after, which the local refractive index change was calculated using equation 1. The total experienced phase change was then calculated through numerical integration along the waveguide as

$$\Delta\phi = \int_0^L \frac{2\pi}{\lambda}\Delta n(z)dz \tag{2}$$

where λ is the wavelength of operation, Δn(z) is the change in refractive index and L is the total length of the waveguide.

#222405 - $15.00 USD Received 3 Sep 2014; revised 30 Oct 2014; accepted 31 Oct 2014; published 7 Nov 2014

To experimentally asses the performance of the thermo-optic phase shifters, we designed 1×2 Mach Zehnder Interferometers (MZIs) in the 5 μm wavelength range with a fixed path length difference of 260 μm, which resulted in a free spectral range (FSR) of 25 nm. The length of the heater section was varied from 70 μm to 700 μm in steps of 70 μm and both ends were connected to 100 μm x 100 μm pads. The schematic diagram of the MZI is shown in Fig. 2(a) along with a zoomed window showing the heater and the delay waveguide. A typical measured transmission spectrum from the MZIs with and without heater actuation is shown in Fig. 2(b). The insertion loss is 0.5 dB and the extinction ratio is -19 dB. The shift in destructive interference points is used to experimentally determine the obtained phase shift.

3. Ge-on-Si phase shifters

3.1. Standard phase shifter

We performed a COMSOL simulation for the Ge-on-Si phase shifters as shown in Fig. 3(a) and found that one requires 700 mW of power to achieve a 2π phase shift. The heater consisted of a stack of Ti/Au on a germanium strip, the length of which was kept 700 μm and the corresponding temperature profile in the center of the waveguide along its length can be seen in Fig. 3(b). This simulation was then confirmed by measuring the induced phase shift as a function of applied power as shown in Fig. 3(c). A good match between theory and experiment can be observed.

We can immediately draw the conclusion that a heater designed in this configuration is very power inefficient. The main reason behind this is that the underlying silicon (thermal conductivity = 130 W/(m*K)) acts as a perfect heat sink, which can also be seen in the simulation in Fig. 3(a). An improvement in the design is thus needed to bring down the required tuning power. Since the majority of the heat is being sunk in the silicon substrate, a way to improve the efficiency of the thermo-optic phase shifter is by thermally isolating it from the silicon substrate.

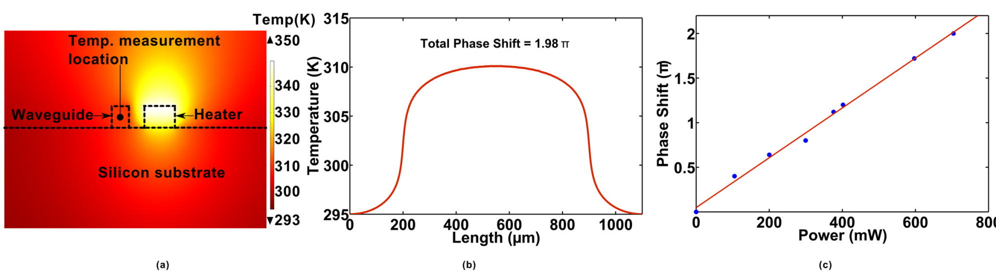

Fig. 3. (a) 2-D cross section in the middle of the simulation window, (b) line plot along the waveguide showing the temperature profile. The length of the heater was kept 700 μm and the power dissipated in the heater was 700 mW, (c) experimentally measured phase shift as a function of power dissipation along with the linear fit.

3.2. Fully undercut phase shifters

To prevent the heat to be sunk in the substrate, air trenches were created using a focused ion beam (FIB) tool on both sides of a heater/waveguide combination of length 210 μm as shown in Fig. 4(a). The rest of the chip was protected by photoresist and lithography was performed to define the areas where FIB is to be done. While in this prototype FIB was used, this undercutting can be realized on a wafer scale through chemically assisted ion beam etching. Fig. 4(b) shows the top view of the undercut heater (which consisted of a Ti/Au metal stack on a germanium

#222405 - $15.00 USD Received 3 Sep 2014; revised 30 Oct 2014; accepted 31 Oct 2014; published 7 Nov 2014

strip) and the waveguide section. The simulated 2-D cross section and the temperature profile along the waveguide can be seen in Fig. 5(a) and Fig. 5(b) respectively. We confirmed the simulation results by measuring the phase shift as a function of applied power and found that 80 mW of power is required to achieve a 2π phase shift as seen in Fig. 5(c).

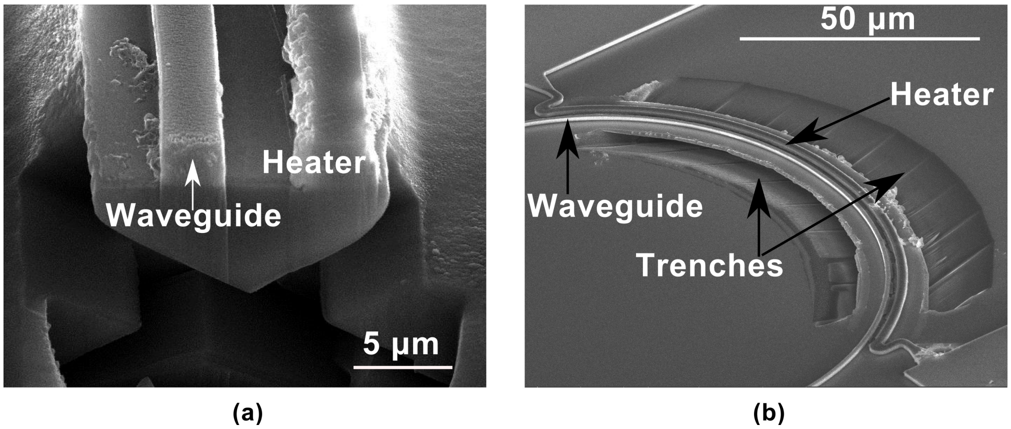

Fig. 4. (a) SEM image of fully undercut heater and (b) top view of a fully undercut heater.

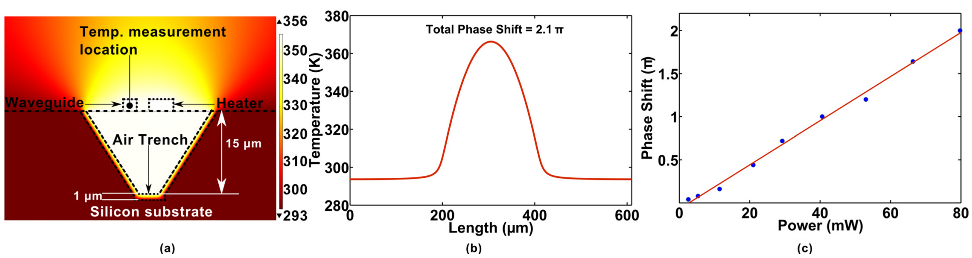

Fig. 5. (a) 2-D cross section in the middle of the simulation window of a fully undercut heater, (b) line plot along the waveguide showing the temperature profile. The length of the heater was kept 210 μm and the power dissipated was 80 mW, (c) experimentally measured phase shift as a function of power dissipation along with the linear fit.

4. Ge-on-SOI phase shifters

As seen in previous section, isolating the heater from the conducting silicon substrate substantially increases its efficiency. Although we have demonstrated a proof-of-principle concept using FIB, a more elegant way of solving this problem is to deliberately introduce a thermal insulator in the layer stack. Silicon dioxide (thermal conductivity = 1.4 W/(m*K)) can assist in confining the heat in the vicinity of the waveguide. Therefore we investigated Ge-on-Si-on-insulator as an alternative waveguide platform for realizing efficient thermo-optic phase shifters.

SiO_2 however has a disadvantage in the mid-ir wavelength range since it strongly absorbs beyond 4 μm wavelength [12]. Therefore, it must be ensured that the light traveling in the Ge waveguide core is not affected by the buried oxide. The simulation of the loss of the fundamental TM mode at 5.3 μm as a function of the underlying Si layer thickness is shown in Fig. 6

(assuming a 2 μm thick SiO_2). It can be seen that a Si thickness of 3 μm is sufficient to achieve low loss propagation.

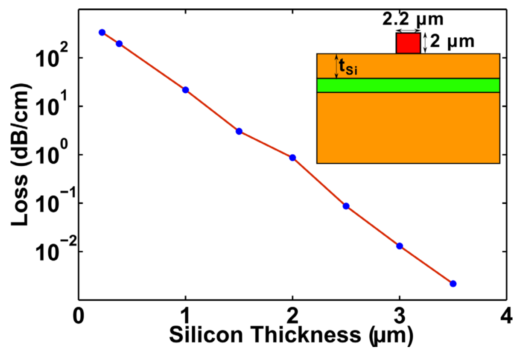

Fig. 6. Simulation showing the absorption loss of the fundamental TM mode at 5.3 μm in the germanium-on-SOI waveguide as a function of silicon thickness.

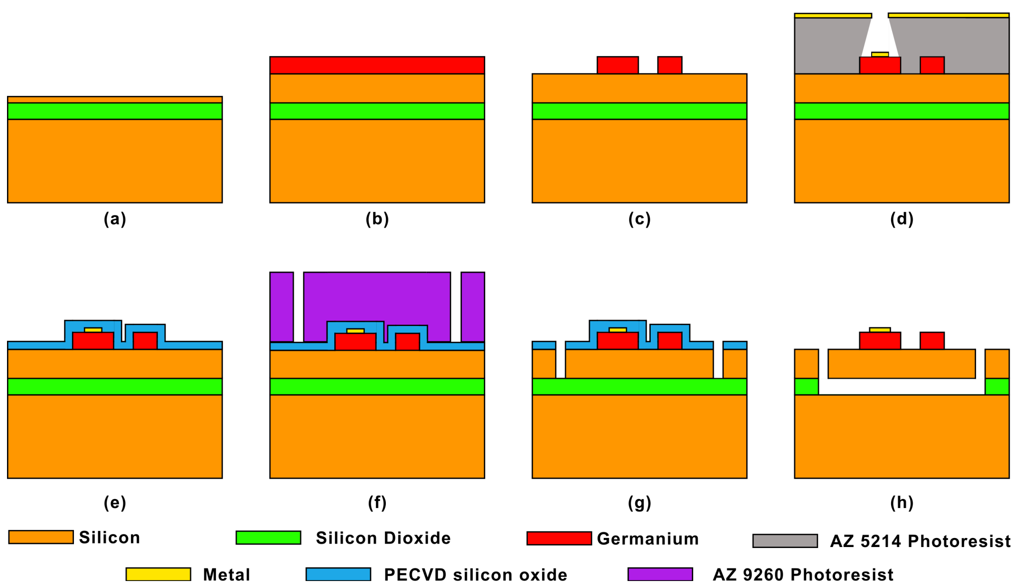

Fig. 7. Schematic fabrication scheme of Ge-on-SOI phase shifters (a) 200 mm SOI wafer with 220 nm silicon layer, (b) epitaxial growth of 3 μm thick silicon and 2 μm thick germanium layers, (c) waveguide definition by lift-off and dry etching, (d) lithography and metal deposition, (e) PECVD oxide deposition, (f) lithography for defining trenches, (g) dry etching of PECVD silicon oxide and silicon and (h) removal of PECVD oxide and buried oxide by HF dip

The fabrication scheme of Ge-on-SOI phase shifters is described schematically in Fig. 7. The process began with a 200 mm SOI wafer with 220 nm silicon thickness, which received an IMEC-clean [13]. 3 μm of silicon was then grown epitaxially in a horizontal, cold wall, load lock reactor (ASM Epsilon 2000). The in-situ bake at 1050°C removed all traces of oxygen. The silicon layer was grown at a temperature of 1050°C using dichlorosilane as silicon precursor and H_2 as carrier gas. The germanium layer was grown at 450°C using germane as precursor and H_2 as carrier gas. The wafer was then annealed at 800° C for three minutes to reduce

#222405 - $15.00 USD Received 3 Sep 2014; revised 30 Oct 2014; accepted 31 Oct 2014; published 7 Nov 2014

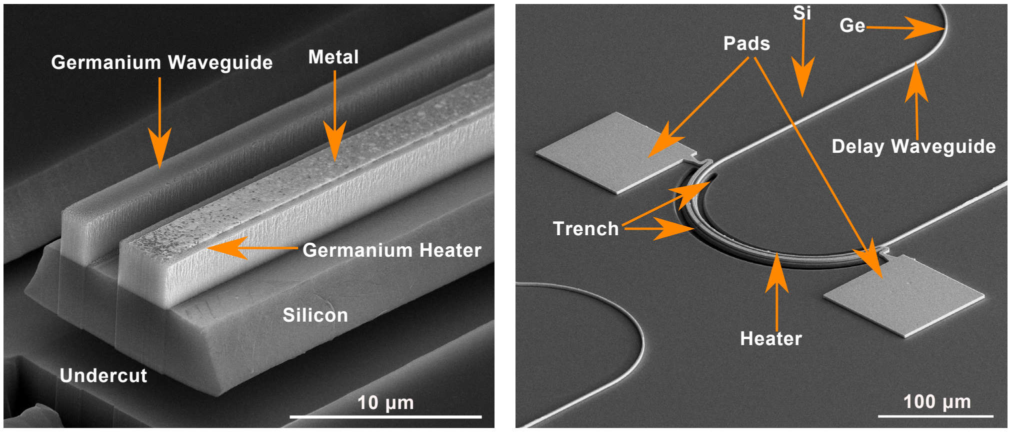

Fig. 8. SEM image showing (a) the cross section of the Ge-on-SOI waveguide where the underlying oxide has been removed and (b) top view of a MZI with a heater on one of the arms.

the threading dislocation density. The germanium waveguide and heater were defined using a metal mask, which was patterned using i-line lithography and lift-off. Germanium etching was carried out in a CF_4:O_2 plasma and the metal was removed by a HF dip. Metal lines on top of the germanium heaters were defined using a second lithography step and lift-off. A 500 nm layer of PECVD silicon oxide was deposited and trenches were defined in the silicon substrate using lithography and dry etching in a SF_6:O_2 plasma. Although a photoresist mask is sufficient to define the trenches, it was found that the photoresist can't be removed completely after dry etching due to photoresist plasma hardening. The PECVD oxide therefore serves as a sacrificial layer, which is removed via HF wet etching. The samples were then thinned and cleaved. To achieve even better isolation samples were put in HF to remove the underlying SiO_2. SEM images showing an undercut Ge-on-SOI heater section and the top view of such a heater incorporated in a MZI can be seen in Fig. 8(a) and Fig. 8(b) respectively.

The waveguide loss of Ge-on-SOI single mode waveguides (2.2 μm wide) was found to be 7 dB/cm in the 5.25 - 5.35 μm wavelength range as can be seen in Fig. 9. The origin of these higher losses compared to the values reported in Ge-on-Si [7] are not yet fully understood. Nevertheless such loss values are still sufficient to make mm-length scale integrated devices.

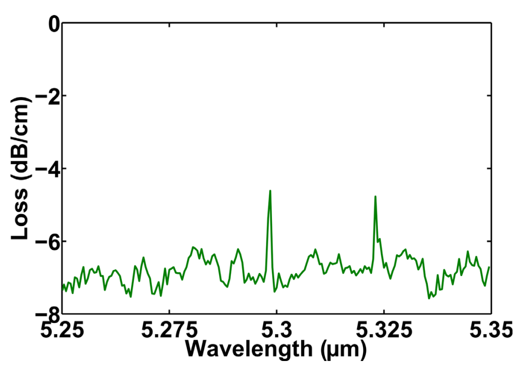

Fig. 9. Measured waveguide loss of Ge-on-SOI waveguides (2.2 μm wide waveguide) for TM polarization.

#222405 - $15.00 USD Received 3 Sep 2014; revised 30 Oct 2014; accepted 31 Oct 2014; published 7 Nov 2014

4.1. Ge-on-SOI phase shifters without undercut

To evaluate the performance of the Ge-on-SOI phase shifters, we performed previously described COMSOL simulations, the results of which are shown in Fig. 10(a) and Fig. 10(b). Since the undercut by FIB was done on a 210 μm long heater, we measured the phase shift as a function of dissipated heat on a heater (consisting of a Ti/Au metal stack on a germanium strip) of similar length as shown in Fig. 10(c) and found that the results match well with the simulations in Fig. 10(b). The heater performance as a function of length was also studied using COMSOL by calculating the tuning power required to achieve a phase shift of 2π and it was found that it decays rapidly at first becoming almost constant for longer heaters as shown in Fig. 11. This can be explained by the longitudinal flow of heat along the waveguide. As seen in the SEM image in Fig. 8(b), the heated waveguide is at its ends is connected to a 3.22 μm thick silicon slab (onto which the germanium waveguides are grown), which extends all over the circuit. This layer serves as an efficient heat spreader, which is the dominant source of heat sinking in the Ge-on-SOI phase shifters. This especially affects the shorter heaters since for longer devices the thermal resistance for the longitudinal heat flow becomes larger. This was also verified experimentally, the results of which are plotted together with the simulation results shown in Fig. 11.

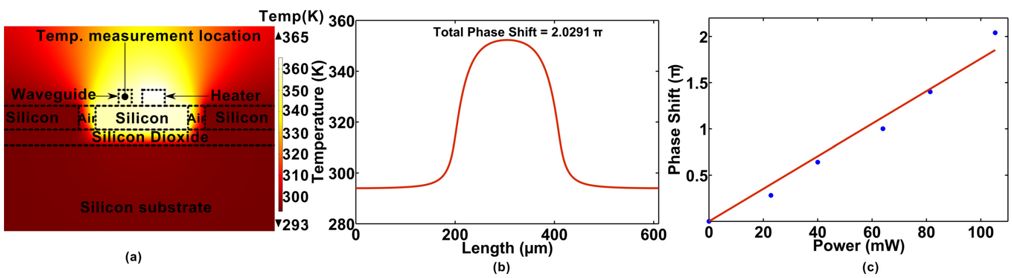

Fig. 10. (a) 2-D cross section in the middle of the simulation window of a Ge-on-SOI heater, (b) line plot along the waveguide showing the temperature profile. The length of the heater was kept 210 μm and the power dissipated was 100 mW. (c) experimentally measured phase shift as a function of power dissipation along with the linear fit.

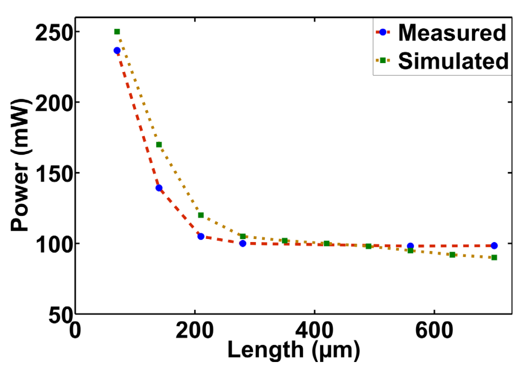

Fig. 11. Tuning power to achieve 2π phase shift as a function of length for a Ge-on-SOI phase shifter without undercut.

#222405 - $15.00 USD Received 3 Sep 2014; revised 30 Oct 2014; accepted 31 Oct 2014; published 7 Nov 2014

4.2. Ge-on-SOI phase shifters with undercut

As described previously, the efficiency of the heater will increase if it is thermally isolated from the highly conducting silicon substrate. To enhance this, we removed the buried oxide using HF etching and carried out the measurements of the phase shift as a function of applied power for a heater of length 210 μm. The heaters consisted of a Cr/Au metal stack on a germanium strip. We chose Cr instead of Ti as Ti would be etched away by HF while performing the undercut. The COMSOL simulation in Fig. 12(a) and Fig. 12(b) suggest that a power of 20 mW would be needed to achieve the 2π phase shift, which is confirmed by the measurements in Fig. 12(c). For heaters longer than 280 μm, it was observed that the free standing germanium waveguide and heater start bending and touch the substrate, which results in a parasitic heat sinking path, which hence again increases the required heating power as shown in Fig. 13. Taking into account this bending, the optimum configuration consists of a 280 μm long phase shifter, which dissipates 16 mW of power for a 2π phase shift. The simulation of the tuning power required for a 2π phase shift as a function of heater length can also be seen in Fig. 13, which indicates that the graph would follow a similar trend as described in previous section, if the free standing section would not bend and touch the silicon substrate. Here the only heat flow is along the waveguide as the undercut completely isolates the heater from the silicon substrate underneath.

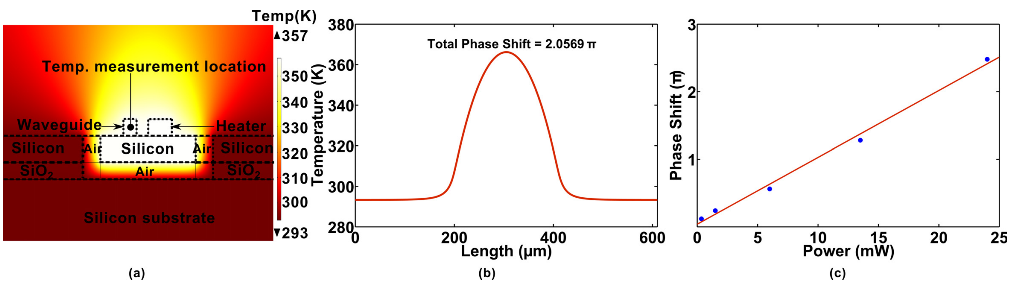

Fig. 12. (a) 2-D cross section in the middle of the simulation window for an undercut Ge-on-SOI phase shifter, (b) line plot along the waveguide showing the temperature profile. The length of the heater was kept 210 μm and the power dissipated was 20 mW. (c) experimentally measured phase shift as a function of power dissipation along with the linear fit.

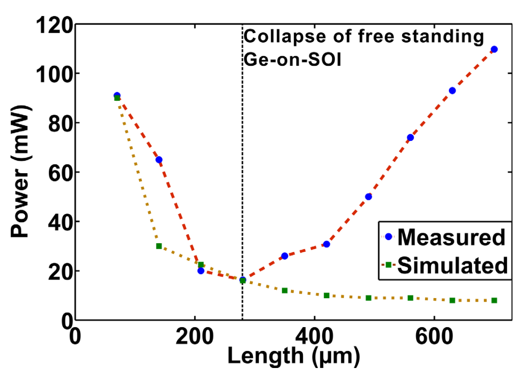

Fig. 13. Tuning power to achieve 2π phase shift as a function of length for a Ge-on-SOI phase shifter with undercut.

#222405 - $15.00 USD Received 3 Sep 2014; revised 30 Oct 2014; accepted 31 Oct 2014; published 7 Nov 2014

5. Conclusion

In conclusion, we have demonstrated thermo-optic phase shifters for the mid-ir for the first time on the Ge-on-Si and Ge-on-SOI waveguide platform. Thermo-optic phase shifters in different configurations have been studied and a new waveguide platform (Ge-on-SOI) has been demonstrated which brings down the required tuning power for a 2π phase shift from 700 mW to 16 mW. This paves the way to the power efficient tuning of mid-infrared photonic integrated circuits.

Acknowledgments

This work was supported by FP-7-ERC MIRACLE. Yosuke Shimura would like to thank FWO for a Pegasus scholarship.