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Photonic Reservoir Computing in Si Chips

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Reservoir computing is a decade-old framework from the field of machine learning to use and train recurrent neural networks. This technique has been among the state-of-the-art for a broad class of problems such as time-series prediction, speech recognition and robot control. However, so far implementations have been mainly software-based, while a hardware implementation in photonics offers the promise of being low-power and fast.

We will show experimental and theoretical results on the use of a generic photonic reservoir on a silicon-on-insulator chip, which can be used to perform arbitrary digital calculations involving input from up to four bit periods in the past, as well as header recognition of sequences of 5 or 6 bits. Using simulations, we also show that such a network can handle more analog tasks like speech recognition and the cleaning up of signals after they pass through a noisy and dispersive channel.

The silicon photonics chip we propose is purely passive, which is beneficial for power consumption. Also, the technology can be easily scaled up to speeds above 100 Gbps.

Biographical sketch

Peter Bienstman was born in Ghent, Belgium, in 1974. He received a degree in electrical engineering from Ghent University, Belgium, in 1997 and a Ph.D. from the same university in 2001, at the Department of Information Technology (INTEC), where he is currently a full professor. His research interests include several applications of nanophotonics (biosensors, photonic information processing, ...) as well as nanophotonics modelling. He has published over 110 papers and holds several patents. He has been awarded an ERC starting grant for the Naresco-project: Novel paradigms for massively parallel nanophotonic information processing.

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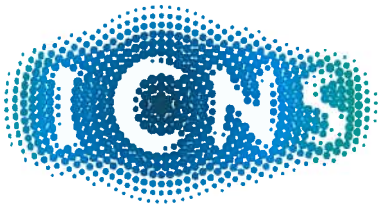

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