High Extinction Ratio Hybrid Graphene-Silicon Photonic Crystal Switch

Leili Abdollahi Shiramin[ID], Weiqiang Xie, Brad Snyder, Peter De Heyn, Peter Verheyen, Gunther Roelkens, and Dries Van Thourhout

Abstract—In this letter, we demonstrate a compact optical switch realized by integrating a graphene layer with a silicon photonic crystal cavity fabricated using deep UV immersion lithography and a novel transfer printing approach. A 17-dB extinction ratio and 0.75-nm shift in the cavity resonance are measured for a swing voltage of only 1.2 V. The graphene layer is limited to 1 × 5 μm in size. The experimental results are linked to a theoretical model and used to predict possible improvements to the design.

Index Terms—Graphene, optical switch, photonic crystals, silicon photonics.

I. INTRODUCTION

SHIFTING the Fermi level of a graphene layer by an externally applied electric field or chemical doping allows tuning the optical absorption through Pauli blocking [1]. Exploiting this property and combining graphene with Silicon nano-photonics structures has led to the demonstration of a diverse range of electro-optical switches and modulators with compact size. Several waveguide integrated graphene devices have already been studied theoretically [2]–[4] and demonstrated experimentally [4]–[10]. However, to reach a high extinction ratio (*ER*), the graphene layer has to be sufficiently long. Values for the *ER* varying between 2 and 6 dB for devices with graphene length varying from 30 to 50 μm were reported [4]–[7]. This leads to a high capacitance and associated lower modulation bandwidth and high power consumption.

Integrating graphene with resonant structures enhances the interaction of the optical field with the graphene layer [11]–[13], resulting in a reduced size of the required graphene layer and the associated capacitance. This is in particular the case for photonic crystal cavities. Earlier work focused on 2D-photonic crystal cavities, addressed in a surface

L. Abdollahi Shiramin, G. Roelkens, and D. Van Thourhout are with the Photonics Research Group, Department of Information Technology, Ghent University–imec, 9000 Ghent, Belgium (e-mail: leili.abdollahishiramin@ ugent.be; gunther.roelkens@ugent.be; dries.vanthourhout@ugent.be).

W. Xie is with the Optoelectronic Research Group, Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93106 USA (e-mail: weiqiangxie@ ece.ucsb.edu).

B. Snyder, P. De Heyn, and P. Verheyen are with imec, 3001 Leuven, Belgium (e-mail: brad.snyder@imec.be; peter.deheyn@imec.be; peter.verheyen@imec.be).

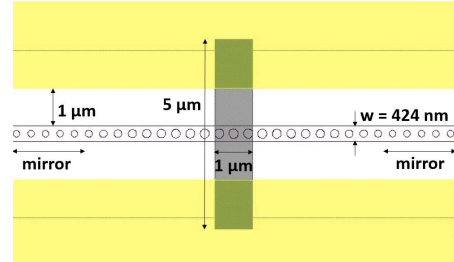Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Fig. 1. Schematic of the graphene-based switch showing the graphene layer on three central holes only and metal pads with 1 μm spacing from the cavity.

normal configuration however. Although up to 10 dB ER was demonstrated the surface normal configuration limits the practical applicability and possibility for integration with other devices. This earlier work did also not discuss insertion loss (IL) and, even more importantly, the optimization of the fundamental trade-off between IL and ER in these devices. Finally, in this earlier work, underetching of the cavity was required limiting the structural stability. In the current work we focus on a 1D-photonic crystal cavity, which is addressed through an integrated waveguide. This allows us to accurately characterize ER and IL. Even without underetching, sufficient optical confinement is reached to reduce the graphene area from 30 μm^2 in previous work [12] to 5 μm^2, especially important for enhancing the modulation speed and reducing the power consumption in the future. Moreover, the device is fabricated using a novel transfer printing process. We thereby use an automated commercial transfer printer to integrate a micron-scale graphene layer with a 1D silicon photonic crystal, while in previous works [11], [12] the graphene transfer method relied on manual processes. The importance of this new method lies in the fact that it allows to transfer small patches of graphene on a given location on a preprocessed wafer, in a cost efficient way. This could be important if the wafer has considerable topography, or if also other materials (III-Vs, other 2Ds, …) need to be transferred. In the next section, we present the experimental results, demonstrating a voltage dependent transmission for the hybrid graphene SOI-PhC nano-cavity. The graphene Fermi level is tuned from its intrinsic state to beyond the transparency region by gating the graphene layer using a polymer electrolyte [14]. Finally, we link these results with a theoretical model and predict possible improvements to the design to fabricate a compact electro-absorption modulator with co-optimized *ER*, *IL* and speed.

II. DESIGN AND FABRICATION

Fig. 1 illustrates the designof the proposed device. It consists of a 1-D SOI-PhC nano-cavity with a patterned
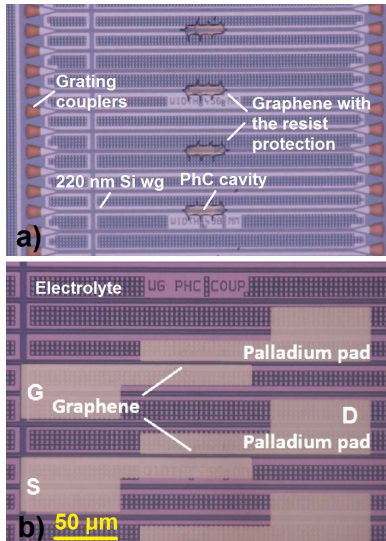
Fig. 2. (a) Top view of the Si sample with the transferred coupons on top. To provide enough space for contacts, only a subset of the cavities are covered with a graphene layer. (b) Top view of a fully fabricated device. An electrolyte layer has been coated on the sample to gate the graphene layer. Given its small size and transparency, the graphene layer is not visible in this image.

graphene layer deposited on top. Metal contacts are deposited at both sides of the graphene layer, 1 μm away from the edges of the cavity. The SOI-PhC nano-cavities consist of two mirror sections with identical holes and a taper section in between. The radius of the holes in the taper section gradually decreases from the center to both sides. The devices are fabricated on a 300 mm SOI wafer in a CMOS pilot line using 193 nm immersion lithography. The holes and waveguides are etched in a 220 nm-thick silicon layer on top of a 2 μm buried silicon oxide layer. The devices are planarized by SiO_2 deposition and chemical mechanical polishing (CMP).

After fabrication of the SOI-PhC nano-cavity, graphene is transfer printed on top using the process described in [15] and [16]. We first fabricate micron-size patterns of graphene on a source substrate using photolithography and an oxygen plasma process. The source substrate consists of a CVD grown graphene layer transferred on a 300nm SiO_2 layer obtained from Graphenea [17]. Photo-resist tethers are then fabricated in a second lithography step. Next, the graphene layer is under-etched and a suspended resist-graphene stack is formed (hereafter called a "coupon"). The resist both serves as a protection layer for the graphene and to form the tethers that are used to hold the suspended graphene layer. Using a PDMS stamp with a protruding post, installed in a commercial transfer printer (X-celeprint, model μTP-100), the coupons are then picked up and placed on the cavity [Fig. 2(a)]. Subsequently, the protective resist is removed with acetone. More detail about the graphene transfer process can be found in [15] and [16]. The next step is to fabricate the palladium contact pads on the graphene layer, 1 μm away from the cavity edges. After the lift-off process, a polymer electrolyte layer consisting of LiClO4 and polyethylene oxide (PEO) in a weight ratio of 1:10 is spin coated on the Si chip. This layer will allow to control the graphene Fermi-level [18]. Fig. 2(b) shows a microscope image of the fully fabricated device.
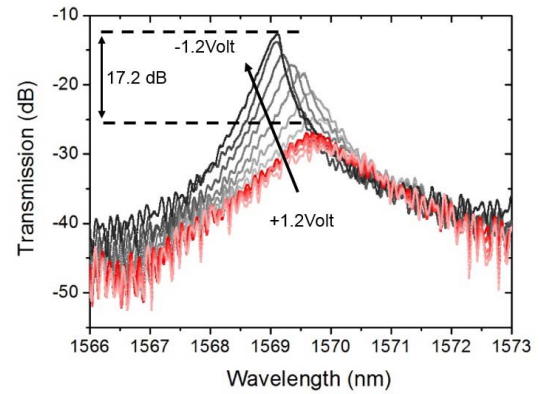

Fig. 3. Transmission spectrum of the hybrid graphene SOI-PhC cavity for different gate voltages.
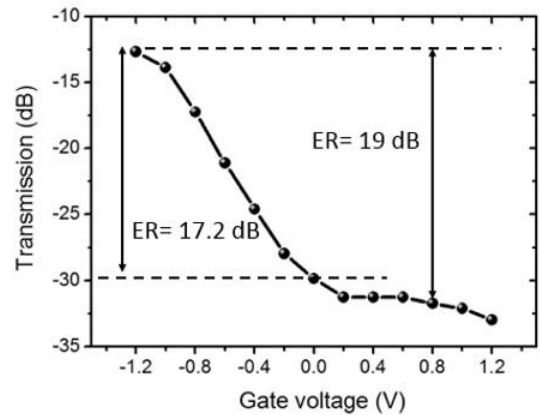

Fig. 4. Transmission at the resonance wavelength of −1.2 Volt versus gate voltage.

III. Characterization of the Device Performance

The 1D PhC device is connected to single mode access waveguides integrated with grating couplers for optical characterization. The graphene Fermi level is tuned by applying a gate voltage V_{gs} between one of the contacts of the device under study and a contact of an identical device directly next to it, with the electrolyte serving as the gate dielectric. Fig. 3 plots the measured transmission for applied gate voltages varying from +1.2 Volt to −1.2 Volt. The transmission increases and the linewidth narrows as the voltage becomes more negative. This indicates the graphene layer becomes more transparent, as expected. It is also possible to apply a voltage higher than −1.2 Volt and hence obtain higher ER. For positive voltages, this effect is weaker as the transferred graphene is intrinsically p-doped.

Fig. 4 shows the ER, measured at 1569.07 nm, the wavelength of maximum transmission for an applied voltage of −1.2 Volt. This figure shows that applying only −1.2 Volt results already in an extinction ratio (ER) as high as 17.2 dB. Increasing the drive voltage to 2 Volt, from −1.2 to 0.8 Volt (the neutrality point of graphene), the ER further increases to 19 dB. The low drive voltage required is related to the small thickness of the the Debye layer [19] forming at the interface between the graphene layer and the ionic liquid, acting as the parallel plate capacitor in this case.

The gate voltage dependent quality factor is extracted by fitting a Lorentzian function to the transmission spectra.
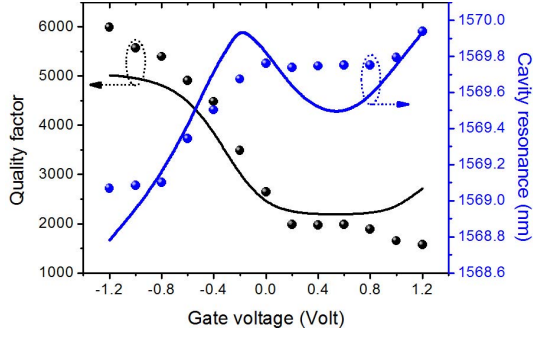
Fig. 5. Quality factor and resonance wavelength versus gate voltage. Solid lines and scatter data represent the theoretical model and measurement data, respectively.
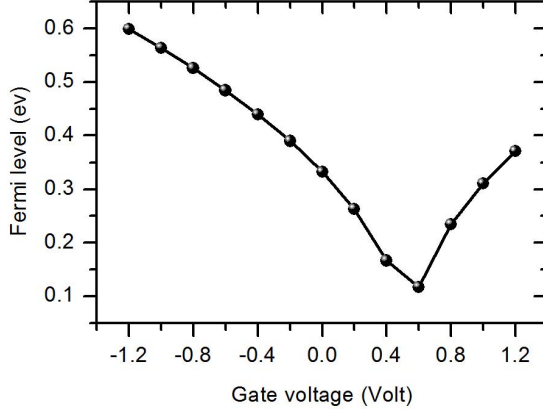

Fig. 6. Fermi level versus gate voltage.

It increases from 2000 at positive voltages to about 6000 at −1.2 Volt (Fig. 5). The corresponding wavelength shift is 0.8 nm. The Q factor enhancement with the gate voltage originates from the decrease in the graphene absorption coefficient. The strong blue shift indicates there is not only a strong modulation of the imaginary part of graphene's dielectric constant but also of its real part, resulting in a phase shift. In line with what is expected from theory [4], this change in the real part is in particular relevant if the chemical potential comes close to 0.4 eV, or for gate voltages below 0 Volt.

Using a perturbative approach, the cavity resonance and its line width can be expected to vary linearly with the gate-dependent dielectric constant of graphene: $\Gamma_R = \Gamma_R^0 + \alpha Im[\varepsilon_g(\omega)]$ for the cavity line width and $\lambda_R = \lambda_R^0 + \beta Re[\varepsilon_g(\omega)]$ for the cavity resonance wavelength [11]. To link the experimental data to a theoretical model for the graphene dielectric constant [20], we need to relate the actually applied gate voltage to the Fermi level of the graphene layer, using the following formula [11]:

$$E_f = \hbar v_f \sqrt{n_0 + \pi \left(\frac{C|V|}{q} \right)} \qquad (1)$$

with C the capacitance related to the depletion layer in the ionic gel, n_0 the intrinsic carrier density and v_f the fermi velocity. Fitting the experimental data to the theoretical model gives us the following values for the different parameters: $\alpha \sim 0.12$, $\beta \sim 0.4$, $C \sim 27$ mF/m^2, $n_0 \sim 9e12$ cm^{-2} and $\Gamma \sim 26$ fs with Γ the scattering time. In Fig. 6 we plot the corresponding relation between E_f and V, showing
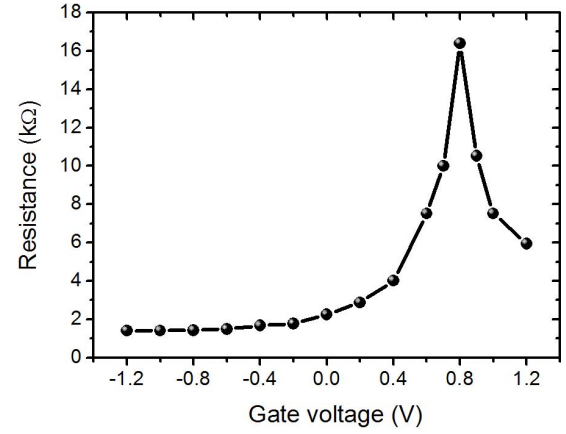

Fig. 7. Resistance as function of gate voltage. The maximum resistance indicates the neutrality point, where graphene has minimum conductivity and minimum carrier density.

the neutrality point at 0.6 Volt. Another observation is that for positive voltages the Fermi level does not reach the transparency region (<0.4 eV) explaining the absorptive behavior of graphene in the transmission spectra for positive voltages (Fig. 3).

We also measured the gate voltage dependent resistance using the source and drain contact pads on both side of the graphene layer (Fig. 7). A maximum resistance of 17 KΩ is measured for a gate voltage of 0.8 V, corresponding to the neutrality point and in line with was obtained from the optical data.

Ideally, in all measurements the Dirac point should be obtained at the same applied voltage. However, the optical (Fig. 6) and electrical measurements (Fig. 7) were not carried out simultaneously and the results obtained with the ionic gel are not 100% reproducible between different measurements (due to aging of the applied ionic gel). In future implementations whereby either the silicon or a second graphene layer is used for gating and this should be no issue.

Another but less important reason is that in the calculation of fermi level (Fig. 6), we have used the parameters extracted from fitting the optical data to a theoretical model. This fit is not perfect as can be seen in Fig. 5 where the theoretical curve does not exactly overlap the experimental data. Also this causes a small error in the calculation of the fermi level and thus a small shift in the Dirac point.

The current device exhibits an excellent ER but also a relatively large IL. To get insight in this trade-off and evaluate possible design improvements we used a model based on standard coupled mode theory [21]. The measured Q-factor can be written as:

$$\frac{1}{Q} = \frac{1}{Q_c} + \frac{1}{Q_g} + \frac{1}{Q_i} \qquad (2)$$

Q_i is related to intrinsic scattering losses of the cavity and found to be very large ($>>$1E5) for the devices under study. Q_i will hence be neglected in the remainder of this discussion. Q_c is a design parameter and related to the strength of the mirror sections of the 1D PhC. Q_g is related to the absorption loss in the graphene layer and hence voltage dependent.
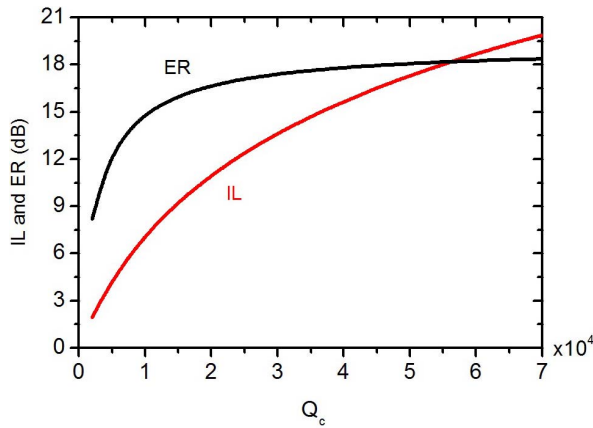
Fig. 8. *ER* and *IL* versus Q_c calculated from the coupled mode theory.

To extract the actual values for Q_c and Q_g we fit the voltage dependent maximal transmission to the following model:

$$T_{max}(V) = |\frac{1/Q_c}{1/Q_c + 1/Q_g(V)}|^2 \quad (3)$$

We find $Q_g(V) = Q/(1 - \sqrt{T_{max}(V)})$ and Q_g varies from about 1000 to 8000 for the voltage varying from $+1.2$ Volt to -1.2 Volt. We also find $Q_c = Q/\sqrt{T_{max}(V)}$. Using the experimental data for $Q_g(V)$ we can now calculate how the *ER* and *IL* would vary for an optimized Q_c. The results are plotted in Fig. 8. One can observe that ER increases steeply for small values of Q_c but then remains almost constant for $Q_c > 2 \times 10^4$. The *IL* on the other hand continuously increases with Q_c. Therefore, the design of the cavity can be optimized by reducing the strength of the mirror section. E.g. for $Q_c = 3500$, it is possible to obtain a good *ER*$\sim$ 10dB while reducing the *IL* below 3dB, taking into account the current quality of the graphene layer. Further improvements are expected for higher quality graphene.

To estimate the device energy consumption, the energy $E = CV^2/2$ required to charge (discharge) the graphene capacitor, where C is the device capacitance and V is the swing voltage can be calculated [11]. With the parameters obtained from fitting the cavity resonance and Q factor to the theoretical models, we find the electrolyte induces a capacitance density of 27 mF/m^2 on the graphene sheet. The graphene area is 5 μm^2, finally resulting in a switching energy of 97 fF for a swing voltage of -1.2 Volt (equivalent with 17.2 dB extinction ratio).

IV. CONCLUSION

We fabricated a wavelength selective switch by integrating graphene with a 1D Si PhC cavity. Graphene was transferred using a new transfer printing method exploiting a commercial transfer printer. The method involves defining suspended graphene coupons on a source substrate and subsequently transferring these using a PDMS stamp to the target substrate in an automatic fashion. Next, we demonstrated switching of the hybrid graphene PhC device demonstrating an *ER* of 17 dB for a voltage swing of only 1.2 Volt. In addition, a 0.75 nm shift in the cavity resonance and an increase in the Q factor from 2000 to 6000 were observed. The experimental results were fitted to a theoretical model allowing us to extract the intrinsic parameters of the device. By combining these with a model based on coupled mode theory we predict how design improvement can result in an improved tradeoff between *IL* and *ER* for the device. Another important feature of the device is the small size of the graphene capacitor, offering potential for low power consumption and high speed operation.

REFERENCES

[1] A. H. C. Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. Mod. Phys.*, vol. 81, no. 1, p. 109, 2009.

[2] L. A. Shiramin and D. Van Thourhout, "Graphene modulators and switches integrated on silicon and silicon nitride waveguide," *IEEE J. Sel. Topics Quantum Electron.*, vol. 23, no. 1, Jan./Feb. 2017, Art. no. 3600107.

[3] J. Gosciniak and D. T. H. Tan, "Theoretical investigation of graphene-based photonic modulators," *Sci. Rep.*, vol. 3, p. 1897, May 2013.

[4] Y. Hu *et al.*, "Broadband 10 Gb/s operation of graphene electro-absorption modulator on silicon," *Laser Photon. Rev.*, vol. 10, no. 2, pp. 307–316, 2016.

[5] H. Dalir, Y. Xia, Y. Wang, and X. Zhang, "Athermal broadband graphene optical modulator with 35 GHz speed," *ACS Photon.*, vol. 3, no. 9, pp. 1564–1568, 2016.

[6] M. Liu *et al.*, "A graphene-based broadband optical modulator," *Nature*, vol. 474, pp. 64–67, Jun. 2011.

[7] M. Liu, X. Yin, and X. Zhang, "Double-layer graphene optical modulator," *Nano lett.*, vol. 12, no. 3, pp. 1482–1485, 2012.

[8] L. Yu, J. Zheng, Y. Xu, D. Dai, and S. He, "Local and nonlocal optically induced transparency effects in graphene-silicon hybrid nanophotonic integrated circuits," *ACS Nano*, vol. 8, no. 11, pp. 11386–11393, 2014.

[9] J. Wang *et al.*, "High-responsivity graphene-on-silicon slot waveguide photodetectors," *Nanoscale*, vol. 8, pp. 13206–13211, Apr. 2016.

[10] Z. Cheng, H. K. Tsang, X. Wang, K. Xu, and J.-B. Xu, "In-plane optical absorption and free carrier absorption in graphene-on-silicon waveguides," *IEEE J. Sel. Topics Quantum Electron.*, vol. 20, no. 1, Jan./Feb. 2014, Art. no. 4400106.

[11] A. Majumdar, J. Kim, J. Vuckovic, and F. Wang, "Electrical control of silicon photonic crystal cavity by graphene," *Nano Lett.*, vol. 13, no. 2, pp. 515–518, 2013.

[12] X. Gan *et al.*, "High-contrast electrooptic modulation of a photonic crystal nanocavity by electrical gating of graphene," *Nano Lett.*, vol. 13, no. 2, pp. 691–696, 2013.

[13] L. A. Shiramin *et al.*, "Electrically tunable absorption in graphene-integrated silicon photonic crystal cavity," in *Proc. IEEE 14th Int. Conf. Group IV Photon. (GFP)*, Aug. 2017, pp. 181–182.

[14] V. Thareja *et al.*, "Electrically tunable coherent optical absorption in graphene with ion gel," *Nano Lett.*, vol. 15, no. 3, pp. 1570–1576, 2015.

[15] L. A. Shiramin *et al.*, "Transfer printing of micron-size graphene for photonic integrated circuits and devices," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 7, pp. 435–439, 2017.

[16] L. A. Shiramin *et al.*, "Demonstration of a new technique for the transfer printing of graphene on photonic devices," in *Proc. Conf. Lasers Electro-Opt. (CLEO)*, San Jose, CA, USA, 2017, paper SW4K.6.

[17] *CVD Graphene Growth.* Accessed: 2017. [Online]. Available: http://www.graphenea.com

[18] M. Mohsin, D. Schall, M. Otto, B. Chmielak, S. Suckow, and D. Neumaier, "Towards the predicted high performance of waveguide integrated electro-refractive phase modulators based on graphene," *IEEE Photon. J.*, vol. 9, no. 1, Feb. 2017, Art. no. 7800507.

[19] A. Das *et al.*, "Monitoring dopants by Raman scattering in an electrochemically top-gated graphene transistor," *Nature Nanotechnol.*, vol. 3, pp. 210–215, Feb. 2008.

[20] G. W. Hanson, "Dyadic Green's functions and guided surface waves for a surface conductivity model of graphene," *J. Appl. Phys.*, vol. 103, no. 6, p. 064302, 2008.

[21] S. Fan, W. Suh, and J. D. Joannopoulos, "Temporal coupled-mode theory for the Fano resonance in optical resonators," *J. Opt. Soc. Amer. A, Opt. Image Sci.*, vol. 20, no. 3, pp. 569–572, 2003.