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# Heterogeneous integration of GaSb on Ge-SOI photonic integrated circuits for SWIR applications

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***Abstract*—We report on the development of a germanium-on-SOI platform for short-wave-infrared applications. Heterogeneous integration of GaSb opto-electronic devices via micro-transfer-printing is reported.**

***Keywords*—Laser integration, micro-Transfer-Printing, Germanium, short-wave-infrared**

## I. INTRODUCTION

Heterogeneously integrating III-V materials on silicon photonic integrated circuits (PICs) has emerged as a promising approach to make laser sources on silicon, where InP and GaAs are the two III-V material systems of interest for the telecommunication wavelength window (1.3 or 1.55 µm, O-band or C-band). On the other hand, outside of the C-band and O-band, there are many other potential applications where PIC technology could play an important role.

For example, the short-wave infrared (SWIR) wavelength range and especially the 2-2.5 µm range is of particular interest for spectroscopic sensing applications [1]. Various molecules including glucose, lactate, urea and ethanol have absorption peaks in this spectral region. Therefore SWIR lasers and photodiodes are of great interest.

In recent years, GaSb, as the 4th generation of the III-V material, has proven its excellent electrical and optical properties in the SWIR range [2-4]. Compared to the InP system, GaSb can probe further into the SWIR and has better performance diode lasers in the 2-2.5 µm range [5]. However, adiabatically coupling light between GaSb-based diode structures and SOI waveguides is difficult, because of the high refractive index of the GaSb material system. Thus, a high-index bridging layer is needed to tackle this problem. Here, we present a solution with a Germanium-on-SOI (Ge-SOI) platform, where the germanium layer functions as a bridging layer. We have patterned and characterized essential optical building blocks such as waveguides and microring resonators (MRRs) by electron-beam lithography. We integrate the GaSb opto-electronic device structures on the Ge-SOI platform via micro-transfer-printing (µTP) technology [6]. This technology allows for the efficient use of III-V materials and enables pre-testing of the devices on the source wafers and the integration of a wide range of materials/devices on wafer scale in a massively parallel way.

## II. DESIGN & SIMULATION

### *A. The Ge-SOI platform*

The Ge-SOI wafers are prepared by imec. We begin with 200 mm SOI wafers with 220 nm Si waveguide layer thickness (on top of 2000 nm buried oxide) on which a 500 nm film of Ge is directly grown. The difference in lattice constants of Ge and Si is 4.2%, which typically results in a threading dislocation density of $10^6$–$10^7$ cm$^{-2}$ [7], which will have an impact on the losses of the Ge waveguides.

### *B. Principle of µTP*

There are various methods to realizing the heterogeneous integration of III-V amplifiers onto a passive PIC, and here we realize it via µTP. The main process flow is described in Fig. 1. The main modification in the III-V wafer to enable the micro-transfer printing is that we embed a release layer (which will be etched away eventually) between the substrate and active epi stack indicated as the green layer in Fig. 1(a). After the device layer has been patterned (Fig. 1(b)), a 600 nm SiNx layer is deposited and patterned to form tethers that will hold the device in place during release etch. Additional photoresist protection is applied to planarize the coupon. The release layer (1500nm of InAsSb) is then selectively etched away using a citric acid:$H_2O_2$ solution at 60°C. The coupons at this point are released and held by the SiNx tethers (Fig. 1(c)). To transfer-print these coupons to the Ge-SOI platform, a dedicated PDMS stamp is applied with the same size as the coupon, using an X-Celeprint *µ*TP-100 tool. The PDMS stamp will pick-up the coupon from the source wafer by retracting the stamp and print it on the Ge-SOI wafer by laminating the stamp to the target substrate, where the Ge waveguide is already being patterned. To ensure a high printing yield, the target sample is spin-coated with a DVS-BCB: mesitylene 1:4

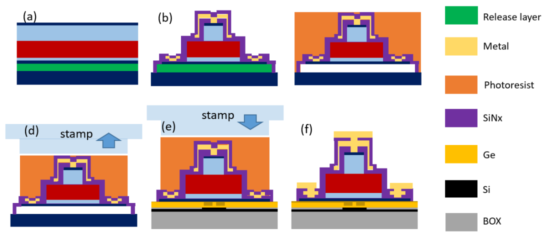

Fig. 1. Process flow of the integration of GaSb amplifier coupons onto Ge-SOI platform via micro-transfer printing.

solution at 3000 rpm, soft baked at 150℃. This bonding material will eventually form a 30-50 nm bonding layer between the III-V coupon and Ge waveguide. Finally, the contacts are opened and an additional metallization is applied to enable wire-bonding or probing (Fig. 1(f)).

### *C. Coupling between Ge and GaSb multiple quantum well (MQW) waveguides*

We designed a 3-stage fast-slow-fast varying taper to realize an adiabatic evanescent coupling between the GaSb MQW and Ge waveguide. We focus on 2.3 micron as the working wavelength for our laser, as several interesting spectroscopic sensing applications are possible around this wavelength. The Ge rib waveguide is 1.1 um wide with an etch depth of 300 nm. We taper down the waveguide to 0.9 µm with a length of 50 µm for the first fast-varying part. The mode is still primarily confined in the Ge waveguide in the first taper. In the slow varying region, we taper the width down from 0.9 to 0.75 µm, where the mode is becoming a super mode and starting to be confined in the MQW region. We further taper down the Ge taper to 0.5 um over a length of 50 µm, making sure the mode is completely confined in MQW region. By sweeping the length of the slow varying taper, it turned out that with a length of 200 µm, a 90% coupling efficiency could be achieved. The GaSb waveguide structure is 4 micron wide and etched down to the SCH layer.

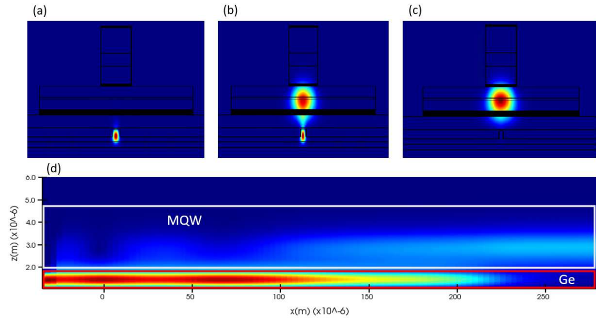

Fig. 2. EME simulation: Mode transition from Ge to GaSb MQW waveguide.

## III. RESULTS

### *A. Performance of Ge waveguide and MRRs*

The Ge waveguide shows a loss of 3.9 dB/cm at 2.3 micron wavelength, which is due to the dislocations at the Ge-Si interface. Given that the tapering region is 600 µm long in total in the laser cavity (because of two taper structures) , the actual loss would be less than 0.3 dB. Based on the same waveguide dimensions, we also fabricated MRRs with a racetrack length of 40 µm, where the gap between the straight waveguide and ring is set to 150 nm. The MRR shows a Full-Width-Half-Maximum (FWHM) of 0.22 nm at 2262 nm, corresponding to a quality factor of $1.03 \times 10^4$.

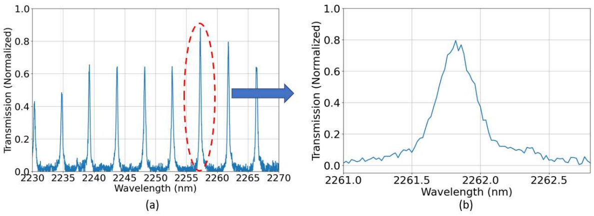

Fig. 3. Spectra of Ge-SOI MRRs.

### *B. Performance of Ge Vernier filter*

One typical method to implement a tunable laser on a PIC is implementing a Vernier filter [8], consisting of two MRRs with slightly different radii. The transmission through both drop ports of two MRRs will reach a maximum when the resonant peaks of the two MRRs overlap. Choosing different radii leads to different free spectral ranges (FSRs). The design and patterned Vernier filter with integrated round heaters & contact pads inside the rings are shown in Fig. 4 (a) and (b) respectively, allowing us to tune both rings thermally using a direct current (DC) probe card. The transmission spectrum of a vernier filter with a radius difference of 2 µm, resulting in an FSR of 94 nm at 2.3 µm are shown in Fig. 4 (c) and (d) when the applied voltage are 2V and 5V respectively.

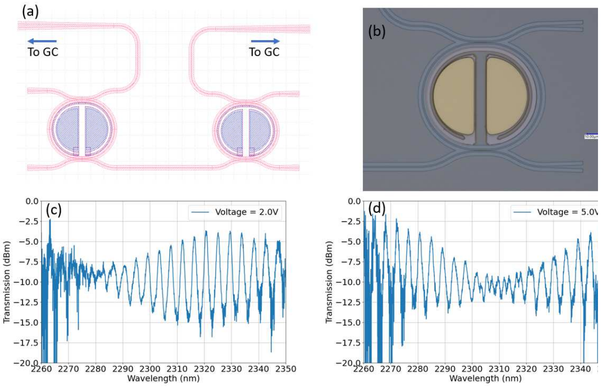

Fig. 4. (a) GDS design of GeSOI Vernier filter; (b) Patterned Vernier filter with heater and contact pads; (c) (d) Thermal tuning of Vernier filter.

### *C. GaSb µTP on Ge-SOI platform*

Fig. 5 (a) shows the top view of patterned and released coupons on the GaSb source sample before the transfer-printing step, where the coupons have a width of 45 µm. After printing on the patterned Ge-SOI, the coupon can be post-processed, as shown in Fig. 5 (b). The FIB image is given in Fig. 5 (c), showing a fine bonding between III-V coupon and Ge-SOI.

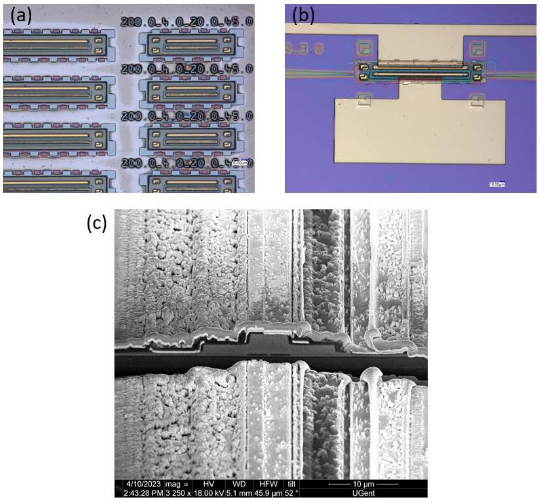

Fig. 5. (a) GaSb coupons after release etch (ready for picking-up); (b) GaSb coupons after µTP and final metalization; (c) FIB cross-section of transfer-printed GaSb coupon.

## IV. DISCUSSION AND OUTLOOK

In this work, characterized the building blocks (waveguides, MRRs, Vernier filters) on a dedicated Ge-SOI platform, which could be used for the passive circuits of a heterogeneously integrated laser. We have fabricated GaSb amplifiers on native III-V wafers and successfully transfer-printed them on the Ge-SOI platform. To further reduce the loss, we can replace Ge with SiGe, which possesses a better lattice-match with Si. Besides, SiGe is transparent at shorter wavelengths, as Ge typically shows strong absorption below 2.1 µm.

On the other hand, to make the platform more robust and versatile, we can expand the platform to the underneath Si waveguide layer by selectively etching the Ge layer [16]. In this way, both Ge and Si are exposed as the top layer on a single chip, which gives the possibility to integrate lasers from 1.1 – 2.5 µm.

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