Letters

Noncontact Integration of Photonic IC and Electronic IC via Inductively Coupled Interconnects

Tongchuan Ma, Liyiming Yang, Yanlu Li, and Yuan Du

***Abstract*— This letter presents an innovative noncontact packaging technique for photonic integrated circuits (PICs) and electronic integrated circuits (EICs) through inductively coupled interconnects. The primary aim of this approach is to enhance thermal isolation between the heat-generating electrical logic die and the thermally sensitive optical interferometer die. The feasibility of this contactless transceiver, which fulfills information transmission from the laser Doppler vibrometry (LDV) to the EIC, is substantiated via electromagnetic simulations. Furthermore, thermal simulations conducted by COMSOL prove that this packaging configuration could potentially reduce the temperature of PICs by up to 4.6 °C when compared to the conventional 3-D stack packaging, underlining its potential for improved thermal performance.**

***Index Terms*— 3-D integration, inductive-coupling link.**

I. Introduction

Developing a proper co-packaging technique for photonic integrated circuits (PICs) and electronic integrated circuits (EICs) has gained significant attention in recent years [1], [2], [3]. It is able to combine the strengths of both EIC and PIC: PICs demonstrate superior performance in data transmission and sensing [4], while EICs have the capability of massive signal processing [5], [6].

To enable independent process selection for each device, hybrid integration has been proposed rather than monolithic integration techniques [7]. The most straightforward way of hybrid integration is through wire bonding [8], shown in Fig. 1(b). The electronic and photonic chips are juxtaposed on a common substrate (e.g., PCB). The limited chip area and the 1-D placement of the metal pads in the sharing edge constrain the total pin count of the interconnection; moreover, channel impedance discontinuity and wire skin effect confine the bandwidth of each I/O. The 3-D integration approach offers a way to integrate complex systems in a small footprint with short low-parasitic interconnects. As shown in Fig. 1(c), the interconnection and adhesion of the face-to-face placed electronic and photonic chips is realized by the microsolder bump and under-bump-metallization (UBM) layer [9]. The form of this integration requires a process comprising lithography, metal deposition, and thermocompression, which is quite costly. Moreover, the interconnect is especially sensitive to misalignment either horizontally or vertically [10]. For the integration of PIC with EIC, this stacked scheme comes up with a new problem: the energy-consuming logic computing component produces massive heat [11]. This will lead to significant troubles in many PIC devices that are based on optical interferometers [12], which can be very sensitive to temperature variations due to the high-temperature coefficient of the refractive index of the photonic waveguides (1.8×10^{-4}/K for silicon).

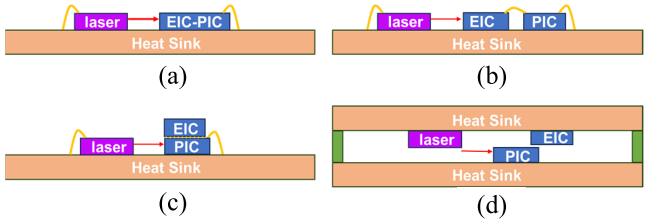

Fig. 1. (a) Monolithic integration. (b) Hybrid integration through wire bonding. (c) Three-dimensional face-to-face hybrid integration. (d) Contactless vertical interconnection hybrid integration.

Contactless vertical interconnection could be a superior option for the integration of PICs and EICs. By utilizing the electromagnetic coupling between inductors, it is capable of addressing some of the limitations inherent in 3-D integration [13], [14]. First of all, it is less costly since there is no additional process needed other than the original photoelectron and CMOS process. Second, it has a better tolerance for bonding misalignment [15]. Furthermore, contactless link possesses better thermal isolation [16], [17], and the air gap between the chips provides a high thermal resistance between the thermal conductively silicon substrates.

This letter will focus on the noncontacting inductively integration of one specific system: a multibeam laser Doppler vibrometry (LDV) system. This system measures the vibrations of a target through the Doppler effect of the reflected sensing beams [18]. A PIC-based multibeam LDV comprises a laser source with an optical isolator, a PIC with multiple interferometers (the core part of the laser Doppler vibrometers, which is heat-sensitive), and an EIC, including multiple transimpedance amplifiers (TIAs) and a digital signal processor (DSP). Incorporating an appropriate co-packaging approach could potentially miniaturize this system and dramatically improve the signal quality and power consumption.

II. Proposed Method

The packing structure of our proposed noncontacting packaging LDV system is shown in Fig. 1(d). The PIC performs as a multibeam LDV. When the laser is scattered by the moving surface of the target, a Doppler frequency shift occurs, after which it is mixed interferometrically producing a megahertz range photocurrent. This photocurrent is injected into the transmit inductors without any amplification circuit because the process we apply for the PIC could not provide any FET devices. The modulator and photodiode are positioned on the left side of the PIC, to be as far from the heat source as possible.

The laser source is put on the left side of the photonic chip and kept at a distance of 5 mm to minimize the thermal impact on the PIC. The electronic chip is placed face-to-face in the upper right side of the photonic chip with a distance of tens of micrometers. The transmitting

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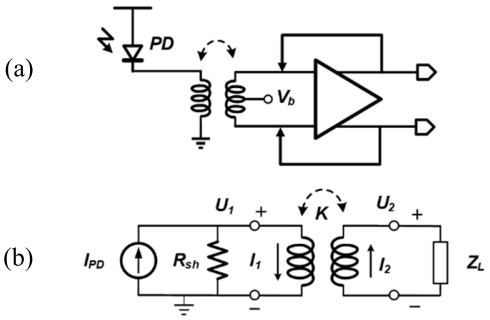

Fig. 2. (a) Block diagram of the PIC and EIC interface. (b) Equivalent model.

and receiving inductors will be printed in the overlap region. Other PIC and EIC I/O pins and power supplies are distributed on the other three sides of the chips and wire bonded to the PCB. To our intuition, with a larger distance and smaller overlap between the EIC and PIC, the thermal isolation would be better while the link efficiency would be worse. So, to properly leverage between thermal isolation and electrical link efficiency, HFSS and COMSOL are used to analyze the impact of gap and overlap on the received signal strength and the temperature increase of the PIC, and a latch amplifier is established with a 28-nm CMOS process model to amplify the weak signal for the subsequent digital signal processing.

A. Electromagnetic Simulation

Fig. 2(a) shows the block diagram of the PIC and EIC interface. The inductive coupled link could be regarded as a balun, turning the single-ended signal from PD, into a differential signal with a dc bias V_b fed through the center tap of the secondary inductor, to define an operating point of the nMOS in the latch amplifier. The equivalent model is shown in Fig. 2(b), where the PD is modelized into an ac current source I_{PD} with a shunt resistance R_{sh} and the amplifier is modelized into a load impedance Z_L. The high output resistance of the PD R_{sh} is transferred into a low output resistance approximating to the impedance of the secondary inductor Z_2. This indicates that TIA is not appropriate for the amplifying of the output signal. A voltage-gain stage is needed for the application.

The inductors are modelized and simulated in HFSS, shown in Fig. 3(a). The metal thickness of the inductors is set to be 500 nm. To evaluate the influence of the inductors' diameter on the link strength and leverage between pitch size and channel gain, three-coil inductors with the diameters of 70, 120, and 190 μm are chosen for the simulation. The respective inductance is shown in Fig. 3(b). The channel gain of each pair of inductors is simulated with various distances, and the respective s-parameters are then imported into Cadence and tested in a circuit as in Fig. 2(b). I_{PD} is set as 1 μA and R_{sh} as 60 KΩ. The output voltage of the secondary inductor U_2 is shown in Fig. 3(c) and (d). Fig. 3(c) plotted the output as a function of the beat current frequency, demonstrating a linear relationship. Fig. 3(d) shows the output voltage when different air gaps are applied with a pair of 190-μm-diameter inductors. They are in a negative exponent relation. The dashed lines are fitted curves with $U_2 \propto e^{d/d0}$, and they have a good agreement with the simulated points.

This inductively coupled interconnect shows a high resistance to the horizontal chip misalignment. All three pairs of inductors are tested for misalignment loss, as shown in Fig. 4. The larger inductor size corresponds to a smaller sensitivity to mismatch, but even for the 70-μm-diameter inductor, the misalignment loss is smaller than 3 dB when the offset is as large as 20 μm.

B. Thermal Simulation

To reveal the heat-handling advantage of our proposed package, thermal simulations are performed by COMSOL. To simplify the

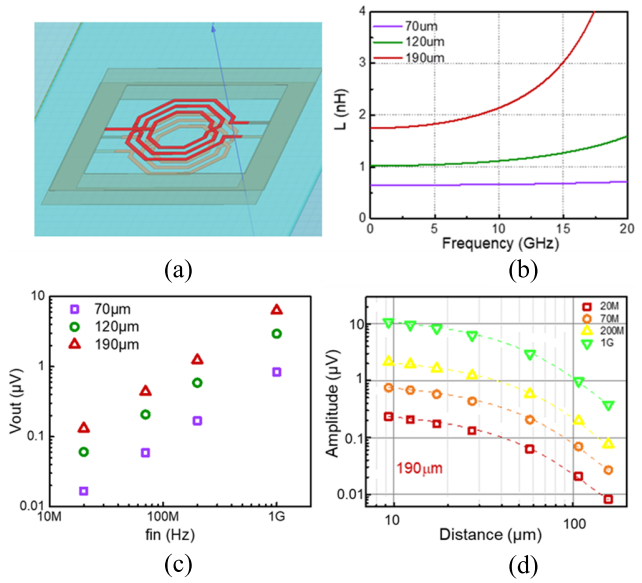

Fig. 3. (a) Inductors model in HFSS. (b) Inductance of inductors with different diameters. (c) Output voltage as a function of the carrier frequency. (d) Output voltage as a function of the chip distance.

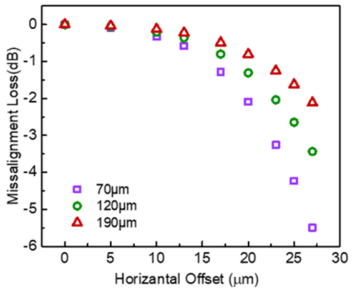

Fig. 4. Relationship between loss and offset.

calculation, a 2-D scheme is applied. All three active components are placed as in Fig. 1, the heavily heat-producing laser and EIC are attached to one aluminum heat sink, and PIC is attached to another. The whole package transfers heat to the surrounding air through radiation and convection, which complies with laminar flow module. The ambient temperature is set to be 293.15 K. In our thermal simulation, all of the EICs and lasers are set with a heat generation power of 0.01 W. The distance between the lasers and the PICs is kept at a constant of 5 mm for all three package schemes. The heat sinks in all the three simulated packages are kept the same size for a fair comparison. The simulated temperature distribution is shown in Fig. 5. The surface temperatures of the PICs as a function of the position are plotted in Fig. 5(d). It is obvious that this vertical contactless integration through inductively coupled connection has the best performance in heat management. The surface temperature has a 4.6 °C decrease than that of the 3-D stacked packaging.

The temperature changes of the PIC with different air gaps are also simulated, as shown in Fig. 6. We can conclude that the heat isolation does not differ much when the gap is larger than 10 μm. Besides, thermal isolation can be further improved if the inner space is set to vacuum, as shown in Fig. 6. On the other hand, the voltage amplitude decreases exponentially with distance. Therefore, we assign the distance between the two chips as 10 μm.

C. Amplification Circuit

The structure of the used latch amplifier and its output voltage waveforms are shown in Fig. 7(a) and (b). As shown in this figure, the amplifier consists of two stages, the amplifier stage and the latch

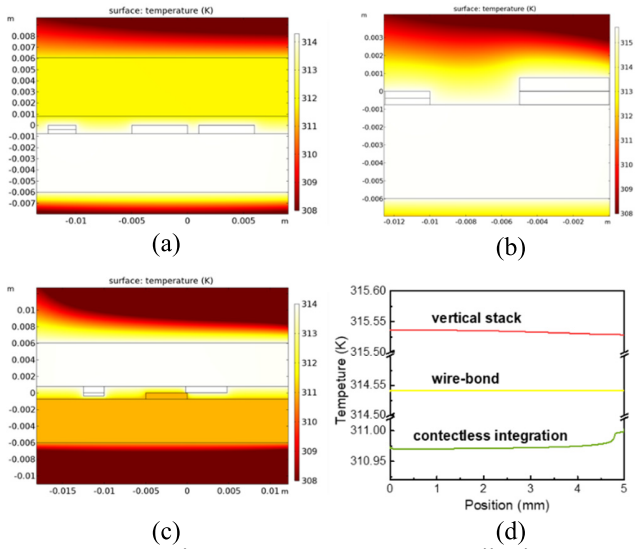

Fig. 5. Simulated temperature distribution of (a) integration through wire bonding, (b) three-dimensional face-to-face integration, (c) contactless vertical integration, and (d) surface temperature of the PICs.

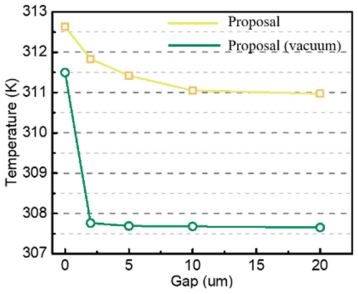

Fig. 6. Surface temperature as a function of the air gap.

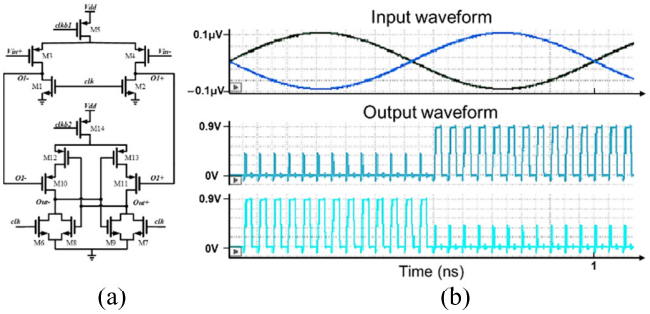

Fig. 7. (a) Schematic of the latch amplifier. (b) Output voltage waveforms.

stage. In this circuit, the input differential signal is amplified to motivate the latch stage and the latch amplifies it to settle at V_{dd} and *Gnd*. The latched output voltage is reset at each clock period. Shown in Fig. 7(b), the amplifier is simulated with an HFSS-extracted channel, which consist of 190-μm inductors and a 10-μm air gap.

The amplitude of the output signal is ignored while the frequency is retained, which correspond to the vibrating frequency of the object.

III. Conclusion

This noncontacting packaging of PIC with EIC through inductively coupled interconnects we propose has shown its capability of improving the thermal isolation and tolerance of misalignment between EIC and PIC. With the help of a pair of vertically aligned inductors and the after-stage latch amplifier, the detected vibrating frequency of the object is delivered from the PIC to the EIC. Both the electrical signal transmission and heat conduction dependence on the distance between the PIC and the EIC are simulated. A 10-μm gap is selected to leverage between signal strength and thermal isolation. At this distance, the proposed noncontacting package provides a 4.6 °C reduction of temperature at the surface of the PIC compared to that of 3-D integration.

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